High-Performance Digital MEMS Microphone Standard Digital Audio Interface to Blackfin DSP

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 allows up to two digital MEMS microphones to be interfaced to a DSP on a single data line. The INMP441 consists of a MEMS microphone element and an I^2S output. This allows stereo microphones to be used in an audio system without the need for a codec between the microphones and the processor. InvenSense MEMS microphones have a high signal-to-noise ratio (SNR) and a flat wideband frequency response, making them an excellent choice for high performance, low power applications.

Up to two INMP441 microphones can be input to a single data line on the ADSP-BF527 Blackfin® processor. The ADSP-BF527 can be set up with up to four serial data inputs; therefore, up to eight INMP441s can connect to a single DSP.

CIRCUIT DESCRIPTION

The INMP441 microphones are connected to the SPORT data input pins of the ADSP-BF527. The only necessary passive components in this circuit are a single 0.1 µF bypass capacitor for each INMP441 and a large pull-down resistor (100 kΩ) on the SD line to discharge it while the INMP441 output drivers are tristated. Place the bypass capacitors as close to the INMP441 V_{DD} pin (Pin 7) as possible. Supply the microphones' V_{DD} from the same source as the 2.25 V to 3.3 V V_{DDEXT} of the ADSP-BF527. Even though the INMP441 can operate with VDD between 1.8 V and 3.3 V, V_{DDEXT} on the ADSP-BF527 must be a minimum of 2.25 V.
There are three signals that must be connected between the INMP441 and ADSP-BF527 for the I^2S data stream: frame clock, bit clock, and data. The ADSP-BF527 is the system clock master and generates the two I^2S clocks.
This circuit demonstrates the microphones connected to a single data input on the SPORT0 of the Blackfin. Each of the two SPORTs of the ADSP-BF527 has two sets of data receive pins that enable up to eight channels of I^2S audio in. Table 1 shows the connections when using the serial SPORT0 of the ADSP-BF527.

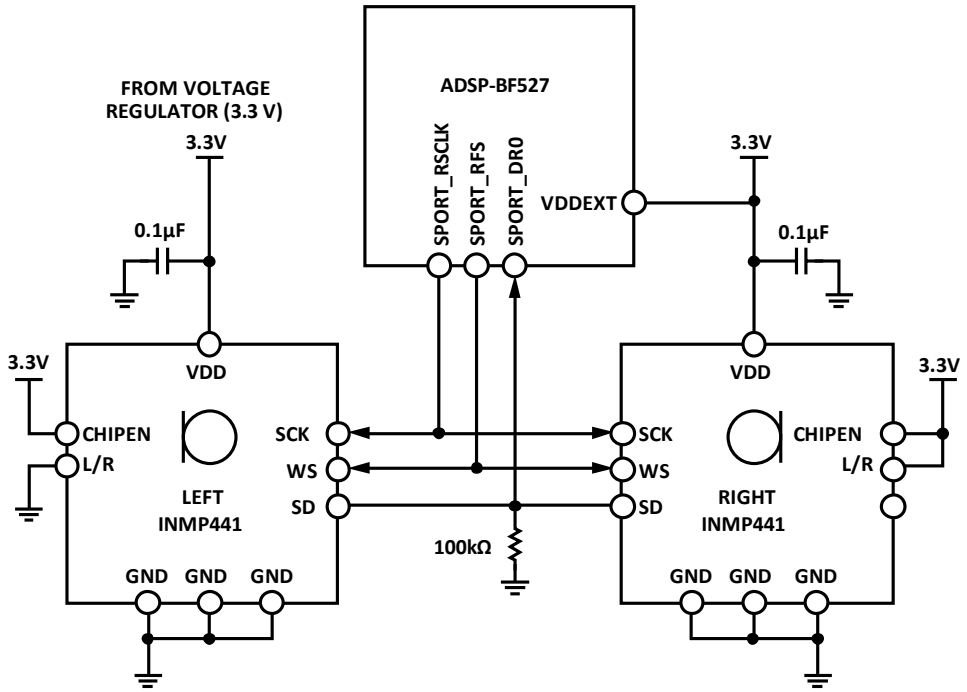

Figure 1. MEMS Microphone Connection to Blackfin DSP (Simplified Schematic: All Connections Not Shown)

InvenSense reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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Table 1. Hardware Signal Connections

Signal	INMP441	ADSP-BF527
Frame Clock	WS (Pin 3)	PF1/PPI_D1/RFS0 (Pin PF1)
Bit Clock	SCK (Pin 1)	PF2/PPI_D2/RSCLK0 (Pin PF2)
Serial Data	SD (Pin 2)	PF0/PPI_D0/DR0PRI (Pin PF0)

Set the L/R pin on the two INMP441s to opposite levels—one pulled to V_{DD} and the other to GND. When pulled to GND, the microphone outputs its data on the left channel of the I^2S stream, and when pulled to V_{DD}, it outputs its data on the right channel.
The INMP441 is enabled by pulling the CHIPEN pin high. This pin can be tied either directly to the V_{DD} of the microphone, which keeps it always enabled while it is powered, or it can be connected to a GPIO on the ADSP-BF527, allowing the Blackfin to enable and disable the microphone.

The INMP441 has a sensitivity of −26 dBFS. In most applications, the microphone outputs require some gain added in the signal path of the Blackfin. If gain is added to the signal in the DSP, the output of the processor must still be limited to 0 dBFS.

ADSP-BF527 REGISTER SETTINGS

The SPORT register settings to set the ADSP-BF527 into I^2S master mode follow. A more detailed description of these register settings can be found in the ADSP-BF52x Blackfin Processor Hardware Reference.
Configure SPORT_RCR1, the primary receive configuration register, with the following non-default settings:

- RCKFE: Drive internal frame sync on falling edge of RSCLK
- RFSR: Require RFS for every data-word
- IRFS: Internal RFS used
- IRSCLK: Internal receive clock select

Configure SPORT_RCR2, the secondary receive configuration register, with the following non-default settings:

- RSFSE: Receive stereo frame sync enable
- SLEN: 32-bit word length

Set SPORT_RCLKDIV, the SPORT receive serial clock divider register, to 17 (0x0011) and set SPORT_RFSDIV to 31 (0x001F). This sets the proper clock frequencies for a 48 kHz frame clock and 3.072 MHz bit clock with a 120 MHz Blackfin system clock (SCLK).
The registers settings described can be applied to either SPORT0 or SPORT1 on the ADSP-BF527, depending on which is being used.

COMMON VARIATIONS

DSPs

This circuit can also be set up with other parts from the Blackfin family instead of an ADSP-BF527. See the appropriate data sheets for details on the differences in number of SPORT channels and other variations.

Microphones

By removing one of the INMP441 microphones, a mono microphone circuit using a single INMP441 can be set up. The other connections remain the same in this mono configuration.

Additional INMP441 microphones can be connected to the SPORT inputs of the ADSP-BF527 in the same way as the first stereo pair.

CIRCUIT EVALUATION AND TEST

The easiest way to evaluate a system with the INMP441 MEMS microphone connected via I^2S to the ADSP-BF527 Blackfin DSP is to use the EV_INMP441Z evaluation board and the Blackfin SDP. These boards are designed to work together and include code to enable the digital audio connection. When connected to the USB port of a PC, the system is identified as a standard USB audio interface and enables streaming of stereo audio from the microphones to the PC.

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Equipment Needed

The two evaluation kits needed include the following:

- EV_INMP441: includes one EV_INMP441-FX board and an interface PCB.
- EVAL-SDP-CB1Z: includes SDP-B controller board

For correct operation of the SDP board, the PC must have the following minimum configuration:

- Windows XP Service Pack 2, Windows Vista (32-bit), or Windows 7 (32-bit).
- USB 2.0 port

A second EV_INMP441-FX can be connected to the interface board to enable stereo audio capture.

Getting Started

The microphone flex PCBs connect to the interface board with ZIF headers, J1 and J2, and the EV_INMP441 connects to the SDP-B with 120-pin header, J3.

The documentation for the SDP-B controller board and EV_INMP441 describes the system setup and gives complete schematics of the boards. The only external connections required are the USB connection to the PC and system power to the INMP441 evaluation board.

Complete documentation for theEV_INMP441 evaluation board can be found in the UG-362 user guide.
Complete documentation for the SDP-B controller board can be found in the SDP-B User Guide, UG-277.

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
2/22/2014	1.0	Initial Release

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