# ICM-20690 Datasheet



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# 1 INTRODUCTION

## 1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-20690 Dual-Interface MotionTracking device. The device is housed in a small 2.5x3x0.91 mm 14-pin LGA package.

## 1.2 PRODUCT OVERVIEW

The ICM-20690 is a 6-axis MotionTracking device with a main Interface for UI and an Auxiliary interface configurable as SPI slave for Optical Image Stabilization (OIS) applications or as $I^2C$ Master to support other sensors such as a compass or pressure sensor. It combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.91 mm (14-pin LGA) package. The device supports independent data paths for UI and OIS, with independent control for full-scale range (FSR), output data rate (ODR).

ICM-20690 also features a 1K-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-20690, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope and accelerometer support the following independently programmable full-scale range settings:

| Signal Path | Gyroscope | Accelerometer |
|---|---|---|
| **UI Path** | ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec | ±2, ±4, ±8, ±16g |
| **OIS Path** | ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec | ±1, ±2, ±4, ±8g |

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features $I^2C$ and SPI serial interfaces, a VDD operating range of 1.71 V to 3.45 V, and a separate digital IO supply, VDDIO from 1.71 V to 3.45 V.

The host interface can be configured to support SPI slave or $I^2C$ slave modes. The SPI interface supports speeds up to 10 MHz and the $I^2C$ interface supports speeds up to 400 kHz. A secondary interface can be configured to support SPI slave mode (3-wire) for interfacing to OIS controllers, or $I^2C$ master mode for interfacing to external sensors. The SPI interface supports speeds up to 20 MHz and the $I^2C$ interface supports speeds up to 400 kHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.91 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

## 1.3 APPLICATIONS

- Smartphones and Tablets
- Head Mounted Displays
- Wearable Sensors

# 2 FEATURES

## 2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-20690 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with independently programmable full-scale range of ±31.25, ±62,5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec for UI and OIS paths
- Integrated 16-bit ADCs per axis
- Digitally-programmable low-pass filters
- Low-power gyroscope operation
- Factory calibrated sensitivity scale factor
- Self-test

## 2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-20690 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with independently programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* for UI path and ±1*g*, ±2*g*, ±4*g* and ±8*g* for OIS path
- Integrated 16-bit ADCs per axis
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

## 2.3 ADDITIONAL FEATURES

The ICM-20690 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 2.5x3x0.91 mm (14-pin LGA)
- 1K byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 20,000 *g* shock tolerant
- Main interface: 10 MHz SPI / 400 kHz $I^2C$ slave host interface
- Auxiliary interface: 20 MHz SPI slave OIS controller interface / 400 kHz $I^2C$ master interface for external sensors
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

# 3 ELECTRICAL CHARACTERISTICS

## 3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **GYROSCOPE SENSITIVITY** | | | | | | |
| Full-Scale Range | FS_SEL=0 | | ±250 | | º/s | 3 |
| | FS_SEL=1 | | ±500 | | º/s | 3 |
| | FS_SEL=2 | | ±1000 | | º/s | 3 |
| | FS_SEL=3 | | ±2000 | | º/s | 3 |
| | FS_SEL=5 | | ±31.25 | | º/s | 3 |
| | FS_SEL=6 | | ±62.5 | | º/s | 3 |
| | FS_SEL=7 | | ±125 | | º/s | 3 |
| Gyroscope ADC Word Length | | | 16 | | bits | 3 |
| Sensitivity Scale Factor | FS_SEL=0 | | 131 | | LSB/(º/s) | 3 |
| | FS_SEL=1 | | 65.5 | | LSB/(º/s) | 3 |
| | FS_SEL=2 | | 32.8 | | LSB/(º/s) | 3 |
| | FS_SEL=3 | | 16.4 | | LSB/(º/s) | 3 |
| | FS_SEL=5 | | 1048.6 | | LSB/(º/s) | 3 |
| | FS_SEL=6 | | 524.3 | | LSB/(º/s) | 3 |
| | FS_SEL=7 | | 262 | | LSB/(º/s) | 3 |
| Sensitivity Scale Factor Initial Tolerance | 25°C | | ±1 | | % | 1 |
| Sensitivity Scale Factor Variation Over Temperature | -40°C to +85°C | | ±0.01 | | %/ºC | 1 |
| Nonlinearity | Best fit straight line; 25°C | | ±0.1 | | % | 1 |
| Cross-Axis Sensitivity | | | ±1 | | % | 1 |
| **ZERO-RATE OUTPUT (ZRO)** | | | | | | |
| Initial ZRO Tolerance | 25°C | | ±1 | | º/s | 1 |
| ZRO Variation vs. Temperature | -40°C to +85°C | | ±0.01 | | º/s/ºC | 1 |
| **OTHER PARAMETERS** | | | | | | |
| Rate Noise Spectral Density | @ 10 Hz | | 0.004 | | º/s/√Hz | 1 |
| Total RMS Noise | Bandwidth = 100 Hz | | 0.04 | | º/s-rms | 1, 4 |
| Gyroscope Mechanical Frequencies | | 25 | 27 | 29 | KHz | 2 |
| Low Pass Filter Response | Programmable Range | 5 | | 250 | Hz | 3 |
| Gyroscope Start-Up Time | Time from gyro enable to gyro drive ready | | 80 | | ms | 1, 5 |
| Output Data Rate | Low-Noise Mode | 3.91 | | 32k | Hz | 3 |
| | Low-Power Mode | 3.91 | | 333.33 | Hz | 3 |

**Table 1. Gyroscope Specifications**

**Notes:**

1. Target spec. Subject to update.
2. Tested in production.
3. Guaranteed by design.
4. For low-noise mode.
5. The gyroscope output will be stable if ~200 ms are provided between a disable and the subsequent enable of the sensor.

## 3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **ACCELEROMETER SENSITIVITY** | | | | | | |
| Full-Scale Range | AFS_SEL=0 | | ±2 | | *g* | 2 |
| | AFS_SEL=1 | | ±4 | | *g* | 2 |
| | AFS_SEL=2 | | ±8 | | *g* | 2 |
| | AFS_SEL=3 | | ±16 | | *g* | 2 |
| ADC Word Length | Output in two's complement format | | 16 | | bits | 2 |
| Sensitivity Scale Factor | AFS_SEL=0 | | 16,384 | | LSB/*g* | 2 |
| | AFS_SEL=1 | | 8,192 | | LSB/*g* | 2 |
| | AFS_SEL=2 | | 4,096 | | LSB/*g* | 2 |
| | AFS_SEL=3 | | 2,048 | | LSB/*g* | 2 |
| Sensitivity Scale Factor Initial Tolerance | Component-level | | ±1 | | % | 1 |
| Sensitivity Change vs. Temperature | -40°C to +85°C | | ±0.008 | | %/ºC | 1 |
| Nonlinearity | Best Fit Straight Line | | ±0.3 | | % | 1 |
| Cross-Axis Sensitivity | | | ±1 | | % | 1 |
| **ZERO-G OUTPUT** | | | | | | |
| Initial Tolerance | Board-level, all axes | | ±40 | | m*g* | 1 |
| Zero-G Level Change vs. Temperature | X & Y-axis (-40°C to +85°C) | | ±0.5 | | m*g*/ºC | 1 |
| | Z-axis (-40°C to +85°C) | | ±1 | | m*g*/ºC | 1 |
| **OTHER PARAMETERS** | | | | | | |
| Power Spectral Density | @ 10 Hz | | 100 | | µ*g*/√Hz | 1 |
| RMS Noise | Bandwidth = 100 Hz | | 1 | | mg-rms | 1, 3 |
| Low-Pass Filter Response | Programmable Range | 5 | | 218 | Hz | 2 |
| Accelerometer Startup Time | From sleep mode to valid data | | 10 | | ms | 2 |
| Output Data Rate | Low-Noise Mode | 3.91 | | 4000 | Hz | 2 |
| | Low-Power Mode | 3.91 | | 500 | Hz | 2 |

**Table 2. Accelerometer Specifications**

**Notes:**

1. Target spec. Subject to update.
2. Guaranteed by design.
3. For low-noise mode.

## 3.3 ELECTRICAL SPECIFICATIONS

### 3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGES** | | | | | | |
| VDD | | 1.71 | 1.8 | 3.45 | V | 2 |
| VDDIO | | 1.71 | 1.8 | 3.45 | V | 2 |
| **SUPPLY CURRENTS** | | | | | | |
| Low-Noise Mode | 6-Axis Gyroscope + Accelerometer | | 3.1 | | mA | 1 |
| | 3-Axis Accelerometer | | 440 | | µA | 1 |
| | 3-Axis Gyroscope | | 2.9 | | mA | 1 |
| Accelerometer Low -Power Mode (Gyroscope disabled) | 100Hz ODR, 1x averaging | | 50 | | µA | 1 |
| Gyroscope Low-Power Mode (Accelerometer disabled) | 100Hz ODR, 1x averaging | | 1.40 | | mA | 1 |
| 6-Axis Low-Power Mode (Gyroscope Low-Power Mode; Accelerometer Low-Noise Mode) | 100Hz ODR, 1x averaging | | 1.66 | | mA | 1 |
| Full-Chip Sleep Mode | At 25ºC | | 6 | | µA | 1 |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Temperature Range | Performance parameters are not applicable beyond Specified Temperature Range | -40 | | +85 | °C | 1 |

**Table 3. D.C. Electrical Characteristics**

**Notes:**

1. Target spec. Subject to update.
2. Derived from validation or characterization of parts, not guaranteed in production.



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### 3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SUPPLIES** | | | | | | |
| Supply Ramp Time | Monotonic ramp. Ramp rate is 10% to 90% of the final value | 0.01 | | 3 | ms | 1 |
| Power Supply Noise | | | 10 | | mV peak-peak | 1 |
| **TEMPERATURE SENSOR** | | | | | | |
| Operating Range | Ambient | -40 | | 85 | °C | 1 |
| 25°C Output | | | 0 | | LSB | 3 |
| ADC Resolution | | | 16 | | bits | 2 |
| ODR | Without Filter | | 8000 | | Hz | 2 |
| | With Filter | 3.91 | | 1000 | Hz | 2 |
| Room Temperature Offset | 25°C | -15 | | 15 | °C | 3 |
| Stabilization Time | | | | 14000 | µs | 2 |
| Sensitivity | Untrimmed | | 326.8 | | LSB/°C | 1 |
| Sensitivity Error | | -2.5 | | +2.5 | % | 1 |
| **POWER-ON RESET** | | | | | | |
| Start-up time for register read/write | From power-up | | | 1 | ms | 1 |
| **I²C ADDRESS** | | | | | | |
| **I²C ADDRESS** | AD0 = 0<br>AD0 = 1 | | 1101000<br>1101001 | | | |
| **DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)** | | | | | | |
| $V_{IH}$, High Level Input Voltage | | 0.7*VDDIO | | | V | 1 |
| $V_{IL}$, Low Level Input Voltage | | | | 0.3*VDDIO | V | |
| $C_I$, Input Capacitance | | | < 10 | | pF | |
| **DIGITAL OUTPUT (SDO, INT1, INT2)** | | | | | | |
| $V_{OH}$, High Level Output Voltage | $R_{LOAD}$=1 MΩ; | 0.9*VDDIO | | | V | 1 |
| $V_{OL1}$, LOW-Level Output Voltage | $R_{LOAD}$=1 MΩ; | | | 0.1*VDDIO | V | |
| $V_{OL.INT}$, INT Low-Level Output Voltage | OPEN=1, 0.3 mA sink Current | | | 0.1 | V | |
| Output Leakage Current | OPEN=1 | | 100 | | nA | |
| $t_{INT}$, INT Pulse Width | LATCH_INT_EN=0 | | 50 | | µs | |
| **I²C I/O (SCL, SDA)** | | | | | | |
| $V_{IL}$, LOW-Level Input Voltage | | -0.5 V | | 0.3*VDDIO | V | 1 |
| $V_{IH}$, HIGH-Level Input Voltage | | 0.7*VDDIO | | VDDIO + 0.5 V | V | |
| $V_{hys}$, Hysteresis | | | 0.1*VDDIO | | V | |
| $V_{OL}$, LOW-Level Output Voltage | 3 mA sink current | 0 | | 0.4 | V | |
| $I_{OL}$, LOW-Level Output Current | $V_{OL}$=0.4 V<br>$V_{OL}$=0.6 V | | 3<br>6 | | mA<br>mA | |
| Output Leakage Current | | | 100 | | nA | |
| $t_{of}$, Output Fall Time from $V_{IHmax}$ to $V_{ILmax}$ | $C_b$ bus capacitance in pf | 20+0.1$C_b$ | | 300 | ns | |
| **INTERNAL CLOCK SOURCE** | | | | | | |
| Sample Rate | FCHOICE_B=1,2,3; SMPLRT_DIV=0 | | 32 | | kHz | 2 |
| | FCHOICE_B=0;<br>DLPFCFG=0 or 7<br>SMPLRT_DIV=0 | | 8 | | kHz | 2 |
| | FCHOICE_B=0;<br>DLPFCFG=1,2,3,4,5,6;<br>SMPLRT_DIV=0 | | 1 | | kHz | 2 |
| Clock Frequency Initial Tolerance | CLK_SEL=0, 6 or gyro inactive; 25°C | -3 | | +3 | % | 1 |
| | CLK_SEL=1,2,3,4,5 and gyro active; 25°C | -1 | | +1 | % | 1 |
| Frequency Variation over Temperature | CLK_SEL=0,6 or gyro inactive. (-40°C to +85°C) | | | ±2 | % | 1 |
| | CLK_SEL=1,2,3,4,5 and gyro active | | | ±2 | % | 1 |

**Table 4. A.C. Electrical Characteristics**

**Notes:**

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.
3. Production tested.

### 3.3.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SERIAL INTERFACE** | | | | | | |
| SPI Operating Frequency, All Registers Read/Write | Low Speed Characterization | 100 | 100 ±10% | | kHz | 1,3 |
| | High Speed Characterization | 0.2 | 1 | 10 | MHz | 1, 2, 3 |
| | OIS Mode Characterization | | | 20 | MHz | 1, 2, 3 |
| SPI Modes | | | 0 and 3 | | | |
| $I^2C$ Operating Frequency | All registers, Fast-mode | 100 | | 400 | kHz | 1 |
| | All registers, Standard-mode | | | 100 | kHz | 1 |

**Table 5. Other Electrical Specifications**

**Notes:**

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 10-MHz/20-MHz operation.
3. Minimum SPI/$I^2C$ clock rate is dependent on ODR. If ODR is below 4 kHz, minimum clock rate is 100 kHz. If ODR is greater than 4 kHz, minimum clock rate is 200 kHz.



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## 3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| Parameters | Conditions | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| **I²C TIMING** | **I²C FAST-MODE** | | | | | |
| $f_{SCL}$, SCL Clock Frequency | | 100 | | 400 | kHz | 1 |
| $t_{HD.STA}$, (Repeated) START Condition Hold Time | | 0.6 | | | µs | 1 |
| $t_{LOW}$, SCL Low Period | | 1.3 | | | µs | 1 |
| $t_{HIGH}$, SCL High Period | | 0.6 | | | µs | 1 |
| $t_{SU.STA}$, Repeated START Condition Setup Time | | 0.6 | | | µs | 1 |
| $t_{HD.DAT}$, SDA Data Hold Time | | 0 | | | µs | 1 |
| $t_{SU.DAT}$, SDA Data Setup Time | | 100 | | | ns | 1 |
| $t_r$, SDA and SCL Rise Time | $C_b$ bus cap. from 10 to 400 pF | 20+0.1$C_b$ | | 300 | ns | 1 |
| $t_f$, SDA and SCL Fall Time | $C_b$ bus cap. from 10 to 400 pF | 20+0.1$C_b$ | | 300 | ns | 1 |
| $t_{SU.STO}$, STOP Condition Setup Time | | 0.6 | | | µs | 1 |
| $t_{BUF}$, Bus Free Time Between STOP and START Condition | | 1.3 | | | µs | 1 |
| $C_b$, Capacitive Load for each Bus Line | | | < 400 | | pF | 1 |
| $t_{VD.DAT}$, Data Valid Time | | | | 0.9 | µs | 1 |
| $t_{VD.ACK}$, Data Valid Acknowledge Time | | | | 0.9 | µs | 1 |

**Table 6. I²C Timing Characteristics**

**Notes:**

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

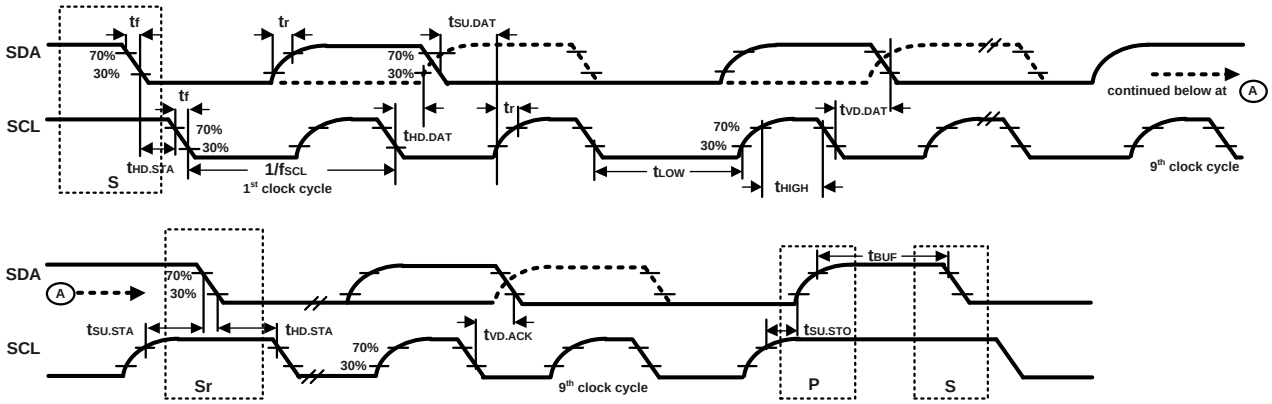


**Figure 1. I²C Bus Timing Diagram**



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## 3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

The following section is applicable to 4-wire SPI mode for the Main Interface.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SPI TIMING** | | | | | | |
| $f_{SPC}$, SCLK Clock Frequency | | | | 10 | MHz | 1 |
| $t_{LOW}$, SCLK Low Period | | 56 | | | ns | 1 |
| $t_{HIGH}$, SCLK High Period | | 56 | | | ns | 1 |
| $t_{SU.CS}$, CS Setup Time | | 2 | | | ns | 1 |
| $t_{HD.CS}$, CS Hold Time | | 63 | | | ns | 1 |
| $t_{SU.SDI}$, SDI Setup Time | | 3 | | | ns | 1 |
| $t_{HD.SDI}$, SDI Hold Time | | 7 | | | ns | 1 |
| $t_{VD.SDO}$, SDO Valid Time | $C_{load}$ = 20 pF | | | 40 | ns | 1 |
| $t_{HD.SDO}$, SDO Hold Time | $C_{load}$ = 20 pF | 6 | | | ns | 1 |
| $t_{DIS.SDO}$, SDO Output Disable Time | | | | 20 | ns | 1 |
| $t_{Fall}$, SCLK Fall Time | | | | 6.5 | ns | 2 |
| $t_{Rise}$, SCLK Rise Time | | | | 6.5 | ns | 2 |

**Table 7. SPI Timing Characteristics (10-MHz Operation)**

**Notes:**

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

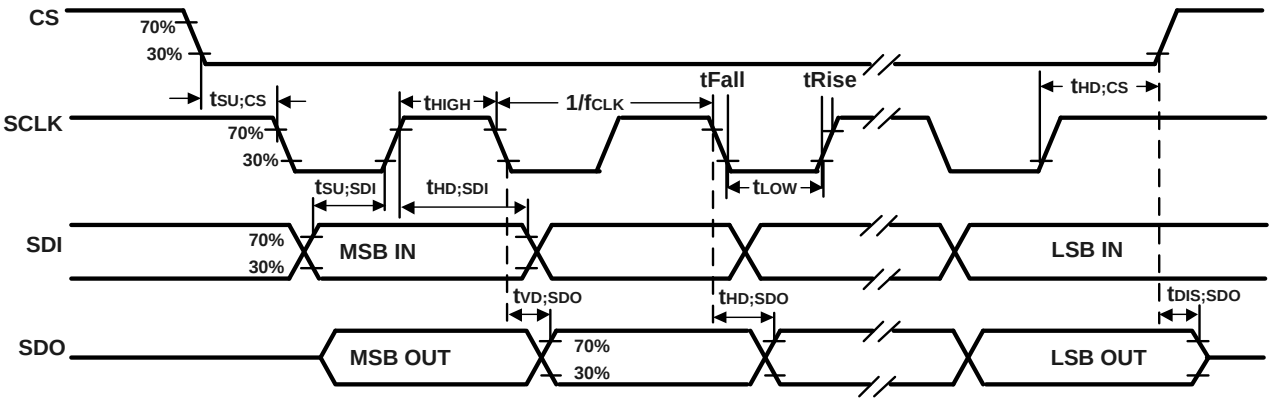


**Figure 2. 4-Wire SPI Bus Timing Diagram**



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## 3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

The following section is applicable to 3-wire SPI mode for the Auxiliary Interface.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, $T_A$=25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SPI TIMING** | | | | | | |
| $f_{SPC}$, SCLK Clock Frequency | | | | 20 | MHz | 1 |
| $t_{LOW}$, SCLK Low Period | | 30 | | | ns | 1 |
| $t_{HIGH}$, SCLK High Period | | 30 | | | ns | 1 |
| $t_{SU.CS}$, CS Setup Time | | 14.5 | | | ns | 1 |
| $t_{HD.CS}$, CS Hold Time | | 9 | | | ns | 1 |
| $t_{SU.SDIO}$, SDOI Input Setup Time | | 3.5 | | | ns | 1 |
| $t_{HD.SDIO}$, SDIO Input Hold Time | | 8.5 | | | ns | 1 |
| $t_{VD.SDIO}$, SDIO Output Valid Time | $C_{load}$ = 20 pF | | | 21 | ns | 1 |
| $t_{HD.SDIO}$, SDIO Output Hold Time | $C_{load}$ = 20 pF | 19 | | | ns | 1 |
| $t_{DIS.SDIO}$, SDIO Output Disable Time | | | | 41 | ns | 1 |
| $t_{Fall}$, SCLK Fall Time | | | | 8 | ns | 2 |
| $t_{Rise}$, SCLK Rise Time | | | | 8 | ns | 2 |

**Table 8. SPI Timing Characteristics (20-MHz Operation)**

**Notes:**

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

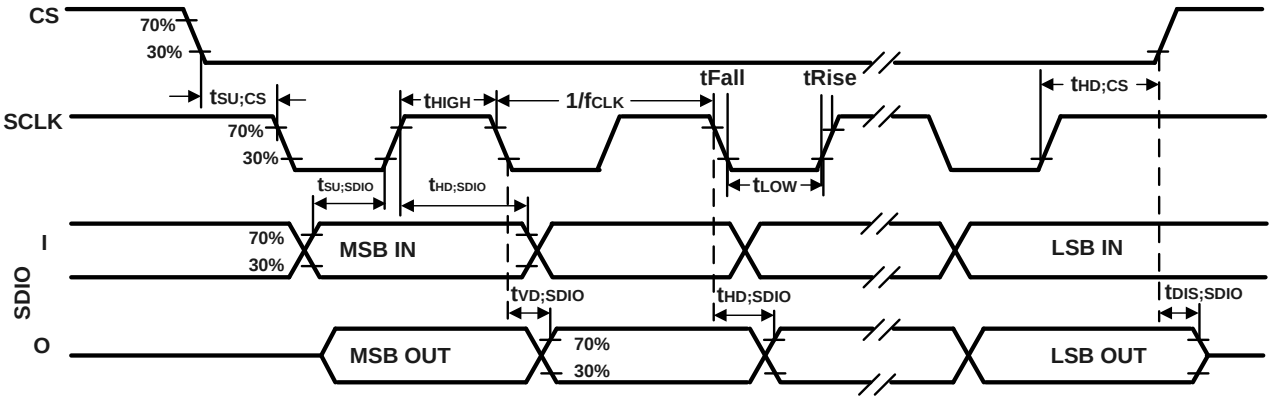


**Figure 3. 3-Wire SPI Bus Timing Diagram**



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## 3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

| Parameter | Rating |
|---|---|
| Supply Voltage, VDD | -0.5 V to +4 V |
| Supply Voltage, VDDIO | -0.5 V to +4 V |
| REGOUT | -0.5 V to 2 V |
| Input Voltage Level (AD0, FSYNC, SCL, SDA) | -0.5 V to VDDIO + 0.5 V |
| Acceleration (Any Axis, unpowered) | 20,000g for 0.2 ms |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -40°C to +125°C |
| Electrostatic Discharge (ESD) Protection | 2 kV (HBM);<br>250 V (MM) |
| Latch-up | JEDEC Class II (2),125°C<br>±100 mA |

**Table 9. Absolute Maximum Ratings**

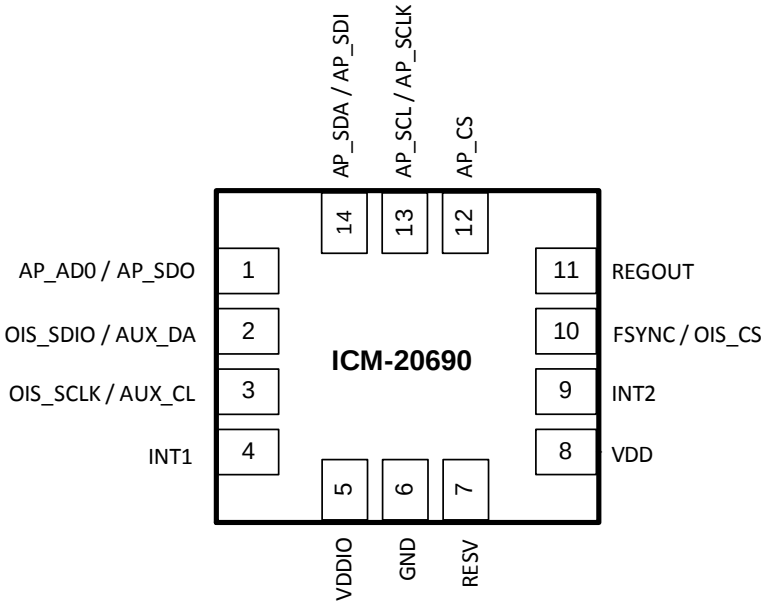
# 4 APPLICATIONS INFORMATION

## 4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

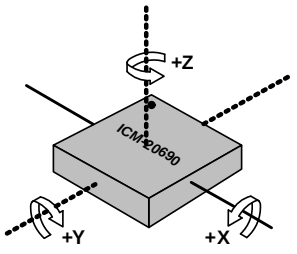
| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | AP_AD0 / AP_SDO | Application Processor (AP) Interface: AP I²C slave address LSB (AP_AD0); AP SPI serial data output (AP_SDO) |
| 2 | OIS_SDIO / AUX_DA | OIS SPI serial data IO (OIS_SDIO); I²C master serial data (AUX_DA) |
| 3 | OIS_SCLK / AUX_CL | OIS SPI serial clock (OIS_SCLK); I²C master serial clock (AUX_CL) |
| 4 | INT1 | Interrupt digital output (totem pole or open-drain) |
| 5 | VDDIO | Digital I/O supply voltage |
| 6 | GND | Power supply ground |
| 7 | RESV | Reserved, connect to ground |
| 8 | VDD | Power supply voltage |
| 9 | INT2 | Interrupt digital output (totem pole or open-drain) |
| 10 | FSYNC / OIS_CS | Frame synchronization digital input; OIS SPI chip select (OIS_CS) |
| 11 | REGOUT | Regulator filter capacitor connection |
| 12 | AP_CS | AP SPI Chip select (SPI mode only) |
| 13 | AP_SCL / AP_SCLK | AP I²C serial clock (AP_SCL); AP SPI serial clock (AP_SCLK) |
| 14 | AP_SDA / AP_SDI | AP I²C serial data (AP_SDA); AP SPI serial data input (AP_SDI) |

**Table 10. Signal Descriptions**

Note: Power up with AP_SCL / AP_SCLK and AP_CS pins held low is not a supported use case. In case this power up approach is used, software reset is required using the PWR_MGMT_1 register, prior to initialization.




**LGA Package (Top view)**




**Orientation of Axes of and Polarity of Rotation**

**Figure 4. Pin Out Diagram for ICM-20690 2.5x3.0x0.91 mm LGA**



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## 4.2 TYPICAL OPERATING CIRCUIT

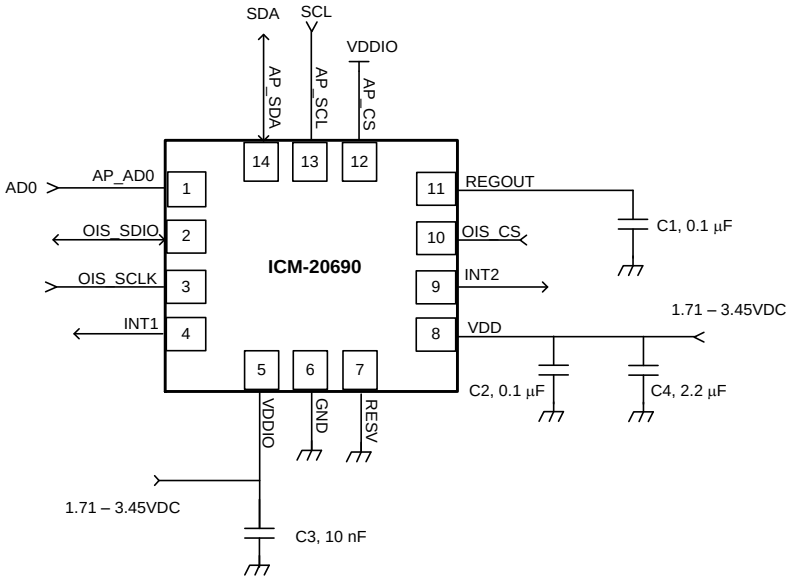


**Figure 5. ICM-20690 Application Schematic (I²C Interface to Host & OIS Operation)**

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

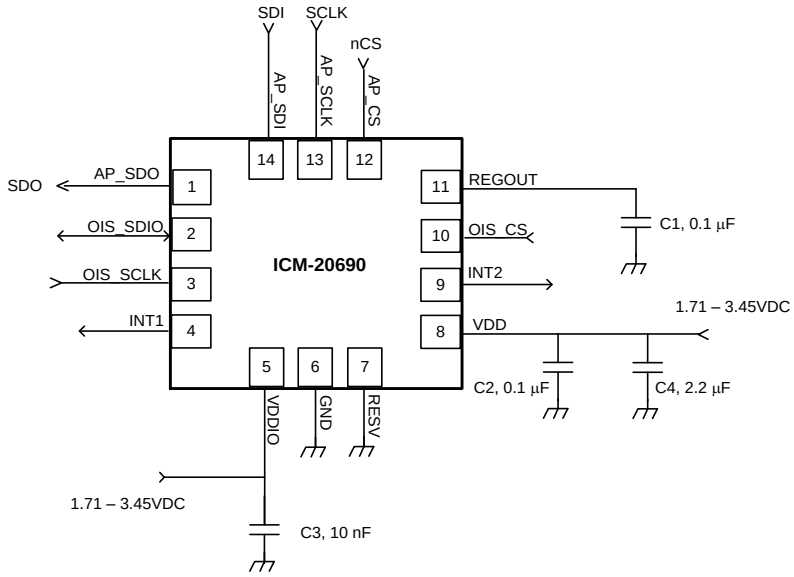


**Figure 6. ICM-20690 Application Schematic (SPI Interface to Host & OIS Operation)**



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## 4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

| Component | Label | Specification | Quantity |
|---|---|---|---|
| REGOUT Capacitor | C1 | X7R, 0.1µF ±10% | 1 |
| VDD Bypass Capacitors | C2<br>C4 | X7R, 0.1µF ±10%<br>X7R, 2.2µF ±10% | 1<br>1 |
| VDDIO Bypass Capacitor | C3 | X7R, 10nF ±10% | 1 |

**Table 11. Bill of Materials**

## 4.4 BLOCK DIAGRAM

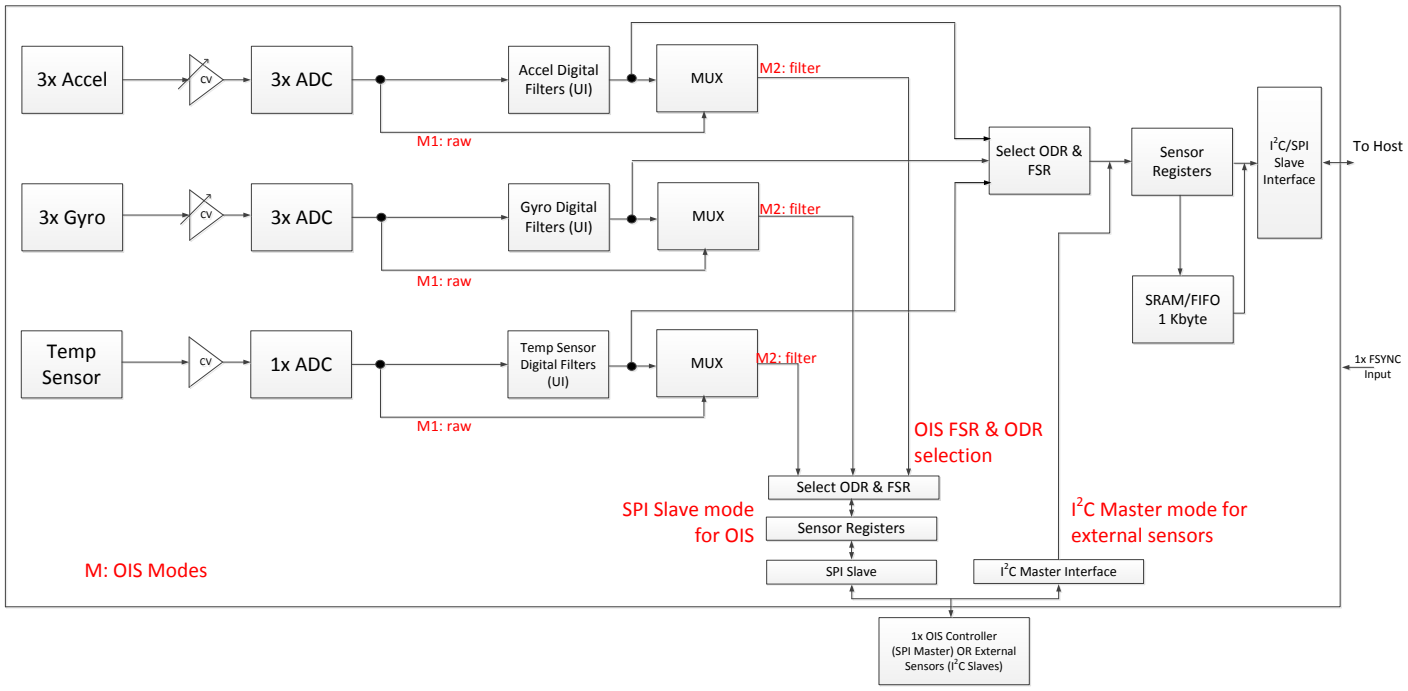


**Figure 7. ICM-20690 Block Diagram**

## 4.5 OVERVIEW

The ICM-20690 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary $I^2C$ and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

## 4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20690 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±31.25, ±62.5, ±125, ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

## 4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20690's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20690's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g* for UI mode or to ±1*g*, ±2*g*, ±4*g*, or ±8*g* for OIS mode.

## 4.8 I²C AND SPI HOST INTERFACE

The ICM-20690 communicates to the application processor using either a SPI or an I²C serial interface. The ICM-20690 always acts as a slave when communicating to the application processor. The LSB of the I²C slave address is set by pin 1 (AD0).

## 4.9 SPI OIS INTERFACE AND AUXILIARY I²C INTERFACE

The ICM-20690 has an SPI interface for communicating to OIS controllers. This interface supports 3-wire SPI. The ICM-20690 always acts as a slave when communicating to OIS controllers over this interface. The SPI interface is multiplexed with an auxiliary I²C bus that can be used for communicating to off-chip sensors. This bus has two operating modes:

I²C Master Mode: The ICM-20690 acts as a master to any external sensors connected to the auxiliary I²C bus. The ICM-20690 can directly access the data registers of external digital sensors. In this mode, the ICM-20690 directly obtains data from auxiliary sensors without intervention from the application processor. The I²C Master can be configured to read up to 12 bytes from up to 3 auxiliary sensors.

Pass-Through Mode: The ICM-20690 directly connects the primary and auxiliary I²C buses together, allowing the application processor to directly communicate with any external sensors connected to the auxiliary I²C interface. Pass-through mode is useful for configuring external sensors.

## 4.10 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.
When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.
The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

## 4.11 CLOCKING

The ICM-20690 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.



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## 4.12 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

## 4.13 FIFO

The ICM-20690 contains a 1K-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.
The ICM-20690 allows FIFO read in low-power accelerometer mode.

## 4.14 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

## 4.15 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-20690 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

## 4.16 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20690. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

## 4.17 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

## 4.18 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-20690.

| Mode | Name | Gyro | Accel |
|---|---|---|---|
| 1 | Sleep Mode | Off | Off |
| 2 | Standby Mode | Drive On | Off |
| 3 | Accelerometer Low-Power Mode | Off | Duty-Cycled |
| 4 | Accelerometer Low-Noise Mode | Off | On |
| 5 | Gyroscope Low-Power Mode | Duty-Cycled | Off |
| 6 | Gyroscope Low-Noise Mode | On | Off |
| 7 | 6-Axis Low-Noise Mode | On | On |
| 8 | 6-Axis Low-Power Mode | Duty-Cycled | On |

**Table 12. Standard Power Modes for ICM-20690**

**Notes:**

1. Power consumption for individual modes can be found in section 3.3.1.

# 5 PROGRAMMABLE INTERRUPTS

The ICM-20690 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

| Interrupt Name | Interrupt Pin |
|---|---|
| Motion Detection | INT2 |
| FIFO Overflow | INT2 |
| FIFO Watermark | INT1 |
| Data Ready | INT1 |
| FSYNC | INT2 |

**Table 13. Table of Interrupt Sources**

## 5.1 WAKE-ON-MOTION INTERRUPT

The ICM-20690 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

***Step 1: Ensure that Accelerometer is running***

- In PWR_MGMT_1 register (0x6B) set CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1

***Step 2: Accelerometer Configuration***

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 1 and A_DLPF_CFG[2:0] = 1 (b001)

***Step 3: Enable Motion Interrupt***

- In INT_ENABLE register (0x38) set WOM_X_INT_EN = WOM_Y_INT_EN = WOM_Z_INT_EN = 1 to enable motion interrupt for X, Y, and Z axis

***Step 4: Set Motion Threshold***

- Set the motion threshold for X-axis in ACCEL_WOM_X_THR register (0x20)
- Set the motion threshold for Y-axis in ACCEL_WOM_Y_THR register (0x21)
- Set the motion threshold for Z-axis in ACCEL_WOM_Z_THR register (0x22)

***Step 5: Set Interrupt Mode***

- In ACCEL_INTEL_CTRL register (0x69) clear bit 0 (WOM_TH_MODE) to select the motion interrupt as an OR of the enabled interrupts for X, Y, Z-axes and set bit 0 to make the interrupt an AND of the enabled interrupts for X, Y, Z axes)

***Step 6: Enable Accelerometer Hardware Intelligence***

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = ACCEL_INTEL_MODE = 1; Ensure that bit 0 is set to 0.

***Step 7: Set Frequency of Wake-Up***

- In register (0x19) set SMPLRT_DIV for a sample rate as indicated in the register map

***Step 8: Enable Cycle Mode (Accelerometer Low-Power Mode)***

- In PWR_MGMT_1 register (0x6B) set CYCLE = 1

# 6 DIGITAL INTERFACE

## 6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-20690 can be accessed using either I²C at 400 kHz or SPI at 10 MHz. SPI operates in four-wire mode.

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | AP_AD0 / AP_SDO | Application Processor (AP) Interface: AP I²C slave address LSB (AP_AD0); AP SPI serial data output (AP_SDO) |
| 12 | AP_CS | AP SPI Chip select (SPI mode only) |
| 13 | AP_SCL / AP_SCLK | AP I²C serial clock (AP_SCL); AP SPI serial clock (AP_SCLK) |
| 14 | AP_SDA / AP_SDI | AP I²C serial data (AP_SDA); AP SPI serial data input (AP_SDI) |

**Table 14. Serial Interface**

**Note:**
To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.
For further information regarding the *I2C_IF_DIS* bit, please refer to sections 11 and 12 of this document.

## 6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20690 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20690 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AD0. This allows two ICM-20690s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

## 6.3 I²C COMMUNICATIONS PROTOCOL

*START (S) and STOP (P) Conditions*

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

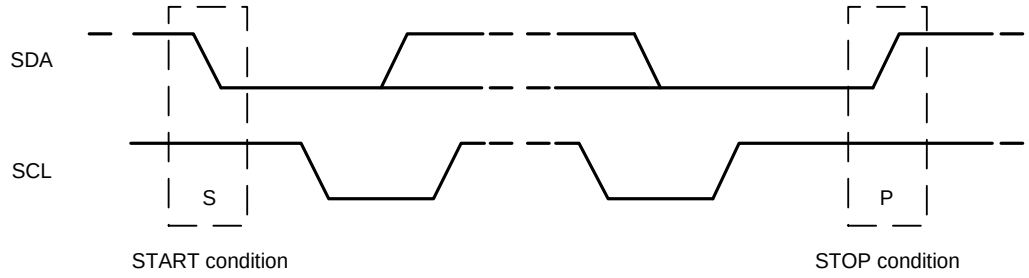


**Figure 8. START and STOP Conditions**

*Data Format / Acknowledge*

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

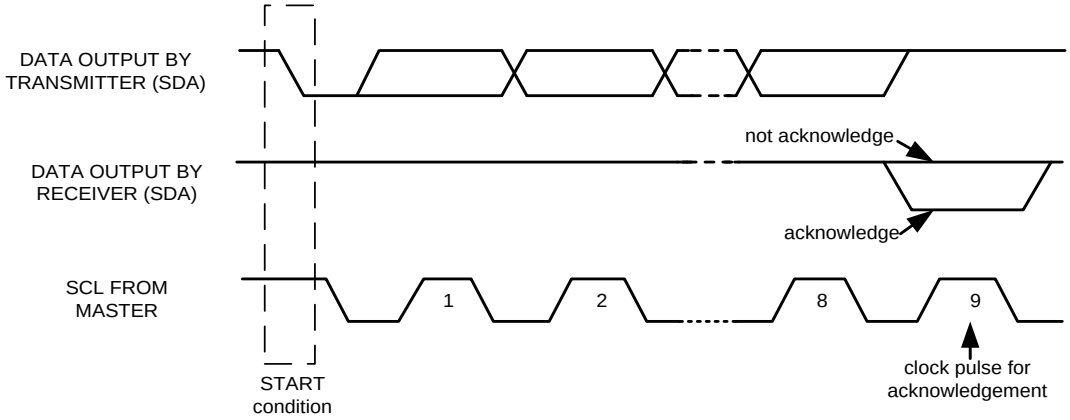


**Figure 9. Acknowledge on the I²C Bus**



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*Communications*

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

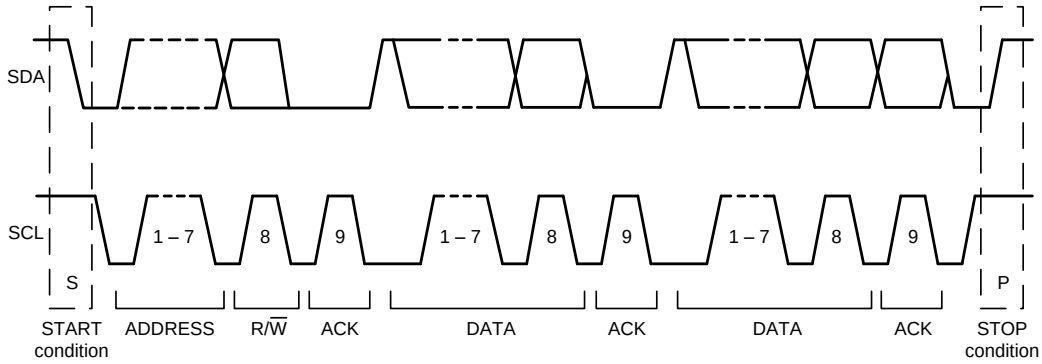


**Figure 10. Complete I²C Data Transfer**

To write the internal ICM-20690 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20690 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20690 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20690 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

*Single-Byte Write Sequence*

| Master | S | AD+W | | RA | | DATA | | P |
|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | ACK | |

*Burst Write Sequence*

| Master | S | AD+W | | RA | | DATA | | DATA | | P |
|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | ACK | | ACK | |

To read the internal ICM-20690 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20690, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20690 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

*Single-Byte Read Sequence*

| Master | S | AD+W | | RA | | S | AD+R | | | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | |

*Burst Read Sequence*

| Master | S | AD+W | | RA | | S | AD+R | | | ACK | | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|



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| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | DATA | | |

## 6.4 I²C TERMS

| Signal | Description |
|---|---|
| S | Start Condition: SDA goes from high to low while SCL is high |
| AD | Slave I²C address |
| W | Write bit (0) |
| R | Read bit (1) |
| ACK | Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle |
| NACK | Not-Acknowledge: SDA line stays high at the 9th clock cycle |
| RA | ICM-20690 internal register address |
| DATA | Transmit or received data |
| P | Stop condition: SDA going from low to high while SCL is high |

**Table 15. I²C Terms**

## 6.5 SPI INTERFACE

The ICM-20690 support 4-wire SPI for host interface and 3-wire SPI for the OIS interface. 4-wire SPI is a synchronous serial interface that uses two control lines and two data lines. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. The ICM-20690 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) for 4-wire SPI (or Serial Data IO (SDOI) for 3-wire SPI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (nCS) line from the master.

nCS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one nCS line is active at a time, ensuring that only one slave is selected at any given time. The nCS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

*SPI Operational Features*

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 10 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

*SPI Address format*

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| R/W | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

*SPI Data format*

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

6. Supports Single or Burst Read/Writes.

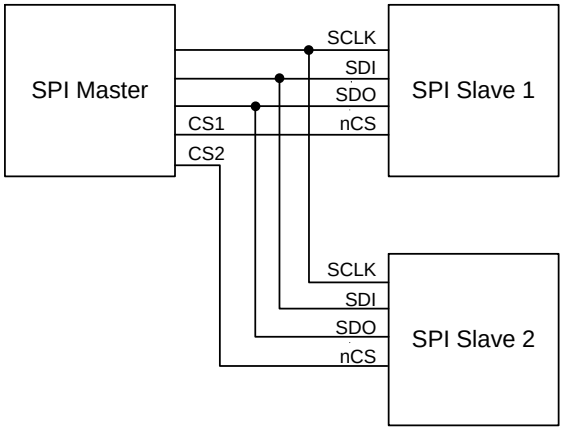


**Figure 11. Typical SPI Master/Slave Configuration**



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# 7 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

## 7.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

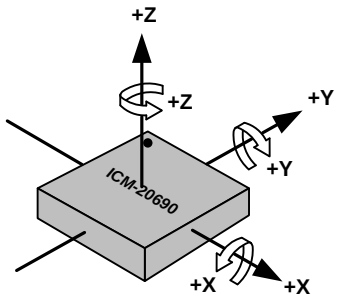


**Figure 12. Orientation of Axes of Sensitivity and Polarity of Rotation**



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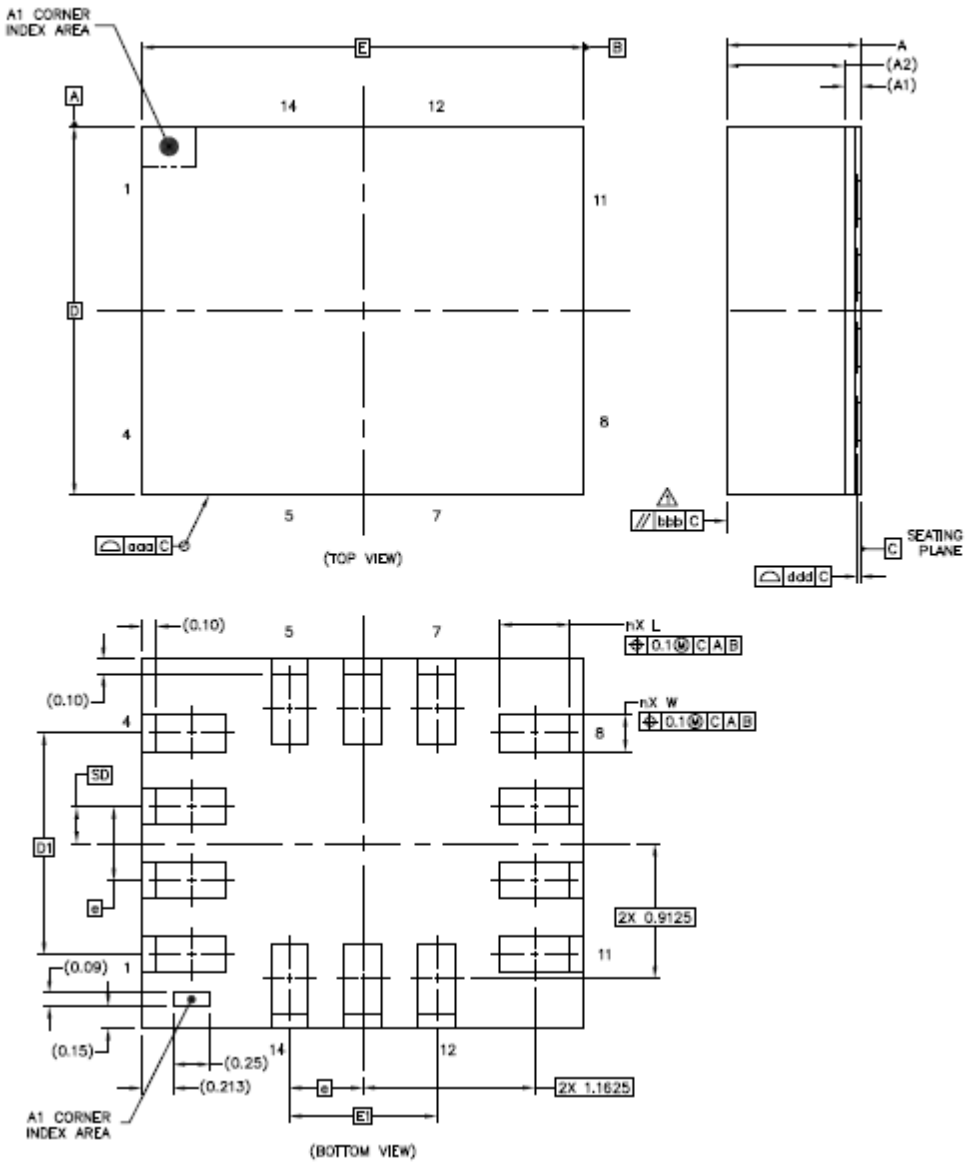
## 7.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.91) mm NiAu pad finish



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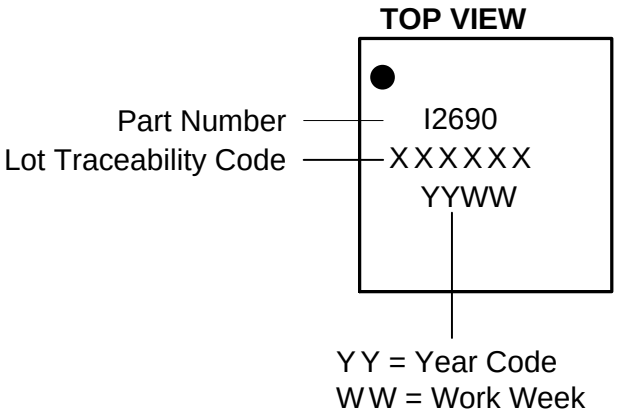
| | SYMBOLS | DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|---|
| | | MIN | NOM | MAX |
| Total Thickness | A | 0.85 | 0.91 | 0.97 |
| Substrate Thickness | A1 | | 0.105 | REF |
| Mold Thickness | A2 | | 0.8 | REF |
| Body Size | D | | 2.5 | BSC |
| | E | | 3 | BSC |
| Lead Width | W | 0.2 | 0.25 | 0.3 |
| Lead Length | L | 0.425 | 0.475 | 0.525 |
| Lead Pitch | e | | 0.5 | BSC |
| Lead Count | n | | 14 | |
| Edge Pin Center to Center | D1 | | 1.5 | BSC |
| | E1 | | 1 | BSC |
| Body Center to Contact Pin | SD | | 0.25 | BSC |
| Package Edge Tolerance | aaa | | 0.1 | |
| Mold Flatness | bbb | | 0.2 | |
| Coplanarity | ddd | | 0.08 | |

# 8 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-20690 devices is summarized below:

| Part Number | Part Number Package Marking |
|---|---|
| ICM-20690 | I2690 |



# 9 ENVIRONMENTAL COMPLIANCE

The ICM-20690 is RoHS and Green compliant.

The ICM-20690 is in full environmental compliance as evidenced in report HS-ICM-20690A, Materials Declaration Data Sheet.

**Environmental Declaration Disclaimer:**

InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

# 10 USE NOTES

## 10.1 VALID COMBINATIONS OF UI AND OIS DATAPATH SETTINGS

When the device is being used with UI and OIS datapaths active, certain combinations of settings are valid and others are invalid. These are summarized in the tables below. The device is in low-noise mode for these configurations.

**Gyroscope Configurations:**

| | UI Mode | | | | | | |
|---|---|---|---|---|---|---|---|
| | **Filter Settings** | | FCHOICE_B = 01 | FCHOICE_B = 10 | FCHOICE_B = 00; DLPFCFG = 7 | FCHOICE_B = 00; DLPFCFG = 0 | FCHOICE_B = 00; DLPFCFG = 1 to 6 |
| | | **ODR** | 32kHz | 32kHz | 8kHz | 8kHz | ≤1kHz |
| **OIS Mode** | FCHOICE_OIS_B = 11 | 32kHz | Valid | Valid | Valid | Valid | Valid |
| | FCHOICE_OIS_B = 10; FCHOICE_B = 10 | 32kHz | Invalid | Valid | Invalid | Invalid | Invalid |
| | FCHOICE_OIS_B = 10; FCHOICE_B = 00 | 8kHz | Invalid | Invalid | Valid | Valid | Valid |
| | FCHOICE_OIS_B = 01; FCHOICE_B = 00 | 8kHz | Invalid | Invalid | Valid | Valid | Valid |
| | FCHOICE_OIS_B = 01; FCHOICE_B = 00; DLPF_CFG = 1 to 6 | ≤1kHz | Invalid | Invalid | Invalid | Invalid | Valid |

**Accelerometer Configurations:**

| | UI Mode | | | | |
|---|---|---|---|---|---|
| | **Filter Settings** | | ACCEL_FCHOICE_B = 1 | ACCEL_FCHOICE_B = 0; A_DLPF_CFG = 7 | ACCEL_FCHOICE_B = 0; A_DLPF_CFG = 0 to 6 |
| | | **ODR** | 4kHz | ≤1kHz | ≤1kHz |
| **OIS Mode** | ACCEL_FCHOICE_OIS_B = 11 | 4kHz | Valid | Valid | Valid |
| | ACCEL_FCHOICE_OIS_B = 10; ACCEL_FCHOICE_B = 0 | ≤1kHz | Invalid | Valid | Valid |
| | ACCEL_FCHOICE_OIS_B = 01; ACCEL_FCHOICE_B = 0; A_DLPF_CFG = 0 to 6 | ≤1kHz | Invalid | Invalid | Valid |

## 10.2 FIFO WATERMARK THRESHOLD

FIFO watermark threshold, FIFO_WM_TH, is limited to 8 bits but the FIFO size is 1Kbytes. This limits the use of FIFO watermark to 256 out of a possible 1024 bytes.

## 10.3 FIFO WATERMARK INTERRUPT

For FIFO watermark interrupt, FIFO_WM_INT, to receive future interrupts after a first interrupt, the host must clear the status register with a read.

## 10.4 ACCELEROMETER-ONLY LOW-NOISE MODE

The first output sample in Accelerometer-Only Low-Noise Mode after wake up from sleep always has 1 ms delay, independent of ODR.

### 10.5 ACCELEROMETER LOW-POWER MODE

Changing the value of SMPLRT_DIV register in Accelerometer Low-Power mode will take effect after up to one sample at the old ODR.

### 10.6 SENSOR MODE CHANGE

When switching from low-power modes to low-noise modes, unsettled output samples may be observed at the gyroscope or accelerometer outputs due to filter switching and settling. The number of unsettled output samples depends on the filter and ODR settings. The number of unsettled output samples is minimized by selecting the widest low-noise-mode filter bandwidth consistent with the chosen ODR.

### 10.7 TEMP SENSOR DURING GYROSCOPE STANDBY MODE

During transition from Gyro Low power mode (GYRO_CYCLE=1), to Gyro Standby mode, in addition to the Gyro axis (axes) being turned off, the Temp Sensor will also be turned off if the Accel is disabled. In order to keep the temp sensor on during Gyroscope standby mode when Accel is disabled, the following procedure should be followed:

- Set GYRO_CYCLE = 0 at least one ODR cycle prior to entering Standby mode
- At least one of the Gyro axis is ON prior to entering Standby mode
- Set GYRO_STANDBY = 1

### 10.8 GYROSCOPE MODE CHANGE

Gyroscope will take one ODR clock period to switch from Low-Noise to Low-Power mode after GYRO_CYCLE bit is set.
If GYRO_CYCLE is set to 1 prior to turning on the gyroscope, the first sample will be from low-noise mode, which may not be a settled value. It is therefore recommended to ignore the first reading in this case.

### 10.9 POWER MANAGEMENT 1 REGISTER SETTING

It is required to set CLKSEL[2:0] to 001 (auto-select) for full performance.

### 10.10 UNLISTED REGISTER LOCATIONS

Do not read unlisted register locations in Sleep mode as this may cause the device to hang up, requiring power cycle to restore operation.

### 10.11 CLOCK TRANSITION WHEN GYROSCOPE IS TURNED OFF

When the gyroscope is on, the on-chip master clock source will be the gyroscope clock (assuming CLKSEL[2:0] = 001 for auto-select mode); otherwise, the master clock source will be the internal oscillator as long as the part is not in Sleep mode. During a power mode transition, whenever the gyroscope is disabled and the part enters a mode other than Sleep, the on-chip master clock source will transition from the gyroscope clock to the internal oscillator. It will take about 20 μs for this transition to complete.

### 10.12 SLEEP MODE

The part will only enter Sleep mode when the SLEEP bit in PWR_MGMT_2 is set to '1'. If SLEEP bit is '0' and bit STBY_[X,Y,Z]A and STBY_[X,Y,Z]G are all set to '1', accelerometer and gyroscope will be turned off, but the on-chip master clock will still be running and consuming power.

### 10.13 NO SPECIAL OPERATION NEEDED FOR FIFO READ IN LOW POWER MODE

The use of FIFO is enabled in all modes including low power mode.

### 10.14 GYROSCOPE STANDBY PROCEDURE

The follow precaution and procedure must be followed while using the Gyroscope Standby mode:
Precaution to follow while entering Standby Mode:

- The user will ensure that at least one gyro axis is ON when setting gyro_standby = 1.

Procedure to transition from Gyro Standby to Gyro off:

- The user should set gyro_standby = 0 first
- Next, turn off gyro x/y/z.

# 11 REGISTER MAP

The following table lists the register map for the ICM-20690. Note that all registers are accessible in all modes of device operation.

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 00 | SELF_TEST_X_GYRO | READ/ WRITE | XG_ST_DATA[7:0] | | | | | | | |
| 01 | 01 | SELF_TEST_Y_GYRO | READ/ WRITE | YG_ST_DATA[7:0] | | | | | | | |
| 02 | 02 | SELF_TEST_Z_GYRO | READ/ WRITE | ZG_ST_DATA[7:0] | | | | | | | |
| 0D | 13 | SELF_TEST_X_ACCEL | READ/ WRITE | XA_ST_DATA[7:0] | | | | | | | |
| 0E | 14 | SELF_TEST_Y_ACCEL | READ/ WRITE | YA_ST_DATA[7:0] | | | | | | | |
| 0F | 15 | SELF_TEST_Z_ACCEL | READ/ WRITE | ZA_ST_DATA[7:0] | | | | | | | |
| 13 | 19 | XG_OFFS_USRH | READ/ WRITE | X_OFFS_USR [15:8] | | | | | | | |
| 14 | 20 | XG_OFFS_USRL | READ/ WRITE | X_OFFS_USR [7:0] | | | | | | | |
| 15 | 21 | YG_OFFS_USRH | READ/ WRITE | Y_OFFS_USR [15:8] | | | | | | | |
| 16 | 22 | YG_OFFS_USRL | READ/ WRITE | Y_OFFS_USR [7:0] | | | | | | | |
| 17 | 23 | ZG_OFFS_USRH | READ/ WRITE | Z_OFFS_USR [15:8] | | | | | | | |
| 18 | 24 | ZG_OFFS_USRL | READ/ WRITE | Z_OFFS_USR [7:0] | | | | | | | |
| 19 | 25 | SMPLRT_DIV | READ/ WRITE | SMPLRT_DIV[7:0] | | | | | | | |
| 1A | 26 | CONFIG | READ/ WRITE | - | FIFO_ MODE | EXT_SYNC_SET[2:0] | | | DLPF_CFG[2:0] | | |
| 1B | 27 | GYRO_CONFIG | READ/ WRITE | XG_ST | YG_ST | ZG_ST | FS_SEL [2:0] | | | FCHOICE_B[1:0] | |
| 1C | 28 | ACCEL_CONFIG | READ/ WRITE | XA_ST | YA_ST | ZA_ST | AFS_SEL[1:0] | | - | AFS_SEL_OIS[1:0] | |
| 1D | 29 | ACCEL_CONFIG 2 | READ/ WRITE | FIFO_SIZE | | DEC2_CFG | | ACCEL_FC HOICE_B | A_DLPF_CFG | | |
| 1E | 30 | LP_MODE_CONFIG | READ/ WRITE | GYRO_CYCL E | GYRO_AVGCFG[2:0] | | | - | | | |
| 20 | 32 | ACCEL_WOM_X_THR | READ/ WRITE | WOM_X_TH[7:0] | | | | | | | |
| 21 | 33 | ACCEL_WOM_Y_THR | READ/ WRITE | WOM_Y_TH[7:0] | | | | | | | |
| 22 | 34 | ACCEL_WOM_Z_THR | READ/ WRITE | WOM_Z_TH[7:0] | | | | | | | |
| 23 | 35 | FIFO_EN | READ/ WRITE | TEMP_OUT | GYRO_XOUT | GYRO_YOUT | GYRO_ZOUT | ACCEL_XY Z_OUT | - | | |
| 24 | 36 | I2C_MST_CTRL | READ/ WRITE | MULT_MST _EN | - | | I2C_MST_P_N SR | I2C_MST_CLK[3:0] | | | |
| 25 | 37 | I2C_SLV0_ADDR | READ/ WRITE | I2C_SLV0_R NW | I2C_ID_0[6:0] | | | | | | |
| 26 | 38 | I2C_SLV0_REG | READ/ WRITE | I2C_SLV0_REG[7:0] | | | | | | | |
| 27 | 39 | I2C_SLV0_CTRL | READ/ WRITE | I2C_SLV0_E N | I2C_SLV0_BY TE_SW | I2C_SLV0_RE G_DIS | I2C_SLV0_GR P | I2C_SLV0_LENG[3:0] | | | |
| 28 | 40 | I2C_SLV1_ADDR | READ/ WRITE | I2C_SLV1_R NW | I2C_ID_1[6:0] | | | | | | |
| 29 | 41 | I2C_SLV1_REG | READ/ WRITE | I2C_SLV1_REG[7:0] | | | | | | | |
| 2A | 42 | I2C_SLV1_CTRL | READ/ WRITE | I2C_SLV1_E N | I2C_SLV1_BY TE_SW | I2C_SLV1_RE G_DIS | I2C_SLV1_GR P | I2C_SLV1_LENG[3:0] | | | |
| 2B | 43 | I2C_SLV2_ADDR | READ/ WRITE | I2C_SLV2_R NW | I2C_ID_2[6:0] | | | | | | |



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| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2C | 44 | I2C_SLV2_REG | READ/ WRITE | I2C_SLV2_REG[7:0] | | | | | | | |
| 2D | 45 | I2C_SLV2_CTRL | READ/ WRITE | I2C_SLV2_EN | I2C_SLV2_BYTE_SW | I2C_SLV2_REG_DIS | I2C_SLV2_GRP | I2C_SLV2_LENG[3:0] | | | |
| 2E | 46 | ODR_DELAY_EN | READ/ WRITE | ODR_DELAY_EN | - | | | | | | |
| 36 | 54 | FSYNC_INT | READ to CLEAR | FSYNC_INT | - | | | | | | |
| 37 | 55 | INT_PIN_CFG | READ/ WRITE | INT_LEVEL | INT_OPEN | LATCH_INT_EN | INT_RD_CLEAR | FSYNC_INT_LEVEL | FSYNC_INT_MODE_EN | - | |
| 38 | 56 | INT_ENABLE | READ/ WRITE | WOM_X_INT_EN | WOM_Y_INT_EN | WOM_Z_INT_EN | FIFO_OFLOW_EN | - | GDRIVE_INT_EN | - | DATA_RDY_INT_EN |
| 39 | 57 | FIFO_WM_INT_STATUS | READ to CLEAR | - | FIFO_WM_INT | - | | | | | |
| 3A | 58 | INT_STATUS | READ to CLEAR | WOM_X_INT | WOM_Y_INT | WOM_Z_INT | FIFO_OFLOW_INT | - | GDRIVE_INT | - | DATA_RDY_INT |
| 3B | 59 | ACCEL_XOUT_H | READ | ACCEL_XOUT[15:8] | | | | | | | |
| 3C | 60 | ACCEL_XOUT_L | READ | ACCEL_XOUT[7:0] | | | | | | | |
| 3D | 61 | ACCEL_YOUT_H | READ | ACCEL_YOUT[15:8] | | | | | | | |
| 3E | 62 | ACCEL_YOUT_L | READ | ACCEL_YOUT[7:0] | | | | | | | |
| 3F | 63 | ACCEL_ZOUT_H | READ | ACCEL_ZOUT[15:8] | | | | | | | |
| 40 | 64 | ACCEL_ZOUT_L | READ | ACCEL_ZOUT[7:0] | | | | | | | |
| 41 | 65 | TEMP_OUT_H | READ | TEMP_OUT[15:8] | | | | | | | |
| 42 | 66 | TEMP_OUT_L | READ | TEMP_OUT[7:0] | | | | | | | |
| 43 | 67 | GYRO_XOUT_H | READ | GYRO_XOUT[15:8] | | | | | | | |
| 44 | 68 | GYRO_XOUT_L | READ | GYRO_XOUT[7:0] | | | | | | | |
| 45 | 69 | GYRO_YOUT_H | READ | GYRO_YOUT[15:8] | | | | | | | |
| 46 | 70 | GYRO_YOUT_L | READ | GYRO_YOUT[7:0] | | | | | | | |
| 47 | 71 | GYRO_ZOUT_H | READ | GYRO_ZOUT[15:8] | | | | | | | |
| 48 | 72 | GYRO_ZOUT_L | READ | GYRO_ZOUT[7:0] | | | | | | | |
| 49 | 73 | EXT_SLV_SENS_DATA_00 | READ | EXT_SLV_SENS_DATA_00[7:0] | | | | | | | |
| 4A | 74 | EXT_SLV_SENS_DATA_01 | READ | EXT_SLV_SENS_DATA_01[7:0] | | | | | | | |
| 4B | 75 | EXT_SLV_SENS_DATA_02 | READ | EXT_SLV_SENS_DATA_02[7:0] | | | | | | | |
| 4C | 76 | EXT_SLV_SENS_DATA_03 | READ | EXT_SLV_SENS_DATA_03[7:0] | | | | | | | |
| 4D | 77 | EXT_SLV_SENS_DATA_04 | READ | EXT_SLV_SENS_DATA_04[7:0] | | | | | | | |
| 4E | 78 | EXT_SLV_SENS_DATA_05 | READ | EXT_SLV_SENS_DATA_05[7:0] | | | | | | | |
| 4F | 79 | EXT_SLV_SENS_DATA_06 | READ | EXT_SLV_SENS_DATA_06[7:0] | | | | | | | |
| 50 | 80 | EXT_SLV_SENS_DATA_07 | READ | EXT_SLV_SENS_DATA_07[7:0] | | | | | | | |
| 51 | 81 | EXT_SLV_SENS_DATA_08 | READ | EXT_SLV_SENS_DATA_08[7:0] | | | | | | | |
| 52 | 82 | EXT_SLV_SENS_DATA_09 | READ | EXT_SLV_SENS_DATA_09[7:0] | | | | | | | |
| 53 | 83 | EXT_SLV_SENS_DATA_10 | READ | EXT_SLV_SENS_DATA_10[7:0] | | | | | | | |
| 54 | 84 | EXT_SLV_SENS_DATA_11 | READ | EXT_SLV_SENS_DATA_11[7:0] | | | | | | | |
| 5F | 95 | ODR_DLY_CNT_HI | READ/ WRITE | ODR_DLY_CNT[15:8] | | | | | | | |
| 60 | 96 | ODR_DLY_CNT_LO | READ/ WRITE | ODR_DLY_CNT[7:0] | | | | | | | |
| 61 | 97 | FIFO_WM_TH | READ/ WRITE | FIFO_WM_TH[7:0] | | | | | | | |
| 63 | 99 | I2C_SLV0_DO | READ/ WRITE | I2C_SLV0_DO[7:0] | | | | | | | |
| 64 | 100 | I2C_SLV1_DO | READ/ WRITE | I2C_SLV1_DO[7:0] | | | | | | | |
| 65 | 101 | I2C_SLV2_DO | READ/ WRITE | I2C_SLV2_DO[7:0] | | | | | | | |
| 67 | 103 | I2C_MST_DELAY_CTRL | READ/ WRITE | DELAY_ES_SHADOW | - | | | | I2C_SLV2_DELAY_EN | I2C_SLV1_DELAY_EN | I2C_SLV0_DELAY_EN |
| 68 | 104 | SIGNAL_PATH_RESET | READ/ WRITE | FS_SEL_OIS[2:0] | | | FCHOICE_OIS_B[1:0] | | GYRO_RST | ACCEL_RST | TEMP_RST |



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| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 69 | 105 | ACCEL_INTEL_CTRL | READ/ WRITE | ACCEL_INTEL_EN | ACCEL_INTEL_MODE | ACCEL_FCHOICE_OIS_B | | - | | | WOM_INT_MODE |
| 6A | 106 | USER_CTRL | READ/ WRITE | - | FIFO_EN | I2C_MST_EN | I2C_IF_DIS | | FIFO_RST | I2C_MST_RST | SIG_COND_RST |
| 6B | 107 | PWR_MGMT_1 | READ/ WRITE | DEVICE_RESET | SLEEP | CYCLE | GYRO_STANDBY | TEMP_DIS | CLKSEL[2:0] | | |
| 6C | 108 | PWR_MGMT_2 | READ/ WRITE | LP_DIS | - | STBY_XA | STBY_YA | STBY_ZA | STBY_XG | STBY_YG | STBY_ZG |
| 70 | 112 | OIS_ENABLE | READ/ WRITE | - | | | | | | OIS_ENABLE | - |
| 72 | 114 | FIFO_COUNTH | READ | FIFO_COUNT[15:8] | | | | | | | |
| 73 | 115 | FIFO_COUNTL | READ | FIFO_COUNT[7:0] | | | | | | | |
| 74 | 116 | FIFO_R_W | READ/ WRITE | FIFO_DATA[7:0] | | | | | | | |
| 75 | 117 | WHO_AM_I | READ | WHOAMI[7:0] | | | | | | | |
| 77 | 119 | XA_OFFSET_H | READ/ WRITE | XA_OFFS[14:7] | | | | | | | |
| 78 | 120 | XA_OFFSET_L | READ/ WRITE | XA_OFFS[6:0] | | | | | | | - |
| 7A | 122 | YA_OFFSET_H | READ/ WRITE | YA_OFFS[14:7] | | | | | | | |
| 7B | 123 | YA_OFFSET_L | READ/ WRITE | YA_OFFS[6:0] | | | | | | | - |
| 7D | 125 | ZA_OFFSET_H | READ/ WRITE | ZA_OFFS[14:7] | | | | | | | |
| 7E | 126 | ZA_OFFSET_L | READ/ WRITE | ZA_OFFS[6:0] | | | | | | | - |

**Table 16. ICM-20690 Register Map**

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

The reset value is 0x00 for all registers other than the registers below; also, the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Registers 00 – 02: Trim values
- Registers 13 – 15: Trim values
- Register 105 ACCEL_INTEL_CTRL value: 0x10
- Register 107 Power Management 1 value: 0x41
- Register 117 WHO_AM_I value: 0x20
- Registers 119, 120, 122, 123, 125, 126: Trim values

## 11.1 REGISTERS SPECIFIC TO SECONDARY INTERFACE IN OIS MODE

The following registers are accessible from the secondary interface in OIS mode only. OIS controller should only read this data in SPI burst mode to avoid OIS sensor data update during reading. SPI single byte read mode should not be used.

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 00 | ACCEL_XOUT_OIS_H | READ | ACCEL_XOUT_OIS[15:8] | | | | | | | |
| 01 | 01 | ACCEL_XOUT_OIS_L | READ | ACCEL_XOUT_OIS[7:0] | | | | | | | |
| 02 | 02 | ACCEL_YOUT_OIS_H | READ | ACCEL_YOUT_OIS[15:8] | | | | | | | |
| 03 | 03 | ACCEL_YOUT_OIS_L | READ | ACCEL_YOUT_OIS[7:0] | | | | | | | |
| 04 | 04 | ACCEL_ZOUT_OIS_H | READ | ACCEL_ZOUT_OIS[15:8] | | | | | | | |
| 05 | 05 | ACCEL_ZOUT_OIS_L | READ | ACCEL_ZOUT_OIS[7:0] | | | | | | | |
| 06 | 06 | TEMP_OUT_OIS_H | READ | TEMP_OUT_OIS[15:8] | | | | | | | |
| 07 | 07 | TEMP_OUT_OIS_L | READ | TEMP_OUT_OIS[7:0] | | | | | | | |
| 08 | 08 | GYRO_XOUT_OIS_H | READ | GYRO_XOUT_OIS[15:8] | | | | | | | |
| 09 | 09 | GYRO_XOUT_OIS_L | READ | GYRO_XOUT_OIS[7:0] | | | | | | | |
| 0A | 10 | GYRO_YOUT_OIS_H | READ | GYRO_YOUT_OIS[15:8] | | | | | | | |
| 0B | 11 | GYRO_YOUT_OIS_L | READ | GYRO_YOUT_OIS[7:0] | | | | | | | |
| 0C | 12 | GYRO_ZOUT_OIS_H | READ | GYRO_ZOUT_OIS[15:8] | | | | | | | |
| 0D | 13 | GYRO_ZOUT_OIS_L | READ | GYRO_ZOUT_OIS[7:0] | | | | | | | |

**Table 17. Registers Specific to Secondary Interface in OIS Mode**



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# 12 REGISTER DESCRIPTIONS

This section describes the function and contents of the registers within the ICM-20690.

Note: The device powers up in Sleep Mode.

## 12.1 REGISTERS 0 TO 2 – GYROSCOPE SELF-TEST REGISTERS

**Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO**
**Register Type: READ/WRITE**
**Register Address: 00, 01, 02 (Decimal); 00, 01, 02 (Hex)**

| REGISTER | BIT | NAME | FUNCTION |
|---|---|---|---|
| SELF_TEST_X_GYRO | [7:0] | XG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Y_GYRO | [7:0] | YG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Z_GYRO | [7:0] | ZG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$



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## 12.2 REGISTERS 13 TO 15 – ACCELEROMETER SELF-TEST REGISTERS

**Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL**
**Register Type: READ/WRITE**
**Register Address: 13, 14, 15 (Decimal); 0D, OE, OF (Hex)**

| REGISTER | BITS | NAME | FUNCTION |
|---|---|---|---|
| SELF_TEST_X_ACCEL | [7:0] | XA_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Y_ACCEL | [7:0] | YA_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Z_ACCEL | [7:0] | ZA_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}) + 1$$

## 12.3 REGISTER 19 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: XG_OFFS_USRH**
**Register Type: READ/WRITE**
**Register Address: 19 (Decimal); 13 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | X_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 12.4 REGISTER 20 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: XG_OFFS_USRL**
**Register Type: READ/WRITE**
**Register Address: 20 (Decimal); 14 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | X_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |



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## 12.5 REGISTERS 21 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: YG_OFFS_USRH**
**Register Type: READ/WRITE**
**Register Address: 21 (Decimal); 15 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | Y_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 12.6 REGISTERS 22 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: YG_OFFS_USRL**
**Register Type: READ/WRITE**
**Register Address: 22 (Decimal); 16 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | Y_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 12.7 REGISTERS 23 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: ZG_OFFS_USRH**
**Register Type: READ/WRITE**
**Register Address: 23 (Decimal); 17 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | Z_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 12.8 REGISTER 24 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: ZG_OFFS_USRL**
**Register Type: READ/WRITE**
**Register Address: 24 (Decimal); 18 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| **[7:0]** | Z_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 12.9 REGISTER 25 – SAMPLE RATE DIVIDER

**Register Name: SMPLRT_DIV**
**Register Type: READ/WRITE**
**Register Address: 25 (Decimal); 19 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | SMPLRT_DIV[7:0] | Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate.<br>NOTE: This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7).<br>This is the update rate of the sensor register:<br>SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV)<br>Where INTERNAL_SAMPLE_RATE = 1kHz<br><br>SMPLRT_DIV values of 0 and 1 are not supported in low-power mode. |

## 12.10 REGISTER 26 – CONFIGURATION

**Register Name: CONFIG**
**Register Type: READ/WRITE**
**Register Address: 26 (Decimal); 1A (Hex)**

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>[7]</td><td>-</td><td>Default configuration value is 1. User should set it to 0.</td></tr>
<tr><td>[6]</td><td>FIFO_MODE</td><td>When set to '1', when the FIFO is full, additional writes will not be written to FIFO.<br>When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.</td></tr>
<tr><td>[5:3]</td><td>EXT_SYNC_SET[2:0]</td><td>Enables the FSYNC pin data to be sampled.<br><br><table><tr><th>EXT_SYNC_SET</th><th>FSYNC bit location</th></tr><tr><td>0</td><td>function disabled</td></tr><tr><td>1</td><td>TEMP_OUT_L[0]</td></tr><tr><td>2</td><td>GYRO_XOUT_L[0]</td></tr><tr><td>3</td><td>GYRO_YOUT_L[0]</td></tr><tr><td>4</td><td>GYRO_ZOUT_L[0]</td></tr><tr><td>5</td><td>ACCEL_XOUT_L[0]</td></tr><tr><td>6</td><td>ACCEL_YOUT_L[0]</td></tr><tr><td>7</td><td>ACCEL_ZOUT_L[0]</td></tr></table><br>FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.</td></tr>
<tr><td>[2:0]</td><td>DLPF_CFG[2:0]</td><td>For the DLPF to be used, FCHOICE_B[1:0] is 2'b00.<br>See the tables below.</td></tr>
</table>

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.



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UI path gyroscope DLPF configuration:

| FCHOICE_B | | DLPF_CFG | Filter BW (Hz) | Filter Delay (ms) | ODR (kHz) |
|---|---|---|---|---|---|
| <1> | <0> | | | | |
| X | 1 | X | 8800 | 0.064 | 32 |
| 1 | 0 | X | 3600 | 0.11 | 32 |
| 0 | 0 | 0 | 250 | 0.97 | 8 |
| 0 | 0 | 1 | 184 | 2.9 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 2 | 92 | 3.9 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 3 | 41 | 5.9 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 4 | 20 | 9.9 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 5 | 10 | 17.85 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 6 | 5 | 33.48 | 1/(1+SMPLRT_DIV) |
| 0 | 0 | 7 | 3600 | 0.17 | 8 |

Temperature sensor DLPF configuration:

| DLPF_CFG | Filter BW (Hz) | Filter Delay (ms) |
|---|---|---|
| 0 | NA | NA |
| 1 | 188 | 1.9 |
| 2 | 98 | 2.8 |
| 3 | 42 | 4.8 |
| 4 | 20 | 8.3 |
| 5 | 10 | 13.4 |
| 6 | 5 | 18.6 |
| 7 | NA | NA |

## 12.11 REGISTER 27 – GYROSCOPE CONFIGURATION

**Register Name: GYRO_CONFIG**
**Register Type: READ/WRITE**
**Register Address: 27 (Decimal); 1B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | XG_ST | 1: Enable X Gyro self-test |
| [6] | YG_ST | 1: Enable Y Gyro self-test |
| [5] | ZG_ST | 1: Enable Z Gyro self-test |
| [4:2] | FS_SEL[2:0] | UI Path Gyro Full Scale Select:<br>000 = ±250dps<br>001= ±500dps<br>010 = ±1000dps<br>011 = ±2000dps<br>101= ±31.25dps<br>110 = ±62.5dps<br>111 = ±125dps |
| [1:0] | FCHOICE_B[1:0] | Used to bypass DLPF as shown in table above |



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## 12.12 REGISTER 28 – ACCELEROMETER CONFIGURATION

**Register Name: ACCEL_CONFIG**
**Register Type: READ/WRITE**
**Register Address: 28 (Decimal); 1C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | XA_ST | 1: Enable X Accel self-test |
| [6] | YA_ST | 1: Enable Y Accel self-test |
| [5] | ZA_ST | 1: Enable Z Accel self-test |
| [4:3] | AFS_SEL[1:0] | UI Path Accel Full Scale Select:<br>00 = ±2g<br>01 = ±4g<br>10 = ±8g<br>11 = ±16g |
| [2] | - | Reserved |
| [1:0] | AFS_SEL_OIS[1:0] | OIS Path Accel Full Scale Select:<br>00 = ±2g<br>01= ±4g<br>10 = ±8g<br>11 = ±1g |

## 12.13 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

**Register Name: ACCEL_CONFIG2**
**Register Type: READ/WRITE**
**Register Address: 29 (Decimal); 1D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:6] | FIFO_SIZE | Controls FIFO size as follows:<br><br>00 = 128bytes<br>01 = 256 bytes<br>10 = 512 bytes<br>11 = 1024 bytes |
| [5:4] | DEC2_CFG[1:0] | Averaging filter settings for Low Power Accelerometer mode as explained in the second table below |
| [3] | ACCEL_FCHOICE_B | Used to bypass DLPF as shown in the table below |
| [2:0] | A_DLPF_CFG | UI path accelerometer low pass filter setting as shown in the table below |

| ACCEL_FCHOICE_B | A_DLPF_CFG | Filter BW (Hz) | Filter Delay (ms) | ODR (kHz) |
|---|---|---|---|---|
| 1 | X | 1046.00 | 0.50 | 4 |
| 0 | 0 | 218.10 | 1.88 | 1/(1+SMPLRT_DIV) |
| 0 | 1 | 218.10 | 1.88 | 1/(1+SMPLRT_DIV) |
| 0 | 2 | 99.00 | 2.88 | 1/(1+SMPLRT_DIV) |
| 0 | 3 | 44.80 | 4.88 | 1/(1+SMPLRT_DIV) |
| 0 | 4 | 21.20 | 8.87 | 1/(1+SMPLRT_DIV) |
| 0 | 5 | 10.20 | 16.80 | 1/(1+SMPLRT_DIV) |
| 0 | 6 | 5.05 | 32.50 | 1/(1+SMPLRT_DIV) |
| 0 | 7 | 420.00 | 1.38 | 1 |



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Low Power accelerometer mode averaging filter settings:

| ACCEL_FCHOICE_B | A_DLPF_CFG | DEC2_CFG | Averaging Filter |
|---|---|---|---|
| 1 | X | 0 | 1x |
| 0 | 7 | 0 | 4x |
| 0 | 7 | 1 | 8x |
| 0 | 7 | 2 | 16x |
| 0 | 7 | 3 | 32x |

## 12.14 REGISTER 30 – GYROSCOPE LOW POWER MODE CONFIGURATION

**Register Name: LP_MODE_CONFIG**
**Register Type: READ/WRITE**
**Register Address: 30 (Decimal); 1E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | GYRO_CYCLE | When set to '1' low-power gyroscope mode is enabled. Default setting is '0' |
| [6:4] | GYRO_AVGCFG[2:0] | Averaging filter configuration for low-power gyroscope mode. Default setting is '000'<br><br>The following list shows averaging filter configurations for different settings:<br>000 = 1x<br>001 = 2x<br>010 = 4x<br>011 = 8x<br>100 = 16x<br>101 = 32x<br>110 = 64x<br>111 = 128x |
| [3:0] | - | Reserved |

To operate in gyroscope low-power mode or 6-axis low-power mode, GYRO_CYCLE should be set to '1.' Gyroscope filter configuration is determined by GYRO_AVGCFG[2:0] that sets the averaging filter configuration. It is not dependent on DLPF_CFG[2:0].

## 12.15 REGISTER 32 – WAKE-ON MOTION THRESHOLD (X-AXIS ACCELEROMETER)

**Register Name: ACCEL_WOM_X_THR**
**Register Type: READ/WRITE**
**Register Address: 32 (Decimal); 20 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | WOM_X_TH[7:0] | This register holds the threshold value for the Wake on Motion Interrupt for X-axis accelerometer. |



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## 12.16 REGISTER 33 – WAKE-ON MOTION THRESHOLD (Y-AXIS ACCELEROMETER)

**Register Name: ACCEL_WOM_Y_THR**
**Register Type: READ/WRITE**
**Register Address: 33 (Decimal); 21 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | WOM_Y_TH[7:0] | This register holds the threshold value for the Wake on Motion Interrupt for Y-axis accelerometer. |

## 12.17 REGISTER 34 – WAKE-ON MOTION THRESHOLD (Z-AXIS ACCELEROMETER)

**Register Name: ACCEL_WOM_Z_THR**
**Register Type: READ/WRITE**
**Register Address: 34 (Decimal); 22 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | WOM_Z_TH[7:0] | This register holds the threshold value for the Wake on Motion Interrupt for Z-axis accelerometer. |

## 12.18 REGISTER 35 – FIFO ENABLE

**Register Name: FIFO_EN**
**Register Type: READ/WRITE**
**Register Address: 35 (Decimal); 23 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | TEMP_OUT | 1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate. If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [6] | GYRO_XOUT | 1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate. If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [5] | GYRO_YOUT | 1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate. If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [4] | GYRO_ZOUT | 1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate. If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [3] | ACCEL_XYZ_OUT | 1 – Write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate.<br>0 – Function is disabled. |
| [2:0] | - | Reserved |



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## 12.19 REGISTER 36 – I²C MASTER CONTROL

**Register Name: I2C_MST_CTRL**
**Register Type: READ/WRITE**
**Register Address: 36 (Decimal); 24 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | MULT_MST_EN | 1 – Enables multi-master capability<br>0 – Function is disabled |
| [6:5] | - | Reserved |
| [4] | I2C_MST_P_NSR | This bit controls the I²C master's transition from one slave read to the next slave read<br>1 – There is a stop between reads<br>0 – There is a restart between reads |
| [3:0] | I2C_MST_CLK | Sets I2C master clock according to the table below |

| I2C_MST_CLK[3:0] | Slowest Frequency (kHz) | Duty Cycle |
|---|---|---|
| 0 | 341 | 42% |
| 1 | 341 | 50% |
| 2 | 315 | 38% |
| 3 | 315 | 46% |
| 4 | 293 | 43% |
| 5 | 293 | 50% |
| 6 | 273 | 40% |
| 7 | 273 | 47% |
| 8 | 256 | 38% |
| 9 | Invalid | Invalid |
| 10 | Invalid | Invalid |
| 11 | Invalid | Invalid |
| 12 | 410 | 40% |
| 13 | 410 | 40% |
| 14 | 372 | 45% |
| 15 | 372 | 45% |

## 12.20 REGISTER 37 – I²C SLAVE 0 PHYSICAL ADDRESS

**Register Name: I2C_SLV0_ADDR**
**Register Type: READ/WRITE**
**Register Address: 37 (Decimal); 25 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV0_RNW | 1 – Transfer is a read<br>0 – Transfer is a write |
| [6:0] | I2C_ID_0 | Physical address of I²C slave 0 |



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## 12.21 REGISTER 38 – I²C SLAVE 0 REGISTER ADDRESS

**Register Name: I2C_SLV0_REG**
**Register Type: READ/WRITE**
**Register Address: 38 (Decimal); 26 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV0_REG | I²C slave 0 register address from where to begin data transfer |

## 12.22 REGISTER 39 – I²C SLAVE 0 CONTROL

**Register Name: I2C_SLV0_CTRL**
**Register Type: READ/WRITE**
**Register Address: 39 (Decimal); 27 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV0_EN | 1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I²C slave 0.<br>0 – Function is disabled for this slave |
| [6] | I2C_SLV0_BYTE_SW | 1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV0_REG[0] = 1, or if the last byte read has a register address lsb = 0.<br><br>For example, if I2C_SLV0_REG = 0x1, and I2C_SLV0_LENG = 0x4:<br>1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00,<br>2) The second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01,<br>3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03<br><br>0 – No swapping occurs, bytes are written in order read. |
| [5] | I2C_SLV0_REG_DIS | When set, the transaction does not write a register value, it will only read data, or write data |
| [4] | I2C_SLV0_GRP | External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc..<br>0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address. |
| 3:0 | I2C_SLV0_LENG | Number of bytes to be read from I²C slave 0 |

## 12.23 REGISTER 40 – I²C SLAVE 1 PHYSICAL ADDRESS

**Register Name: I2C_SLV1_ADDR**
**Register Type: READ/WRITE**
**Register Address: 40 (Decimal); 28 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV1_RNW | 1 – Transfer is a read<br>0 – Transfer is a write |
| [6:0] | I2C_ID_1 | Physical address of I²C slave 1 |



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## 12.24 REGISTER 41 – I²C SLAVE 1 REGISTER ADDRESS

**Register Name: I2C_SLV1_REG**
**Register Type: READ/WRITE**
**Register Address: 41 (Decimal); 29 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV1_REG | I²C slave 1 register address from where to begin data transfer |

## 12.25 REGISTER 39 – I²C SLAVE 1 CONTROL

**Register Name: I2C_SLV1_CTRL**
**Register Type: READ/WRITE**
**Register Address: 42 (Decimal); 2A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV1_EN | 1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I²C slave 0.<br>0 – Function is disabled for this slave. |
| [6] | I2C_SLV1_BYTE_SW | 1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV1_REG[0] = 1, or if the last byte read has a register address lsb = 0.<br><br>For example, if I2C_SLV1_REG = 0x1, and I2C_SLV1_LENG = 0x4:<br>1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00,<br>2) The second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01,<br>3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03<br><br>0 – No swapping occurs; bytes are written in the order read. |
| [5] | I2C_SLV1_REG_DIS | When set, the transaction does not write a register value, it will only read data, or write data |
| [4] | I2C_SLV1_GRP | External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc..<br>0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address. |
| 3:0 | I2C_SLV1_LENG | Number of bytes to be read from I²C slave 1. |

## 12.26 REGISTER 43 – I²C SLAVE 2 PHYSICAL ADDRESS

**Register Name: I2C_SLV2_ADDR**
**Register Type: READ/WRITE**
**Register Address: 43 (Decimal); 2B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV2_RNW | 1 – Transfer is a read.<br>0 – Transfer is a write. |
| [6:0] | I2C_ID_2 | Physical address of I²C slave 2. |



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## 12.27 REGISTER 44 – I²C SLAVE 2 REGISTER ADDRESS

**Register Name: I2C_SLV2_REG**
**Register Type: READ/WRITE**
**Register Address: 44 (Decimal); 2C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV2_REG | I²C slave 2 register address from where to begin data transfer. |

## 12.28 REGISTER 45 – I²C SLAVE 2 CONTROL

**Register Name: I2C_SLV2_CTRL**
**Register Type: READ/WRITE**
**Register Address: 45 (Decimal); 2D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | I2C_SLV2_EN | 1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I²C slave 0.<br>0 – Function is disabled for this slave. |
| [6] | I2C_SLV2_BYTE_SW | 1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV2_REG[0] = 1, or if the last byte read has a register address lsb = 0.<br><br>For example, if I2C_SLV2_REG = 0x1, and I2C_SLV2_LENG = 0x4:<br>1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00,<br>2) The second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01,<br>3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03<br><br>0 – No swapping occurs; bytes are written in the order read. |
| [5] | I2C_SLV2_REG_DIS | When set, the transaction does not write a register value, it will only read data, or write data. |
| [4] | I2C_SLV2_GRP | External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc..<br>0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address. |
| 3:0 | I2C_SLV2_LENG | Number of bytes to be read from I²C slave 2. |

## 12.29 REGISTER 46 – FSYNC ODR DELAY ENABLE

**Register Name: ODR_DELAY_EN**
**Register Type: READ/WRITE**
**Register Address: 46 (Decimal); 2E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | ODR_DELAY_EN | 1 – Enables FSYNC ODR delay counter.<br>0 – Function is disabled. |
| [6:0] | - | Reserved |



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## 12.30 REGISTER 54 – FSYNC INTERRUPT STATUS

**Register Name: FSYNC_INT**
**Register Type: READ to CLEAR**
**Register Address: 54 (Decimal); 36 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | FSYNC_INT | This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read. |
| [6:0] | - | Reserved |

## 12.31 REGISTER 55 – INT PIN CONFIGURATION

**Register Name: INT_PIN_CFG**
**Register Type: READ/WRITE**
**Register Address: 55 (Decimal); 37 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | INT_LEVEL | 1 – The logic level for INT pin is active low.<br>0 – The logic level for INT pin is active high. |
| [6] | INT_OPEN | 1 – INT pin is configured as open drain.<br>0 – INT pin is configured as push-pull. |
| [5] | LATCH_INT_EN | 1 – INT pin level held until interrupt status is cleared.<br>0 – INT pin indicates interrupt pulse's width is 50 µs. |
| [4] | INT_RD_CLEAR | 1 – Interrupt status is cleared if any read operation is performed.<br>0 – Interrupt status is cleared only by reading INT_STATUS register. |
| [3] | FSYNC_INT_LEVEL | 1 – The logic level for the FSYNC pin as an interrupt is active low.<br>0 – The logic level for the FSYNC pin as an interrupt is active high. |
| [2] | FSYNC_INT_MODE_EN | When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by F*SYNC_INT_LEVEL*.<br>When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt. |
| [1:0] | - | Reserved |

## 12.32 REGISTER 56 – INTERRUPT ENABLE

**Register Name: INT_ENABLE**
**Register Type: READ/WRITE**
**Register Address: 56 (Decimal); 38 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | WOM_X_INT_EN | 1 – Enable WoM interrupt on X-axis accelerometer. Default setting is 0. |
| [6] | WOM_Y_INT_EN | 1 – Enable WoM interrupt on Y-axis accelerometer. Default setting is 0. |
| [5] | WOM_Z_INT_EN | 1 – Enable WoM interrupt on Z-axis accelerometer. Default setting is 0. |
| [4] | FIFO_OFLOW_EN | 1 – Enables a FIFO buffer overflow to generate an interrupt.<br>0 – Function is disabled. |
| [3] | - | Reserved |
| [2] | GDRIVE_INT_EN | Gyroscope Drive System Ready interrupt enable |
| [1] | - | Reserved |
| [0] | DATA_RDY_INT_EN | Data ready interrupt enable |

### 12.33 REGISTER 57 – FIFO WATERMARK INTERRUPT STATUS

**Register Name: FIFO_WM_INT_STATUS**
**Register Type: READ to CLEAR**
**Register Address: 57 (Decimal); 39 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | - | Reserved |
| [6] | FIFO_WM_INT | FIFO Watermark interrupt status. Cleared on Read. |
| [5:0] | - | Reserved |

### 12.34 REGISTER 58 – INTERRUPT STATUS

**Register Name: INT_STATUS**
**Register Type: READ to CLEAR**
**Register Address: 58 (Decimal); 3A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | WOM_X_INT | X-axis accelerometer WoM interrupt status. Cleared on Read. |
| [6] | WOM_Y_INT | Y-axis accelerometer WoM interrupt status. Cleared on Read. |
| [5] | WOM_Z_INT | Z-axis accelerometer WoM interrupt status. Cleared on Read. |
| [4] | FIFO_OFLOW_INT | This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read. |
| [3] | - | Reserved |
| [2] | GDRIVE_INT | Gyroscope Drive System Ready interrupt. |
| [1] | - | Reserved |
| [0] | DATA_RDY_INT | This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read. |

### 12.35 REGISTER 59 – HIGH BYTE OF ACCELEROMETER X-AXIS DATA

**Register Name: ACCEL_XOUT_H**
**Register Type: READ**
**Register Address: 59 (Decimal); 3B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_XOUT[15:8] | High byte of accelerometer x-axis data. |

### 12.36 REGISTER 60 – LOW BYTE OF ACCELEROMETER X-AXIS DATA

**Register Name: ACCEL_XOUT_L**
**Register Type: READ**
**Register Address: 60 (Decimal); 3C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_XOUT[7:0] | Low byte of accelerometer x-axis data. |



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## 12.37 REGISTER 61 – HIGH BYTE OF ACCELEROMETER Y-AXIS DATA

**Register Name: ACCEL_YOUT_H**
**Register Type: READ**
**Register Address: 61 (Decimal); 3D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_YOUT[15:8] | High byte of accelerometer y-axis data. |

## 12.38 REGISTER 62 – LOW BYTE OF ACCELEROMETER Y-AXIS DATA

**Register Name: ACCEL_YOUT_L**
**Register Type: READ**
**Register Address: 62 (Decimal); 3E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_YOUT[7:0] | Low byte of accelerometer y-axis data. |

## 12.39 REGISTER 63 – HIGH BYTE OF ACCELEROMETER Z-AXIS DATA

**Register Name: ACCEL_ZOUT_H**
**Register Type: READ**
**Register Address: 63 (Decimal); 3F (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_ZOUT[15:8] | High byte of accelerometer z-axis data. |

## 12.40 REGISTER 64 – LOW BYTE OF ACCELEROMETER Z-AXIS DATA

**Register Name: ACCEL_ZOUT_L**
**Register Type: READ**
**Register Address: 64 (Decimal); 40 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_ZOUT[7:0] | Low byte of accelerometer z-axis data. |

## 12.41 REGISTER 65 – HIGH BYTE OF TEMPERATURE SENSOR DATA

**Register Name: TEMP_OUT_H**
**Register Type: READ**
**Register Address: 65 (Decimal); 41 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT[15:8] | High byte of the temperature sensor output. |

## 12.42 REGISTER 66 – LOW BYTE OF TEMPERATURE SENSOR DATA

**Register Name: TEMP_OUT_L**
**Register Type: READ**
**Register Address: 66 (Decimal); 42 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT[7:0] | Low byte of the temperature sensor output. |

TEMP_OUT may be converted to temperature in degrees C by using the following formula:

TEMP_degC = (TEMP_OUT[15:0]/Temp_Sensitivity) + RoomTemp_Offset

where Temp_Sensitivity = 326.8 LSB/$^{o}$C and RoomTemp_Offset = 25$^{o}$C

## 12.43 REGISTER 67 – HIGH BYTE OF GYROSCOPE X-AXIS DATA

**Register Name: GYRO_XOUT_H**
**Register Type: READ**
**Register Address: 67 (Decimal); 43 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT[15:8] | High byte of gyroscope x-axis data. |

## 12.44 REGISTER 68 – LOW BYTE OF GYROSCOPE X-AXIS DATA

**Register Name: GYRO_XOUT_L**
**Register Type: READ**
**Register Address: 68 (Decimal); 44 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT[7:0] | Low byte of gyroscope x-axis data. |

## 12.45 REGISTER 69 – HIGH BYTE OF GYROSCOPE Y-AXIS DATA

**Register Name: GYRO_YOUT_H**
**Register Type: READ**
**Register Address: 69 (Decimal); 45 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT[15:8] | High byte of gyroscope y-axis data. |

## 12.46 REGISTER 70 – LOW BYTE OF GYROSCOPE Y-AXIS DATA

**Register Name: GYRO_YOUT_L**
**Register Type: READ**
**Register Address: 70 (Decimal); 46 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT[7:0] | Low byte of gyroscope y-axis data. |

## 12.47 REGISTER 71 – HIGH BYTE OF GYROSCOPE Z-AXIS DATA

**Register Name: GYRO_ZOUT_H**
**Register Type: READ**
**Register Address: 71 (Decimal); 47 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT[15:8] | High byte of gyroscope z-axis data. |

## 12.48 REGISTER 72 – LOW BYTE OF GYROSCOPE Z-AXIS DATA

**Register Name: GYRO_ZOUT_L**
**Register Type: READ**
**Register Address: 72 (Decimal); 48 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT[7:0] | Low byte of gyroscope z-axis data. |

## 12.49 REGISTER 73 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_00**
**Register Type: READ**
**Register Address: 73 (Decimal); 49 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_00 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.50 REGISTER 74 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_01**
**Register Type: READ**
**Register Address: 74 (Decimal); 4A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_01 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.51 REGISTER 75 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_02**
**Register Type: READ**
**Register Address: 75 (Decimal); 4B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_02 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.52 REGISTER 76 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_03**
**Register Type: READ**
**Register Address: 76 (Decimal); 4C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_03 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.53 REGISTER 77 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_04**
**Register Type: READ**
**Register Address: 77 (Decimal); 4D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_04 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.54 REGISTER 78 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_05**
**Register Type: READ**
**Register Address: 78 (Decimal); 4E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_05 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.55 REGISTER 79 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_06**
**Register Type: READ**
**Register Address: 79 (Decimal); 4F (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_06 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.56 REGISTER 80 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_07**
**Register Type: READ**
**Register Address: 80 (Decimal); 50 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_07 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.57 REGISTER 81 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_08**
**Register Type: READ**
**Register Address: 81 (Decimal); 51 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_08 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.58 REGISTER 82 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_09**
**Register Type: READ**
**Register Address: 82 (Decimal); 52 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_09 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.59 REGISTER 83 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_10**
**Register Type: READ**
**Register Address: 83 (Decimal); 53 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_10 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.60 REGISTER 84 – SENSOR DATA FROM EXTERNAL I²C DEVICES

**Register Name: EXT_SLV_SENS_DATA_11**
**Register Type: READ**
**Register Address: 84 (Decimal); 54 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | EXT_SLV_SENS_DATA_11 | Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers |

## 12.61 REGISTER 95 – FSYNC ODR DELAY COUNTER HIGH BYTE

**Register Name: ODR_DLY_CNT_HI**
**Register Type: READ/WRITE**
**Register Address: 95 (Decimal); 5F (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ODR_DLY_TIME_CNT[15:8] | High byte of FSYNC ODR delay counter. |

## 12.62 REGISTER 96 – FSYNC ODR DELAY COUNTER LOW BYTE

**Register Name: ODR_DLY_CNT_LO**
**Register Type: READ/WRITE**
**Register Address: 96 (Decimal); 60 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ODR_DLY_TIME_CNT[7:0] | Low byte of FSYNC ODR delay counter. |

## 12.63 REGISTER 97 – FIFO WATERMARK THRESHOLD IN NUMBER OF BYTES

**Register Name: FIFO_WM_TH**
**Register Type: READ/WRITE**
**Register Address: 97 (Decimal); 61 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_WM_TH | FIFO watermark threshold in number of bytes. If zero then watermark interrupt is disabled. |

## 12.64 REGISTER 99 – SLAVE 0 DATA OUT

**Register Name: I2C_SLV0_DO**
**Register Type: READ/WRITE**
**Register Address: 99 (Decimal); 63 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV0_DO | Data out when slave 0 is set to write. |

## 12.65 REGISTER 100 – SLAVE 1 DATA OUT

**Register Name: I2C_SLV1_DO**
**Register Type: READ/WRITE**
**Register Address: 100 (Decimal); 64 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV1_DO | Data out when slave 1 is set to write. |

## 12.66 REGISTER 101 – SLAVE 2 DATA OUT

**Register Name: I2C_SLV2_DO**
**Register Type: READ/WRITE**
**Register Address: 101 (Decimal); 65 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | I2C_SLV2_DO | Data out when slave 2 is set to write. |

## 12.67 REGISTER 103 – I2C MASTER DELAY CONTROL

**Register Name: I2C_MST_DELAY_CTRL**
**Register Type: READ/WRITE**
**Register Address: 103 (Decimal); 67 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | DELAY_ES_SHADOW | Delays shadowing of external sensor data until all data is received. |
| [6:3] | - | Reserved |
| [2] | I2C_SLV2_DELAY_EN | When enabled, slave 2 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG. |
| [1] | I2C_SLV1_DELAY_EN | When enabled, slave 1 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG. |
| [0] | I2C_SLV0_DELAY_EN | When enabled, slave 0 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG |

## 12.68 REGISTER 104 – SIGNAL PATH RESET

**Register Name: SIGNAL_PATH_RESET**
**Register Type: READ/WRITE**
**Register Address: 104 (Decimal); 68 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:5] | FS_SEL_OIS | OIS Path Gyro Full Scale Select:<br>000 = ±250 dps<br>001 = ±500 dps<br>010 = ±1000 dps<br>011 = ±2000 dps<br>101 = ±31.25 dps<br>110 = ±62.5 dps<br>111 = ±125 dps |
| [4:3] | FCHOICE_OIS_B | Used for OIS path gyroscope DLPF configuration as shown in the table below. |
| [2] | GYRO_RST | Reset gyroscope digital signal path.<br>Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers. |
| [1] | ACCEL_RST | Reset accelerometer digital signal path.<br>Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers. |
| [0] | TEMP_RST | Reset temperature sensor digital signal path.<br>Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers. |



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| FCHOICE_OIS_B | FCHOICE_B | DLPF_CFG | Filter BW (Hz) | Filter Delay (ms) | ODR (kHz) |
|---|---|---|---|---|---|
| 11 | xx | x | 8800 | 0.064 | 32 |
| 10 | 10 | x | 3600 | 0.11 | 32 |
| 10 | 00 | x | 3600 | 0.17 | 8 |
| 01 | 00 | x | 250 | 0.97 | 8 |
| 00 | 00 | 1 | 184 | 2.9 | 1/(1+SMPLRT_DIV) |
| 00 | 00 | 2 | 92 | 3.9 | 1/(1+SMPLRT_DIV) |
| 00 | 00 | 3 | 41 | 5.9 | 1/(1+SMPLRT_DIV) |
| 00 | 00 | 4 | 20 | 9.9 | 1/(1+SMPLRT_DIV) |
| 00 | 00 | 5 | 10 | 17.85 | 1/(1+SMPLRT_DIV) |
| 00 | 00 | 6 | 5 | 33.48 | 1/(1+SMPLRT_DIV) |

## 12.69 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

**Register Name: ACCEL_INTEL_CTRL**
**Register Type: READ/WRITE**
**Register Address: 105 (Decimal); 69 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | ACCEL_INTEL_EN | This bit enables the Wake-on-Motion detection logic. |
| [6] | ACCEL_INTEL_MODE | 0 – Do not use.<br>1 – Compare the current sample with the previous sample, |
| [5:4] | ACCEL_FCHOICE_OIS_B | Used for OIS path accelerometer DLPF configuration as shown in the table below. |
| [3:1] | - | Reserved |
| [0] | WOM_INT_MODE | 0 – Set WoM interrupt on the OR of all enabled accelerometer thresholds.<br>1 – Set WoM interrupt on the AND of all enabled accelerometer threshold.<br>Default setting is 0 |

| ACCEL_FCHOICE_OIS_B | ACCEL_FCHOICE_B | A_DLPF_CFG | Filter BW (Hz) | Filter Delay (ms) | ODR (kHz) |
|---|---|---|---|---|---|
| 11 | X | X | 1046.00 | 0.50 | 4 |
| 10 | 0 | X | 420.00 | 1.38 | 1 |
| 01 | 0 | 0 | 218.10 | 1.88 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 1 | 218.10 | 1.88 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 2 | 99.00 | 2.88 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 3 | 44.80 | 4.88 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 4 | 21.20 | 8.87 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 5 | 10.20 | 16.80 | 1/(1+SMPLRT_DIV) |
| 01 | 0 | 6 | 5.05 | 32.50 | 1/(1+SMPLRT_DIV) |

## 12.70 REGISTER 106 – USER CONTROL

**Register Name: USER_CTRL**
**Register Type: READ/WRITE**
**Register Address: 106 (Decimal); 6A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | - | Reserved |
| [6] | FIFO_EN | 1 – Enable FIFO operation mode.<br>0 – Disable FIFO access from serial interface. |



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| BIT | NAME | FUNCTION |
|---|---|---|
| [5] | I2C_MST_EN | 1 – Enable the I²C master interface module: Pins AUX_DA and AUX_CL are isolated from pins AP_SDA/AP_SDI and AP_SCL/AP_SCLK.<br>0 – Disable the I²C master interface module: Pins AUX_DA and AUX_CL are driven by pins AP_SDA/AP_SDI and AP_SCL/AP_SCLK. |
| [4] | I2C_IF_DIS | Disable I2C slave interface to host and put the interface in SPI mode. |
| [3] | - | Reserved |
| [2] | FIFO_RST | 1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20MHz clock. |
| [1] | - | Reserved |
| [0] | SIG_COND_RST | 1 – Reset gyroscope digital signal path, accelerometer digital signal path, and temperature sensor digital signal path. This bit also clears all the sensor registers. |

## 12.71 REGISTER 107 – POWER MANAGEMENT 1

**Register Name: PWR_MGMT_1**
**Register Type: READ/WRITE**
**Register Address: 107 (Decimal); 6B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | DEVICE_RESET | 1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done. |
| [6] | SLEEP | When set to 1, the chip is set to sleep mode. |
| [5] | CYCLE | When set to 1, and SLEEP and GYRO_STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample at a rate determined by SMPLRT_DIV.<br>NOTE: When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples. |
| [4] | GYRO_STANDBY | When set, the gyro drive and PLL circuitry are enabled, but the sense paths are disabled. This is a low power mode that allows quick enabling of the gyros. |
| [3] | TEMP_DIS | When set to 1, this bit disables the temperature sensor. |
| [2:0] | CLKSEL[2:0] | **Code** **Clock Source**<br>0 Internal 20 MHz oscillator<br>1 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator<br>2 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator<br>3 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator<br>4 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator<br>5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator<br>6 Internal 20MHz oscillator<br>7 Stops the clock and keeps timing generator in reset |



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## 12.72 REGISTER 108 – POWER MANAGEMENT 2

**Register Name: PWR_MGMT_2**
**Register Type: READ/WRITE**
**Register Address: 108 (Decimal); 6C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | LP_DIS | When gyroscope is disabled, this bit controls accelerometer duty cycling operation mode.<br>1 – System will not enter sleep when gyroscope is disabled and accelerometer is off while duty cycling.<br>0 - System will enter sleep when gyroscope is disabled and accelerometer is off while duty cycling.<br><br>This bit should be set to 1 when reading from SRAM/FIFO. |
| [6] | - | Reserved |
| [5] | STBY_XA | 1 – X accelerometer is disabled.<br>0 – X accelerometer is on. |
| [4] | STBY_YA | 1 – Y accelerometer is disabled.<br>0 – Y accelerometer is on. |
| [3] | STBY_ZA | 1 – Z accelerometer is disabled.<br>0 – Z accelerometer is on. |
| [2] | STBY_XG | 1 – X gyro is disabled.<br>0 – X gyro is on. |
| [1] | STBY_YG | 1 – Y gyro is disabled.<br>0 – Y gyro is on. |
| [0] | STBY_ZG | 1 – Z gyro is disabled.<br>0 – Z gyro is on. |

## 12.73 REGISTER 112 – OIS ENABLE

**Register Name: OIS_ENABLE**
**Register Type: READ/WRITE**
**Register Address: 112 (Decimal); 70 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:2] | - | Reserved |
| [1] | OIS_ENABLE | 1 - Configures auxiliary interface as SPI slave (for connection to OIS controller).<br>0 – Configures auxiliary interface as I2C master (for connection to external sensors). |
| [0] | - | Reserved |



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## 12.74 REGISTERS 114 AND 115 – FIFO COUNT REGISTERS

**Register Name: FIFO_COUNTH**
**Register Type: READ**
**Register Address: 114 (Decimal); 72 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_COUNT[15:8] | High Bits, count indicates the number of written bytes in the FIFO.<br>Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL. |

**Register Name: FIFO_COUNTL**
**Register Type: READ**
**Register Address: 115 (Decimal); 73 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_COUNT[7:0] | Low Bits, count indicates the number of written bytes in the FIFO.<br>Note: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL. |

## 12.75 REGISTER 116 – FIFO READ WRITE

**Register Name: FIFO_R_W**
**Register Type: READ/WRITE**
**Register Address: 116 (Decimal); 74 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_DATA | Read/Write command provides Read or Write operation for the FIFO. |

**Description:**

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit FIFO_OFLOW_INT is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data is available. Normal data is precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

## 12.76 REGISTER 117 – WHO AM I

**Register Name: WHO_AM_I**
**Register Type: READ**
**Register Address: 117 (Decimal); 75 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | WHOAMI | Register to indicate to user which device is being accessed. |

**Description:**

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x20. This is different from the $I^2C$ address of the device as seen on the slave $I^2C$ controller by the applications processor. The $I^2C$ address of the ICM-20690 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

## 12.77 REGISTER 119 TO 126 – ACCELEROMETER OFFSET REGISTERS

**Register Name: XA_OFFSET_H**
**Register Type: READ/WRITE**
**Register Address: 119 (Decimal); 77 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | XA_OFFS[14:7] | Upper bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |

**Register Name: XA_OFFSET_L**
**Register Type: READ/WRITE**
**Register Address: 120 (Decimal); 78 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:1] | XA_OFFS[6:0] | Lower bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |
| [0] | - | Reserved |

**Register Name: YA_OFFSET_H**
**Register Type: READ/WRITE**
**Register Address: 122 (Decimal); 7A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | YA_OFFS[14:7] | Upper bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |

**Register Name: YA_OFFSET_L**
**Register Type: READ/WRITE**
**Register Address: 123 (Decimal); 7B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:1] | YA_OFFS[6:0] | Lower bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |
| [0] | - | Reserved |

**Register Name: ZA_OFFSET_H**
**Register Type: READ/WRITE**
**Register Address: 125 (Decimal); 7D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ZA_OFFS[14:7] | Upper bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |

**Register Name: ZA_OFFSET_L**
**Register Type: READ/WRITE**
**Register Address: 126 (Decimal); 7E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:1] | ZA_OFFS[6:0] | Lower bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps. |
| [0] | - | Reserved |



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# 13 DESCRIPTION OF REGISTERS SPECIFIC TO SECONDARY INTERFACE IN OIS MODE

The following registers are accessible from the secondary interface in OIS mode only. OIS controller should only read this data in SPI burst mode to avoid OIS sensor data update during reading. SPI single byte read mode should not be used.

## 13.1 REGISTER 0 – HIGH BYTE OF ACCELEROMETER X-AXIS OIS DATA

**Register Name: ACCEL_XOUT_OIS_H**
**Register Type: READ**
**Register Address: 00 (Decimal); 00 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_XOUT_OIS[15:8] | High byte of accelerometer x-axis OIS data. |

## 13.2 REGISTER 1 – LOW BYTE OF ACCELEROMETER X-AXIS OIS DATA

**Register Name: ACCEL_XOUT_OIS_L**
**Register Type: READ**
**Register Address: 01 (Decimal); 01 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_XOUT_OIS[7:0] | Low byte of accelerometer x-axis OIS data. |

## 13.3 REGISTER 2 – HIGH BYTE OF ACCELEROMETER Y-AXIS OIS DATA

**Register Name: ACCEL_YOUT_OIS_H**
**Register Type: READ**
**Register Address: 02 (Decimal); 02 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_YOUT_OIS[15:8] | High byte of accelerometer y-axis OIS data. |

## 13.4 REGISTER 3 – LOW BYTE OF ACCELEROMETER Y-AXIS OIS DATA

**Register Name: ACCEL_YOUT_OIS_L**
**Register Type: READ**
**Register Address: 03 (Decimal); 03 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_YOUT_OIS[7:0] | Low byte of accelerometer y-axis OIS data. |

## 13.5 REGISTER 4 – HIGH BYTE OF ACCELEROMETER Z-AXIS OIS DATA

**Register Name: ACCEL_ZOUT_OIS_H**
**Register Type: READ**
**Register Address: 04 (Decimal); 04 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_ZOUT_OIS[15:8] | High byte of accelerometer z-axis OIS data. |

## 13.6 REGISTER 5 – LOW BYTE OF ACCELEROMETER Z-AXIS OIS DATA

**Register Name: ACCEL_ZOUT_OIS_L**
**Register Type: READ**
**Register Address: 05 (Decimal); 05 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | ACCEL_ZOUT_OIS[7:0] | Low byte of accelerometer z-axis OIS data. |

## 13.7 REGISTER 6 – HIGH BYTE OF TEMPERATURE SENSOR OIS DATA

**Register Name: TEMP_OUT_OIS_H**
**Register Type: READ**
**Register Address: 06 (Decimal); 06 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT_OIS[15:8] | High byte of temperature sensor OIS data. |

## 13.8 REGISTER 7 – LOW BYTE OF TEMPERATURE SENSOR OIS DATA

**Register Name: TEMP_OUT_OIS_L**
**Register Type: READ**
**Register Address: 07 (Decimal); 07 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT_OIS[7:0] | Low byte of temperature sensor OIS data. |

## 13.9 REGISTER 8 – HIGH BYTE OF GYROSCOPE X-AXIS OIS DATA

**Register Name: GYRO_XOUT_OIS_H**
**Register Type: READ**
**Register Address: 08 (Decimal); 08 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT_OIS[15:8] | High byte of gyroscope x-axis OIS data. |

## 13.10 REGISTER 9 – LOW BYTE OF GYROSCOPE X-AXIS OIS DATA

**Register Name: GYRO_XOUT_OIS_L**
**Register Type: READ**
**Register Address: 09 (Decimal); 09 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT_OIS[7:0] | Low byte of gyroscope x-axis OIS data. |

### 13.11 REGISTER 10 – HIGH BYTE OF GYROSCOPE Y-AXIS OIS DATA

**Register Name: GYRO_YOUT_OIS_H**
**Register Type: READ**
**Register Address: 10 (Decimal); 0A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT_OIS[15:8] | High byte of gyroscope y-axis OIS data. |

### 13.12 REGISTER 11 – LOW BYTE OF GYROSCOPE Y-AXIS OIS DATA

**Register Name: GYRO_YOUT_OIS_L**
**Register Type: READ**
**Register Address: 11 (Decimal); 0B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT_OIS[7:0] | Low byte of gyroscope y-axis OIS data. |

### 13.13 REGISTER 12 – HIGH BYTE OF GYROSCOPE Z-AXIS OIS DATA

**Register Name: GYRO_ZOUT_OIS_H**
**Register Type: READ**
**Register Address: 12 (Decimal); 0C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT_OIS[15:8] | High byte of gyroscope z-axis OIS data. |

### 13.14 REGISTER 13 – LOW BYTE OF GYROSCOPE Z-AXIS OIS DATA

**Register Name: GYRO_ZOUT_OIS_L**
**Register Type: READ**
**Register Address: 13 (Decimal); 0D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT_OIS[7:0] | Low byte of gyroscope z-axis OIS data. |

# 14 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

# 15 DOCUMENT INFORMATION

## 15.1 REVISION HISTORY

| Revision Date | Revision | Description |
|---|---|---|
| 10/11/2016 | 1.0 | Initial Release |

InvenSense