Synchronous Sampling with an Array of ICS-52000 TDM Microphones

INTRODUCTION

The ICS-52000 is a MEMS microphone that supports up to 16 mic outputs, driving a common time division multiplexed (TDM) bus. By design, all of the ICS-52000 microphones on a common bus will sample their acoustic signals simultaneously and output their individual data words in their respective time slots in the TDM bus. Synchronized sampling is critical for the performance of a multi-microphone array because the algorithms typically used with these arrays require accurate synchronization between signals for optimum performance. Without the ICS-52000's integrated synchronization at start-up, these DSP algorithms would require a complicated series of delays and/or buffers to pre-process the signals to achieve the best algorithm performance.

This application note describes how an array of ICS-52000 microphones is synchronized and how multiple arrays can be synchronized together. See the ICS-52000 datasheet for a complete description of the microphone's operation and TDM interface.

SYNCHRONIZATION AT POWER-UP

The ICS-52000 follows a power-up sequence that ensures that all microphones in a common array will sample synchronously. To ensure this, all microphones in the array should share a common serial clock (CLK) from the system's clock master. This same master should also provide the word select (WS) signal to the first microphone in the array and the WS signal is daisy-chained from the WSO output of one mic to the WS input pin of the next microphone in the array, as illustrated in Figure 1. At start-up, signals are passed from WSO of one microphone to WS of the next microphone in the daisy chain. These signals enable each microphone to enumerate itself on the TDM bus so that it is properly configured to sample at the same time as all other mics in the array.
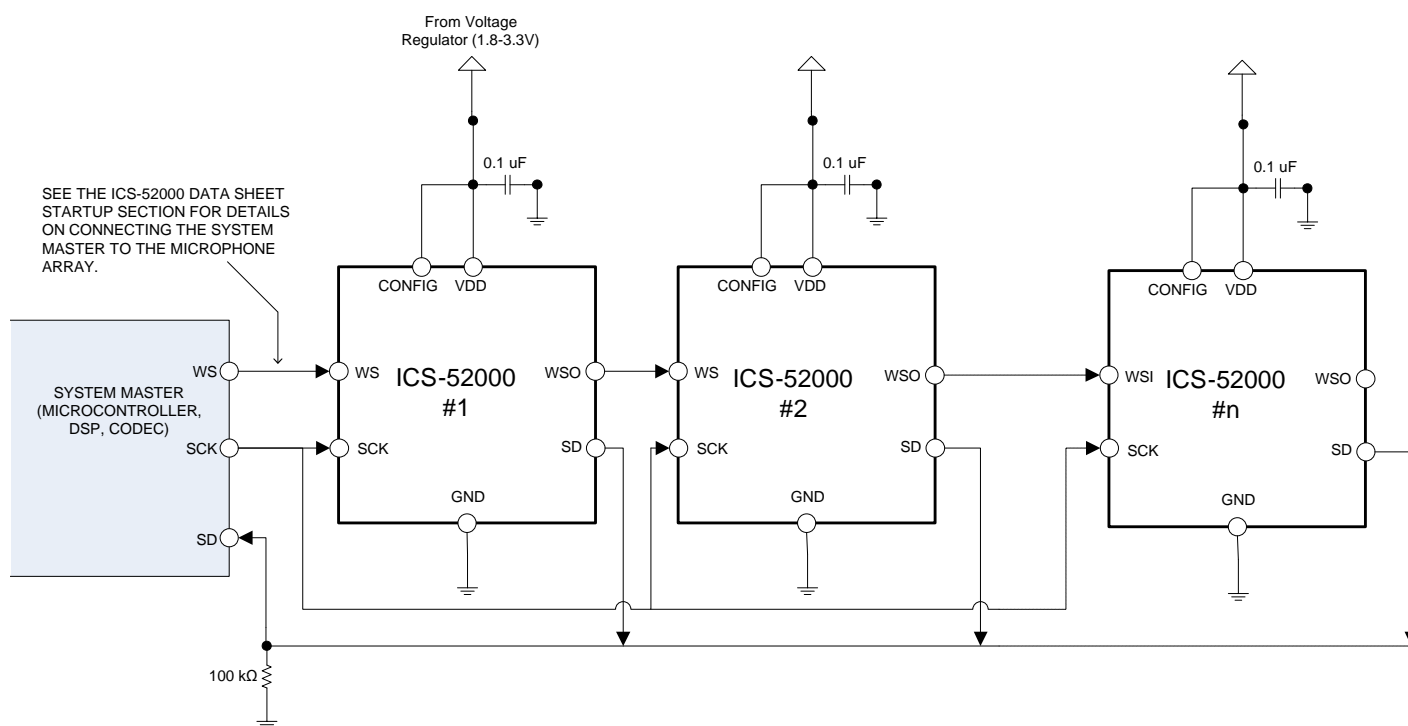

Figure 1. System Block Diagram

Following the start-up sequence, the signals in the WSO-to-WS daisy chain operate simply as a trigger for each microphone to output its data word in its respective TDM time slot on the common SD line. Each microphone holds its data word in a buffer until the time that the microphone is triggered to output onto the TDM bus. All words output in a single frame are sampled synchronously.

If the array is powered down or if the clock signals are stopped to enter standby mode, the array of ICS-52000 microphones will restart the synchronization sequence when the clocks are restarted.

SYNCHRONIZING MULTIPLE TDM BUSSES

Up to 16 ICS-52000 microphones can output data onto a common TDM SD data line. If more than 16 microphones are required for an array, or if lower clock frequencies are required for a specific application, multiple arrays of ICS-52000 microphones driving different SD signals can still be synchronized. If all microphones in these multiple TDM arrays share the same clock from the system master, then all microphones will start up in sync and will sample synchronously. Figure 2 shows a simple example of four ICS-52000 microphones driving two separate SD signals with two mics on each bus. The mics on these two separate busses are still clocked from the same source so the sampling will be in sync.
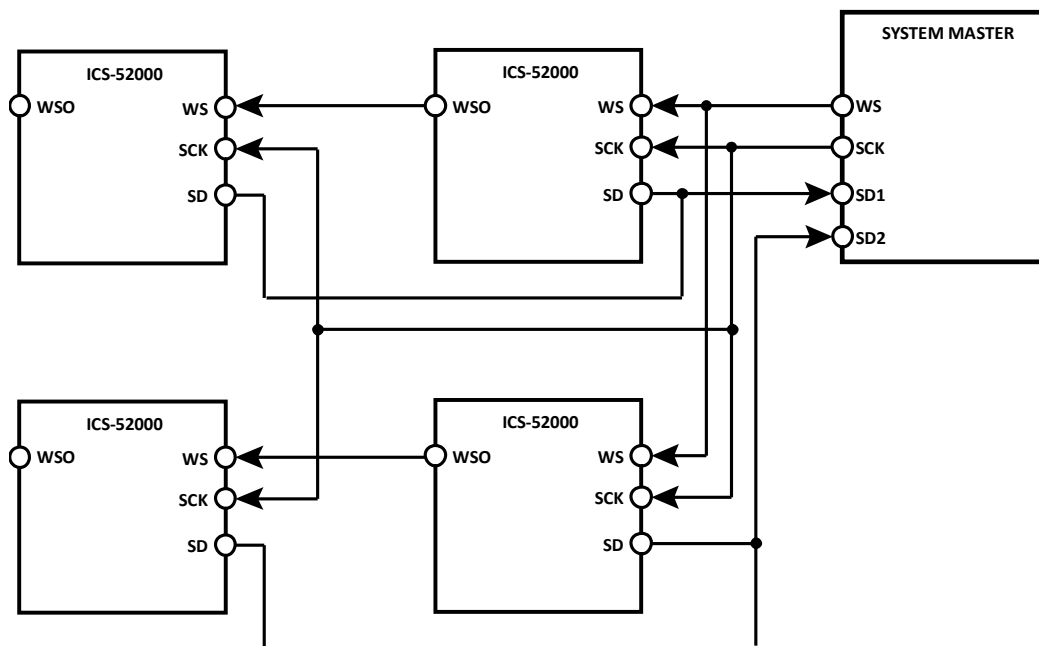
Figure 2. Multiple Synchronized TDM Data Busses

As with a design with a single SD bus, the drive strength of the clock master should be ensured to be sufficient to supply clean digital signals to all microphones across the designed PCB trace lengths.

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
10/11/2016	1.0	Initial Release
04/04/2017	1.1	Updated synchronization description and Figure 1
07/05/2017	1.2	Updated Formatting

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