T5808

Bottom-Port SoundWire® Digital Multi-Mode Microphone

GENERAL DESCRIPTION

The T5808 is a multi-mode, low noise digital MEMS microphone in a small package. The T5808 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order Σ-Δ modulator. The digital interface is a MIPI Alliance SoundWire® compliant interface which allows bi-directional data flow.

The T5808 has multiple modes of operation: High Quality, Low Power Listen (Always-On), Concurrent and Idle (sleep). The T5808 has high SNR and high AOP in all operational modes.

The T5808 is available in a standard 3.5 × 2.65 × 0.98 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation.

APPLICATIONS

- Smartphones
- Microphone Arrays
- Smart Speakers
- Headsets
- Tablets and Notebook PCs

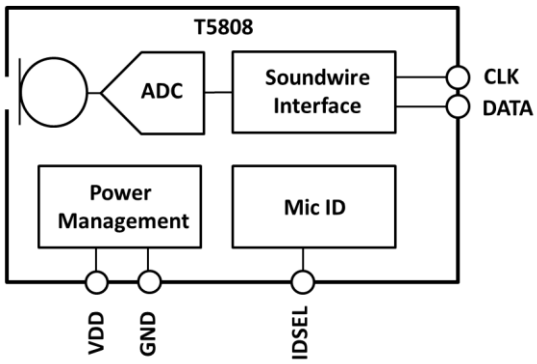
FEATURES

SPEC	HIGH QUALITY MODE	LOW POWER LISTEN MODE
Sensitivity	−41 dB FS ±1 dB	−26 dB FS ±1 dB
SNR	66 dBA	62 dBA
Current	650 µA	215 µA
AOP	135 dB SPL	120 dB SPL
Microphone Data Rate	2.4 Mbps or 3.072 Mbps[1]	0.6 Mbps or 0.768 Mbps[1]
SoundWire Bus Clock Frequency	Integer Multiple of Microphone data rate up to 9.6 MHz or 12.288 MHz	

Note 1: Acoustic performance for 2.4MHz, 0.768MHz

- 3.5 × 2.65 × 0.98 mm surface-mount package
- Extended frequency response from 40 Hz to 20 kHz
- Low power: 215 µA in Low Power Listen Mode
- Sleep (ClockStop) Mode: 9 µA
- MIPI Alliance SoundWire Slave v1.1 compliant
- IDSEL pin for multi-microphone enumeration (up to 7 devices)
- Compatible with Sn/Pb and Pb-free solder processes
- RoHS/WEEE compliant

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGING
MMICT5808-00-012	−40°C to +85°C	13” Tape and Reel

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SPECIFICATIONS

TABLE 1. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – GENERAL

T_A = 25°C, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE						
Directionality			Omni			
Output Polarity	Input acoustic pressure vs. output data		Non-Inverted			
Supply Voltage (V_{DD})		1.62	1.8	1.98	V	

TABLE 2. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 1-1 (HIGH QUALITY MODE)

T_A = 25°C, VDD = 1.8 V, f_{swclk} >= 2.4 MHz (Note 2), Mic Data Rate = 2.4 Mbps or 3.072 Mbps, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Sensitivity	1 kHz, 94 dB SPL	−42	−41	−40	dB FS	2
Signal-to-Noise Ratio (SNR)	20 kHz bandwidth, A-weighted		66		dBA	
Equivalent Input Noise (EIN)	20 kHz bandwidth, A-weighted		28		dBA SPL	
Dynamic Range	Derived from EIN and acoustic overload point		107		dB	
Total Harmonic Distortion (THD)	94 dB SPL		0.1		%	
Power Supply Rejection (PSR) Sine	1 kHz Sine Wave		-117		dB FS	
Power Supply Rejection (PSR) Square	217 Hz, 100 mV p-p square wave superimposed on VDD = 1.8 V, A-weighted		-114		dB FS (A)	
Acoustic Overload Point	10% THD		135		dB SPL	
Supply Current (Idd)	V_{DD} = 1.8 V, f_{swclk} = 2.4 MHz, No load		650		µA	3
	V_{DD} = 1.8 V, f_{swclk} = 2.4 MHz, 5 pF load		671		µA	3
Supported Ports						
Data Port 1 (High Quality Mode)	Active					
Data Port 2 (Low Power-Listen Mode)	Disabled					
Control Port	Active					

Note 2: Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.
Note 3: f_{swclk} should be an integer multiple of the desired Mic Data Rate see table 14 with permissible f_{swclk} and Mic Data Rates.

TABLE 3. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 1-2 (LOW POWER LISTEN MODE)

T_A = 25°C, VDD = 1.8V, f_{swclk} >= 0.6MHz (Note 2), Mic Data Rate =0.6 Mbps or 0.768 Mbps C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Sensitivity	1 kHz, 94 dB SPL	−27	−26	−25	dB FS	2
Signal-to-Noise Ratio (SNR)	8 kHz bandwidth, A-weighted, f_{swclk} = 0.768MHz		62		dBA	3
Equivalent Input Noise (EIN)	8 kHz bandwidth, A-weighted, f_{swclk} = 0.768MHz		32		dBA SPL	
Signal-to-Noise Ratio (SNR)	8 kHz bandwidth, A-weighted, f_{swclk} = 0.600MHz		60		dBA	3
Equivalent Input Noise (EIN)	8 kHz bandwidth, A-weighted, f_{swclk} = 0.600MHz		34		dBA SPL	
Dynamic Range	Derived from EIN and acoustic overload point, f_{swclk} = 0.768MHz		88		dB	
Total Harmonic Distortion (THD)	94 dB SPL		0.1		%	
Acoustic Overload Point	10% THD		120		dB SPL	
Supply Current (I_{dd})	V_{DD} = 1.8 V, f_{swclk} = 0.6 MHz , no load		215		µA	3
	V_{DD} = 1.8 V, f_{swclk} = 0.6 MHz , 5 pF load		220		µA	3
Supported Ports						
Data Port 1 (High Quality Mode)	Disabled					
Data Port 2 (Low Power-Listen Mode)	Active					
Control Port	Active					

Note 2: Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.
Note 3: f_{swclk} should be an integer multiple of the desired Mic Data Rate see table 14 with permissible f_{swclk} and Mic Data Rates.

TABLE 4. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 1-3 (CONCURRENT MODE)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Current (Idd)	V_{DD} = 1.8 V, f_{swclk} = 2.4MHz , no load		775		µA	3
	V_{DD} = 1.8 V, f_{swclk} = 2.4MHz , 5 pF load		796		µA	3
Acoustical/Electrical Specifications						
See Mode 1-1 Specifications for Port 1 Data						
See Mode 1-2 Specifications for Port 2 Data						
Supported Data Rates						
Data Port 1 (High Quality Mode)	Active					
Data Port 2 (Low Power-Listen Mode)	Active					
Control Port	Active					

Note 3: f_{swclk} should be an integer multiple of the desired Mic Data Rate see table 14 with permissible f_{swclk} and Mic Data Rates.

TABLE 5. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 1-4 (IDLE 1, CONTROL ONLY)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Current (I_{dd})	V_{DD} = 1.8 V, No load f_{swclk} = 0.6 MHz		31		µA	
Supported Data Rates						
Data Port 1 (High Quality Mode)	Disabled					
Data Port 2 (Low Power-Listen Mode)	Disabled					
Control Port	Active					

TABLE 6. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 2-2 (CLOCK STOP)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Current (I_{dd})	V_{DD} = 1.8 V, no load f_{swclk} = Off		9		µA	4
Supported Data Rates						
Data Rate, Port 1 f_{DATA1}	Disabled					
Data Rate, Port 2 f_{DATA2}	Disabled					
Control	Active					

Note 4: Mode 2-2 (Clock Stop) is notified through the SoundWire bus. When the clock restarts, the microphone will immediately enter Idle 1 Mode for ClockStopMode=0 OR re-sync and re-enumerate for ClockStopMode=1.

TABLE 7. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 3-1 (SYNC AND ENUMERATION)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Current (I_S)	V_{DD} = 1.8 V, no load f_{swclk} = 0.6MHz (assumes mic id 1 and 0 only)		350		µA	7
Acoustical/Electrical Specifications						
No Signal						
Supported Data Rates						
Data Rate, Port 1 f_{DATA1}	Disabled					
Data Rate, Port 2 f_{DATA2}	Disabled					
Control	Active					
Enumeration Control						
Unique ID = 0	IDSEL pin state: Tied to GND		0		Ω	5,6
Unique ID = 1	IDSEL pin state: Tied to VDD (max 1.98V)		0		Ω	5,6
Unique ID = 2	IDSEL pin state: Resistor to GND	25.7	27	28.3	kΩ	5,6
Unique ID = 3	IDSEL pin state: Resistor to GND	14.3	15	15.7	kΩ	5,6
Unique ID = 4	IDSEL pin state: Resistor to GND	7.8	8.2	8.6	kΩ	5,6
Unique ID = 5	IDSEL pin state: Resistor to GND	4.1	4.3	4.5	kΩ	5,6
Unique ID = 6	IDSEL pin state: Resistor to GND	2.1	2.2	2.3	kΩ	5,6
Tolerance of resistors			± 5		%	

Note 5: Unique ID refers to the 4 LSB bits in the SCP_DevID_0 register.
Note 6: Up to 7 T5808 slave devices can be configured by a single SoundWire master. See Sync & Enumeration section for details on slave enumeration.
Note 7: Guaranteed by design

TABLE 8. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 4-1 (POWER OFF, CLOCK ON)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V_{DD})				1.2	V	
Supply Current (I_{dd})	No load			9	µA	
Acoustical/Electrical Specifications						
No Signal						
Supported Data Rates						
Data Rate, Port 1 f_{DATA1}	Any Clock		Disabled		Mbps	
Data Rate, Port 2 f_{DATA2}	Any Clock		Disabled		Mbps	
Control	Inactive					

TABLE 9. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 4-2 (POWER OFF, CLOCK OFF)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V_{DD})				1.2	V	
Supply Current (Idd)	No load *f_{swclk} = max 1kHz*			9	µA	
Acoustical/Electrical Specifications						
Supported Data Rates						
Data Rate, Port 1 f_{DATA1}	Disabled					
Data Rate, Port 2 f_{DATA2}	Disabled					
Control	Inactive					

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TABLE 10. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – MODE 4-3 (POWER ON, CLOCK OFF)

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V_{DD})		1.5	1.8	1.98	V	
Supply Current (Idd)	No load *f_{swclk} = max 1kHz*		9		µA	
Acoustical/Electrical Specifications						
No Signal						
Supported Data Rates						
Data Rate, Port 1 f_{DATA1}	Disabled					
Data Rate, Port 2 f_{DATA2}	Disabled					
Control	Inactive					

TABLE 11. MODE TRANSITION TIMES

T_A = 25°C, VDD = 1.8 V, C_{LOAD} = 60 pF unless otherwise noted. All transition times are from simulation and are typical specifications which are not guaranteed.

FROM MODE \ TO MODE	1-1	1-2	1-3	1-4	2-2	3-1	4-1	4-2	4-3
1-1			100 µs	100 µs	100 µs		100 µs	100 µs	100 µs
1-2			100 µs	100 µs	100 µs		100 µs	100 µs	100 µs
1-3	100 µs	100 µs		100 µs	100 µs		100 µs	100 µs	100 µs
1-4	10 ms	10 ms			100 µs		100 µs	100 µs	100 µs
2-2				100 µs		100 µs	100 µs	100 µs	100 µs
3-1				100 µs			100 µs	100 µs	100 µs
4-1									
4-2									
4-3									

Greyed out cells are either same mode, not allowed, or not specified

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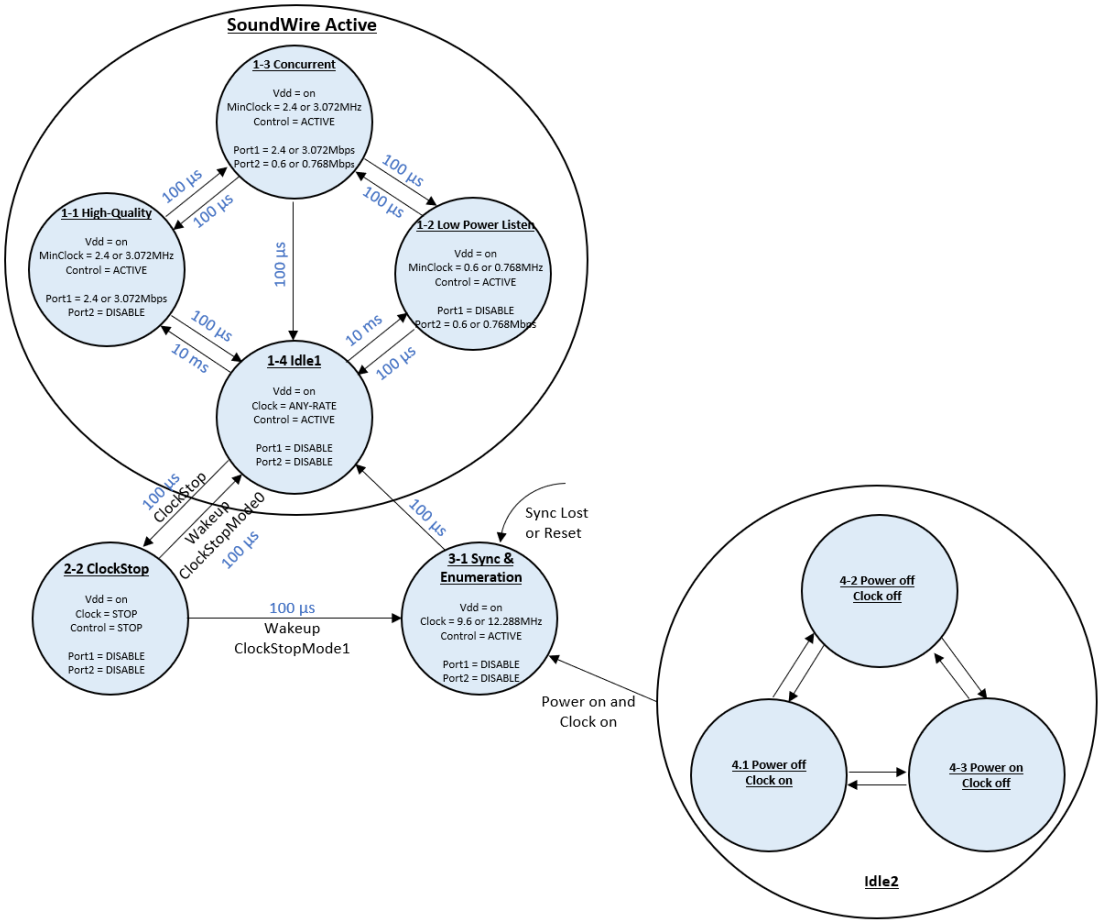

Figure 1. State transition diagram of available modes on T5808, transition time conditions described in Table 11.

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TABLE 12. DIGITAL INPUT/OUTPUT CHARACTERISTICS

T_A = 25°C, 1.62V < VDD < 1.98V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Voltage High (V_{IH})		0.65 × V_{DD}			V	
Input Voltage Low (V_{IL})				0.35 × V_{DD}	V	
Output Voltage High (V_{OH})	I_{LOAD} = 0.5 mA	0.7 × V_{DD}	V_{DD}		V	
Output Voltage Low (V_{OL})	I_{LOAD} = 0.5 mA		0	0.3 × V_{DD}	V	

TABLE 13. DIGITAL (PHY) INPUT/OUTPUT TIMING CHARACTERISTICS

T_A = 25°C, 1.7V < VDD < 1.9V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
f_{SWCLK}	Input clock frequency	0.024		12.288	MHz	
t_{CLKIN} (t_1/f_Clock)	Input clock period	81		41,666	ns	
t_Slew_Clock	Clock Slew Time	2		5.4	ns	
Clock Duty Cycle	f_{SWCLK} < 12.288MHz	45	50	55	%	
t_ISetup_min_Data	Data input setup time			0	ns	7
t_IHold_min_Data	Data input hold time			4	ns	7
t_ZD_Data_Min	Data output enable time from initial clock edge	7.9			ns	
t_DZ_Data_Max	Data output disable time from subsequent clock edge			4	ns	
t_OV_Data_Max	Data output valid time			27.9	ns	

Note 7: Guaranteed by design

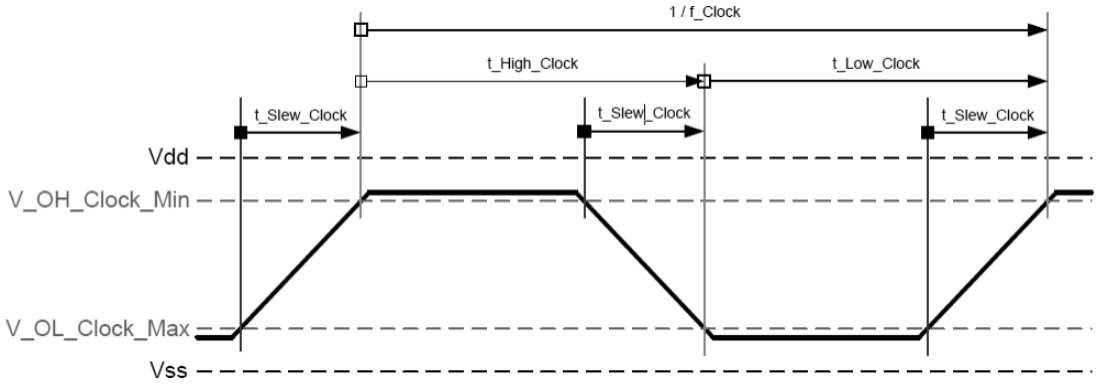

Figure 2. Digital Timing – Clock Output

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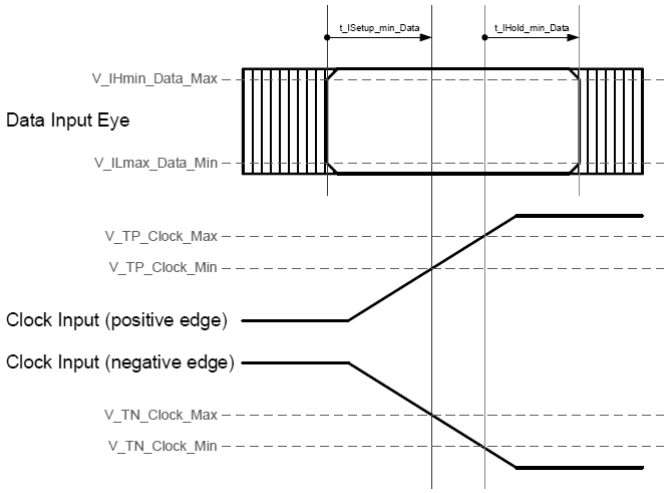

Figure 3. Digital Timing – Data Input

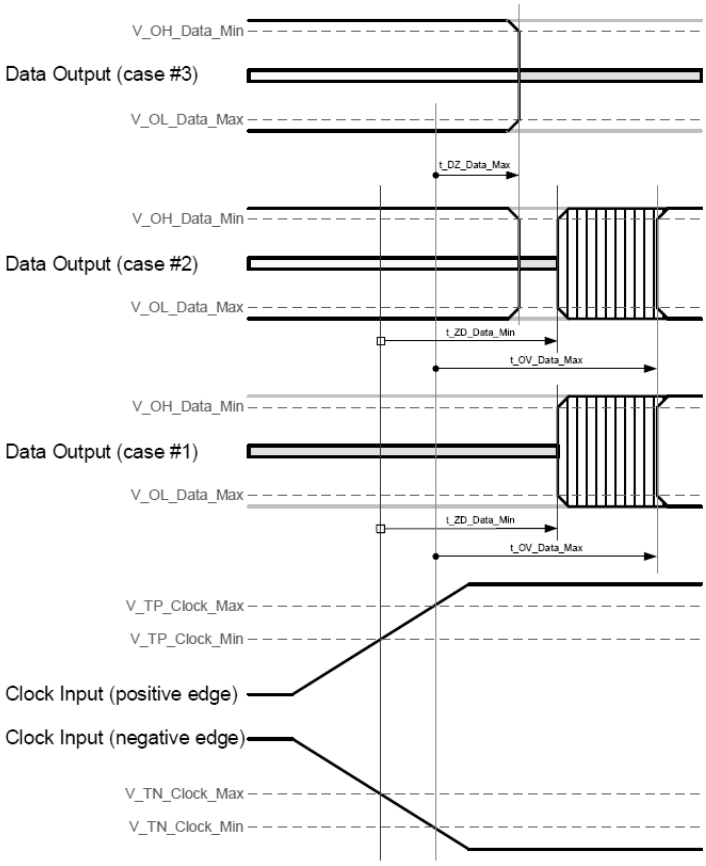

Figure 4. Digitial Timing – Data Output

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SOUNDWIRE OVERVIEW

The following section provides an overview of SoundWire. For the detailed SoundWire spec, please review the MIPI SoundWire specification document.

SoundWire microphones provide an interface to transport both audio and control over a pin efficient interface. In older microphone interfaces, the control portion has either been provided by separate pin, interpreted from the audio bus or power supply pins, or not supported – leading to a limited ability to control microphone behavior. The ability of SoundWire microphones to control the microphone from a centralized point in the audio subsystem enables better overall functionality and the following features:

- Control of power mode of each microphone in the system using an explicit control instead of implicit control using power or clock pins.
- Transition between Low Power Listen mode and High Quality mode without interruption for continuous audio use cases (i.e. low-power voice activation).

The SoundWire interface provides the following key capabilities:

- Transport of the following over a single two-pin interface:
  - Payload data channels
    - Each slave microphone has 2 data ports. Depending on how the SoundWire devices are configured, a microphone on the bus can operate in High Quality mode, Low Power Listen mode or both.
  - Control information
  - Setup commands
- Support for microphone low latency PDM audio transport over the same link with other audio sources
- Support for multilevel power saving by enabling frequency changes, temporary clock stoppage, and wake up response to in-band signaling
- Active indication of microphone device status including interrupt-style alerts

T5808 SOUNDWIRE MICROPHONE

The T5808 is a SoundWire v1.1 fully compatible microphone. It connects directly to the SoundWire bus without the need for an intermediary SoundWire ADC or Codec, as shown in the figure below. The T5808 is configured as a SoundWire slave, where the Application Processor operates as the SoundWire master, with the ability to control the mic and access its Payload data through the SoundWire data stream.

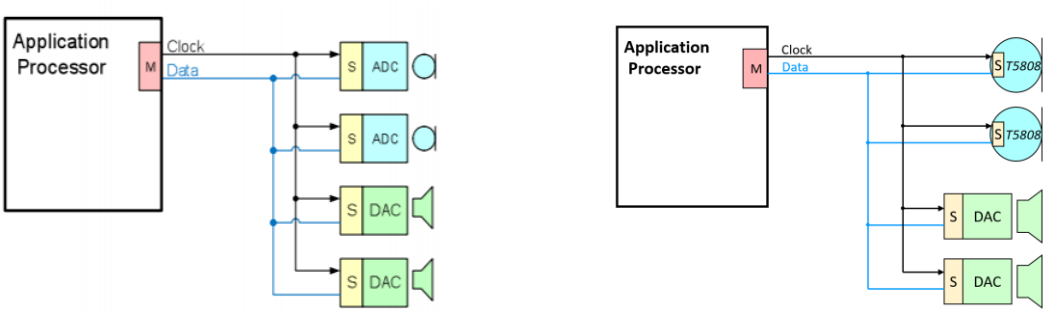

Figure 5. MIPI Example Microphone Topology (left) includes SoundWire ADC. T5808 digital mic with integrated SoundWire Slave functionality connects directly to the SoundWire bus without need for ADC (right).

The audio captured by the T5808 is a low latency PDM bitstream which is transmitted in the Payload of the SoundWire data stream. The T5808 can transmit data from both of its dataports, High Quality Mode and Low Power Listen Mode, simultaneously in the same Payload. This means the SoundWire bus can contain data from multiple T5808 dataports across multiple T5808 microphones, as well as data from other SoundWire devices on the same bus. The T5808 has 7 unique device ID (IDSEL) configurations, allowing connection of up to 7 T5808 SoundWire Microphone Slaves on a single SoundWire bus.

T5808 SoundWire features:

- SoundWire v1.1 slave
- Basic PHY device
- 1.8V signal support
- 7 unique microphones on the system

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ATTACHING TO SOUNDWIRE AND TRANSMITTING AUDIO

In order to transmit audio on the SoundWire bus, the T5808 needs to be established (attached) as a SoundWire slave on the bus, set up a data port and then start sending audio data on the data port. This involves transition across three defined modes in the SoundWire protocol:

- 3-1 Sync&Eumeration
- 1-4 Idle1
- 1-1 High Quality OR 1-2 Low Power Listen

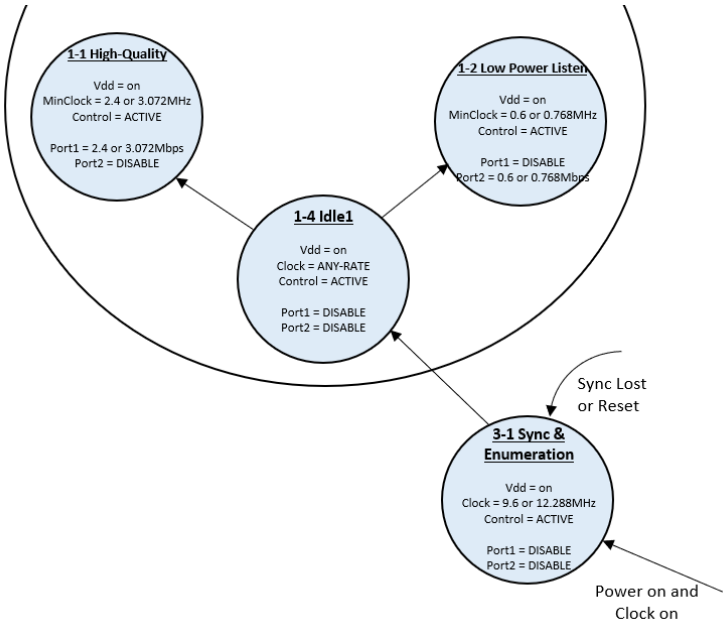

Figure 6. State transitions during start up

SYNC AND ENUMERATION

The T5808 is established as a slave on the SoundWire bus in the Sync And Enumeration mode. On entering the mode the following conditions exist:

- Vdd is on
- SoundWire CLK is on
- T5808 is not attached
- SoundWire has not enumerated the device
- Audio channels are disabled

The T5808 attaches itself as a SoundWire slave by:

- Frame Synchronization: It syncs with the control word within the control portion of the frame with the default device id = 0.
- Slave Enumeration: The master gives it a unique device id to distinguish from the other slaves on the bus.

IDLE1

After enumeration has been successfully carried out the microphone enters Idle1 mode. On entering the mode the following conditions exist:

- Vdd is on
- SoundWire CLK is on
- T5808 is attached
- SoundWire has enumerated the device
- Audio channels are disabled

Before audio data can be sent on the SoundWire bus, a Data Port needs to be set up on the device. A Data Port is a subset of a device that is either a source or sink of one Payload Stream on the SoundWire bus. On the T5808 there are two Data Ports

implemented - Data Port 1 and Data Port 2, for High Quality and Low Power Listen modes respectively. The Data Port has to be configured with the necessary information to describe how the Payload data is organized within a SoundWire frame. This information includes:

- Data Type
- Sample Length
- Sample Interval
- HStart and HStop
- Offset
- Word Length

TRANSMITTING AUDIO (HQM OR LPLM)

When a Data Port has been enabled (Data Port 1 or 2), the mic exits Idle1 mode and enters HQM or LPLM (depending on which is selected) and the audio data captured by the microphone will become active on the SoundWire data bus in the form of a PDM bitstream. The data rate of the bitstream will be determined by the SoundWire clock and the Sample Interval as outlined in the *Frame Structure* section. For HQM this is 2.4Mbps or 3.072Mbps, and for LPLM it is 0.6Mbps or 0.768Mbps. It is possible to leave HQM or LPLM and go back into Idle1 mode at any time.

The HQM and LPLM, and therefore Data Ports 1 and 2, can both be active at the same time in Concurrent mode. However either one of HQM or LPLM have to be established first, before the other mode is added. When in Concurrent mode, it is possible to leave and go back to either HQM or LPLM. It is also possible in Concurrent mode to go directly to Idle1 mode without having to transition to HQM or LPLM first.

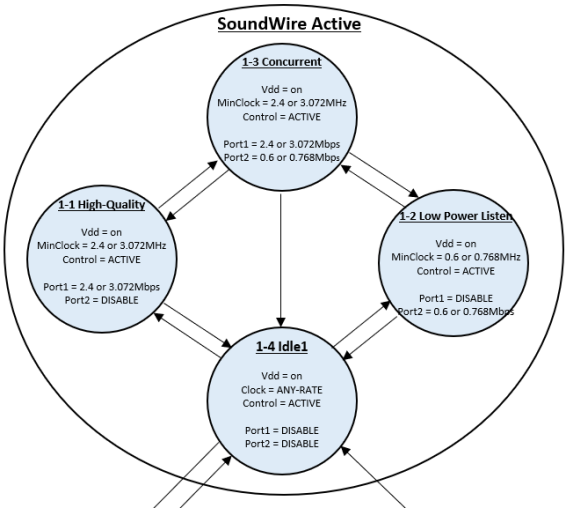

Figure 7. State transition options when the Data Port has been established and the audio stream is up and running

CONCURRENT MODE

In Concurrent Mode the microphone simultaneously outputs HQM and LPLM audio streams on Data Port 1 and Data Port 2 respectively. It can be used to minimize interruption in transitioning from LPLM to HQM and back to LPLM again, by operating as an intermediate mode. By allowing the datastreams to overlap, the SoundWire Master can extract each data stream and stitch together a single uninterrupted audio stream. Concurrent Mode can also be used to provide independent audio streams where two simultaneous applications need LPLM and HQM respectively. Concurrent mode is enabled by the SoundWire capability to output multiple audio data streams at different data rates.

TABLE 14. AVAILABLE MODES AND DATA RATES

MODE NAME	MODE NUMBER	PORT 1	PORT 2	PDM RATE
High Quality	1-1	Enabled	Disabled	2.4Mbps, 3.072Mbps
Low Power Listen	1-2	Disabled	Enabled	0.6Mbps, 0.768Mbps
Concurrent	1-3	Enabled	Enabled	0.6/2.4Mbps or 0.768/3.072Mbps

FRAME STRUCTURE

The SoundWire bitstream is a continuous stream of bits encoded using the modified-NRZI scheme, but for organizational purposes it is conceptually divided into a repetive sequence of bits to form a frame structure. This section focuses on the organization of the frame structure in order to achieve the desired SoundWire Clock, Frame Size and audio Data Rate. Note the T5808 can send and receive Control data in the data frame but it only sends Payload data as it since it is an audio input device to the Master.

The frame is constructed as a two dimensional array of bit slots, with 48 to 256 rows and 2 to 16 columns. The Control data is always contained in the Control Word which is the first 48 rows of the first column. The number of rows and columns is configurable to provide flexibility in creating an efficient data frame to multiplex data from multiple sources.

Some examples of a 48x2 frame are shown below. It shows the Control Word contained in row 0-47, col 0, per the MIPI spec. The Payload data is contained in row 0-47, col1, is generated by the T5808, ID=0, DataPort=1 (High Quality Mode) which is 2.4Mbit PDM data. The three examples show how the same Payload data (2.4Mbit PDM) is transmitted over different SoundWire clocks 2.4MHz, 4.8MHz and 9.6MHz, while the Frame Size remains constant at 96 bits and the Frame Rate scales accordingly. The Frame Rate can be calculated from the SoundWire Clock and the Frame Size:

Frame Rate = SWCLK*2/Frame Size

The sample interval of the PDM bitstream also scales with the SoundWire Clock and Frame Rate:

Sample Interval = SWCLK*2/PDM Data Rate

(Note: Sample Interval must be greater than 1 to allow for Control Word bits)

In the examples below, the Frame Rate increases from 50kHz to 100kHz to 200kHz as SoundWire Clock increases from 2.4Mhz, 4.8MHz and 9.6MHz. Likewise the Sample Interval Increases from 2 to 4 to 8 to keep the PDM data rate constant. By increasing the SoundWire clock rate (and sample interval), more unused data bit slots become available for other bitstreams to use.

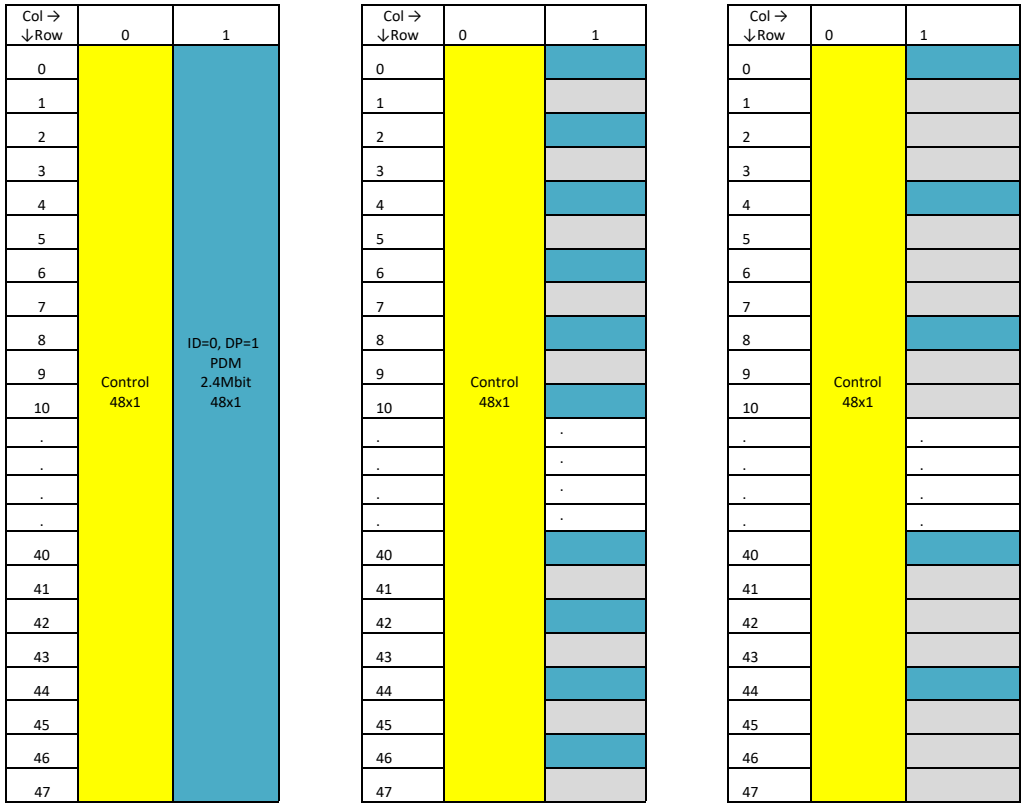

Figure 8. Comparison of different Sample Interval and Frame Rate combinations to achieve 2.4Mbps PDM Payload data

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The SoundWire clock should be fast enough to run the highest desired data rate for the bitstream within the Payload. For PDM data at 3.072, 2.4, 0.768 and 0.6Mbps. See Table 15 below for more details.

TABLE 15. AVAILABLE CLOCK AND DATA RATE COMBINATIONS

	Data Port 1		Data Port 2	
SoundWire CLK	PDM Data Rate	Sample Interval	PDM Data Rate	Sample Interval
12.288MHz	3.072Mbps	8	0.768Mbps	32
9.600MHz	2.400Mbps	8	0.600Mbps	32
6.144MHz	3.072Mbps	4	0.768Mbps	16
4.800MHz	2.400Mbps	4	0.600Mbps	16
3.072Mhz	3.072Mbps	2	0.768Mbps	8
2.400MHz	2.400Mbps	2	0.600Mbps	8
1.536MHz	Min 2.4Mbps	N/A	0.768Mbps	4
1.200MHz	Min 2.4Mbps	N/A	0.600Mbps	4
0.768MHz	Min 2.4Mbps	N/A	0.768Mbps	2
0.600MHz	Min 2.4Mbps	N/A	0.600Mbps	2

Greyed out cells are not valid combinations of SoundWire CLK and Data Port PDM data rates

A larger frame size will also increase the number of available data bits without changing the SoundWire clock rate. The Frame Rate will scale accordingly as shown below:

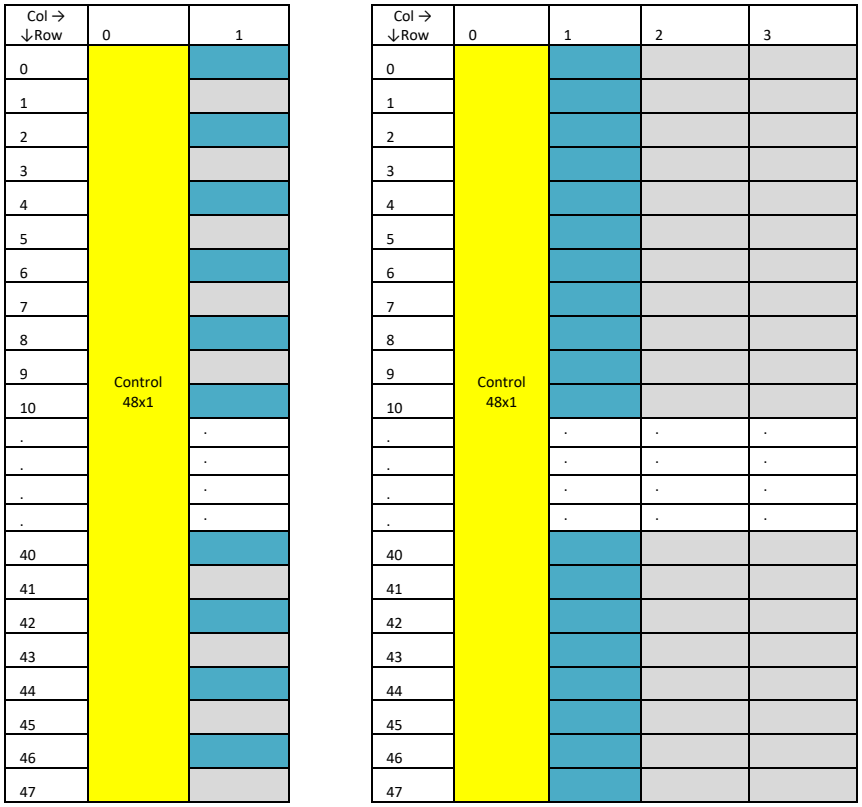

Figure 9. Comparison of different Frame Shape and Frame Rate combinations to achieve 2.4Mbps PDM Payload data

CONTROL WORD

In a similar fashion to the Frame structure, the Control data bits are conceptually organized into a Control Word of 48 bit data. The Control Word is not a continuous sequence of bits since it is interleaved by Payload data, however a word is an effective concept of organizing the control data. The 48 bits in the Control Word are assigned into the following categories:

- Control bits (20) from the Master that keep all interfaces synchronized to the Frame structure
- Command bits (28) from the Master or Monitor with corresponding response bits from the Slave or Master

Within the Command bits are bits which determine the device address, dataport and register for a specific command. SoundWire can write to all devices on the bus, individual device types on the bus or individual devices on the bus.

SoundWire provides a DeviceID[47:0] in the SCP_DevID_0 to SCP_DevID_5 registers that is read by the SoundWireMaster to identify the connected SoundWire slave device. The SoundWire slave DeviceID bits contains bit fields for:

- SoundWire Version (1.1 on this device)[47:44]
- Manufacturer ID [39:32]
- Part ID [23:16]
- Unique ID [43:40]

These fields are fixed except for the slave Unique ID which is pin configurable via the IDSEL pin and has seven possible combinations as shown in Table 7.

SOUNDWIRE REGISTER MAP

The SoundWire register map contains address blocks for the control port and the data ports. On T5818 the base address of the register is defined by whether it is Control Port, DataPort 1 or DataPort 2 as shown in the Table 16 below:

TABLE 16. ADDRESS RANGES FOR EACH DATA PORT

Base Address Range	Port Name	Prefix for Register Name	Notes
0x00000000 – 0x000000FF	Control Port	SCP_	Control and status functions common to the whole Device.
0x00000100 – 0x000001FF	Data Port 1	DP1_	Control and status functions specific to Data Port 1
0x00000200 – 0x000002FF	Data Port 2	DP2_	Control and status functions specific to Data Port 2

The register read/write is based on the base address shown above, along with the register specific offset as shown in Table 17, Table 18 and Table 19. The offset may have two options if it is banked for Bank 0 or Bank 1. Banks of Registers are used as a mechanism to make seamless changes to operation when those changes involve updating parameters in several registers in a device, or registers in several devices.

For detailed register and bit field descriptions, reference the full MIPI SoundWire® Specification (Version 1.1). T5808 uses a simplified data port therefore there are certain optional registers and the accompanying transport features are not implemented.

TABLE 17. SOUNDWIRE REGISTER ADDRESS MAP

Base Address = 0x00000000		**Slave Control Port Register Map**		
Bank Type / Address Offset		**Name**	**Access**	**Notes**
Non-Banked				
+ 0x00 – 0x3F		*Reserved*	None	Optional Data Port 0 not implemented
+ 0x40		SCP_IntStat_1	RO	
+ 0x40		SCP_IntClear_1	WO	
+ 0x41		SCP_IntMask_1	RW	
+ 0x42		SCP_IntStat_2	RO	
+ 0x43		SCP_IntStat_3	RO	
+ 0x44		SCP_Ctrl	WO	
+ 0x44		SCP_Stat	RO	
+ 0x45		SCP_SystemCtrl	RW	
+ 0x46		SCP_DevNumber	RW	
+ 0x47		SCP_High-PHY_Check	RW	Optional register not implemented
+ 0x48		SCP_AddrPage1	RW	Optional register not implemented
+ 0x49		SCP_AddrPage2	RW	Optional register not implemented
+ 0x4A		SCP_KeeperEn	RW	
+ 0x4B		SCP_BankDelay	RW	Optional register not implemented
+ 0x4C – 0x4E		*Reserved*	None	
+ 0x4F		SCP_TestMode	WO	Optional register not implemented
+ 0x50		SCP_DevId_0	RO	
+ 0x51		SCP_DevId_1	RO	
+ 0x52		SCP_DevId_2	RO	
+ 0x53		SCP_DevId_3	RO	
+ 0x54		SCP_DevId_4	RO	
+ 0x55		SCP_DevId_5	RO	
+ 0x56 – 0x5F		*Reserved*	*None*	
Bank 0	**Bank 1**			
+ 0x60	+ 0x70	SCP_FrameCtrl	WO	
+ 0x61	+ 0x71	SCP_NextFrame	WO	Optional registers not implemented
+ 0x62 – 0x6F	+ 0x72 – 0x7F	*Reserved*	None	
Non-Banked				
+ 0x80 – 0xFF		*Reserved*	None	
Base Address = 0x00000100 **Base Address = 0x00000200**		**Data Port 1 Register Map** **Data Port 2 Register Map** **Registers referenced as DP*n*, where *n* = 1 or 2**		
Bank Type / Address Offset		**Name**	**Access**	**Notes**
Non-Banked				
+ 0x00		DP*n*_IntStat	RO	
+ 0x00		DP*n*_IntClear	WO	
+ 0x01		DP*n*_IntMask	RW	
+ 0x02		DP*n*_PortCtrl	RW	
+ 0x03		DP*n*_BlockCtrl1	RW	
+ 0x04		DP*n*_PrepareStatus	RO	Feature not implemented (register can be read)
+ 0x05		DP*n*_PrepareCtrl	RW	Feature not implemented Write response – 'Command Ignored' Read response – ACK=1, data = 0x3F
+ 0x06 – 0x1F		*Reserved*	None	
Bank 0	**Bank 1**			
+ 0x20	+ 0x30	DP*n*_ChannelEn	RW	
+ 0x21	+ 0x31	DP*n*_BlockCtrl2	RW	Not Required in Simplified Data Port
+ 0x22	+ 0x32	DP*n*_SampleCtrl1	RW	

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+ 0x23	+ 0x33	DP*n*_SampleCtrl2	RW	Not Required in Simplified Data Port
+ 0x24	+ 0x34	DP*n*_OffsetCtrl1	RW	
+ 0x25	+ 0x35	DP*n*_OffsetCtrl2	RW	Not Required in Simplified Data Port
+ 0x26	+ 0x36	DP*n*_HCtrl	RW	Not Required in Simplified Data Port
+ 0x27	+ 0x37	DP*n*_BlockCtrl3	RW	Not Required in Simplified Data Port
+ 0x28	+ 0x38	DP*n*_LaneCtrl	RW	Conditional per multi-lane
+ 0x29 – 0x2F	+ 0x39 – 0x3F	*Reserved*	None	
Non-Banked				
+ 0x40 – 0xFF		*Reserved*	None	
Base Address = 0x00000300		**Data Ports 3 to 14 Register Map**		
+ 0x000 – 0xBFF		*Reserved*	None	Ports 3 to 14 are not implemented
Base Address = 0x00000F00		**All Payload Ports Register Address Aliases**		
Bank Type / Address Offset		**Name**	**Access**	**Notes**
Non-Banked				
+ 0x00		DP_All_P_IntStat	RO	
+ 0x00		DP_All_P_IntClear	WO	
+ 0x01		DP_All_P_IntMask	RW	
+ 0x02		DP_All_P_PortCtrl	RW	
+ 0x03		DP_All_P_BlockCtrl1	RW	
+ 0x04		DP_All_P_PrepareStatus	RO	
+ 0x05		DP_All_P_PrepareCtrl	RW	
+ 0x06 – 0x1F		*Reserved*	None	
Bank 0	**Bank 1**			
+ 0x20	+ 0x30	DP_All_P_ChannelEn	RW	
+ 0x21	+ 0x31	DP_All_P_BlockCtrl2	RW	Not Required in Simplified Data Port
+ 0x22	+ 0x32	DP_All_P_SampleCtrl1	RW	
+ 0x23	+ 0x33	DP_All_P_SampleCtrl2	RW	Not Required in Simplified Data Port
+ 0x24	+ 0x34	DP_All_P_OffsetCtrl1	RW	
+ 0x25	+ 0x35	DP_All_P_OffsetCtrl2	RW	Not Required in Simplified Data Port
+ 0x26	+ 0x36	DP_All_P_HCtrl	RW	Not Required in Simplified Data Port
+ 0x27	+ 0x37	DP_All_P_BlockCtrl3	RW	Not Required in Simplified Data Port
+ 0x28	+ 0x38	DP_All_P_LaneCtrl	RW	Conditional per multi-lane
+ 0x29 – 0x2F	+ 0x39 – 0x3F	*Reserved*	None	
Base Address = 0x00003000		**Implementation Defined Registers (DDC)**		
Bank Type / Address Offset		**Name**	**Access**	**Notes**
Non-Banked				
+ 0x00		DDC_Overall_Capability_List	RO	
+ 0x01		DDC_Mic_Directivity	RO	
+ 0x02		DDC_Mic_Min_Sensitivity	RO	
+ 0x03		DDC_Mic_Max_Sensitivity	RO	
+ 0x04		DDC_Mic_AOP	RO	
+ 0x05		DDC_MIC_MAX_AOP	RO	
+ 0x06		DDC_Mic_Clock_Sources	RO	
+ 0x07		DDC_Mic_Change_Audio_Rate	RO	
+ 0x08		DDC_Mic_Min_HPF_Freq	RO	
+ 0x09		DDC_Mic_Max_HPF_Freq	RO	
+ 0x0A		DDC_Mic_Ultrasound_Rates	RO	
+ 0x0B		IO PAD Control	RW	

SOUNDWIRE REGISTER DEFINITIONS

TABLE 18. SLAVE CONTROL PORT REGISTERS

ScP_INTSTAT_1 / SCP_INTCLEAR_1 **ADDRESS BASE + 0X40**

7	6	5	4	3	2	1	0	Default
-	-	Port2 Cascade	Port1 Cascade	-	-	Bus Clash	Parity	
RO						R/W1C	R/W1C	
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:6	-	Reserved
5:4	Portn Cascade (n=1 or 2)	Indicate whether at least one unmasked interrupt condition is set in the corresponding DPn interrupt status register. Cleared by clearing the the source in the appropriate DPn interrupt status register. 0 – No unmasked interrupt condion exists 1 – At least one unmasked interrupt condition exists
3	-	Reserved
2	ImpDef1	not implemented
1	Bus Clash	Indicates whether an interrupt is pending due to detection of a bus clash condition. Will generate an interrupt if the corresponding mask bit is set. Writing a ‘1’ to this bit position clears this condition along with the associated interrupt. 0 – No bus clash detected 1 – Bus clash detected
0	Parity	Indicates whether a parity error has been detected on the bus. Will generate an interrupt if the the corresponding mask bit is set. Writing a ‘1’ to this bit position clears this condition along with the associated interrupt 0 – No parity error detected 1 – Parity error detected

ScP_INTMASK_1 **ADDRESS BASE + 0X41**

7	6	5	4	3	2	1	0	Default
					-	Mask Bus Clash	Mask Parity	
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:3	-	Reserved
2	Mask ImpDef1	not used because ImpDef1 is not implemented
1	Mask Bus Clash	Determines whether a bus clash event generates an interrupt 0 – Bus clash does not generate an interrrupt 1 – Bus clash generates an interrupt
0	Mask Parity	Determines whether a parity error event generates an interrupt 0 – Parity error does not generate an interrupt 1 – Parity error generates an interrupt

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ScP_INTSTAT_2 **ADDRESS BASE + 0X42**

7	6	5	4	3	2	1	0	Default
						-	-	
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	-	Reserved Always reads back a '0'

ScP_INTSTAT_3 **ADDRESS BASE + 0X43**

7	6	5	4	3	2	1	0	Default
						-	-	
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	-	Reserved Always reads back a '0'

ScP_Ctrl / SCP_Stat **Address Base + 0x44**

7	6	5	4	3	2	1	0	Default
Force Reset	Current Bank	High-PHY_ NotOK				ClockStop Now	ClockStop_ NotFinished	
WO	RO	RO				WO	RO	
0	0	1	0	0	0	0	0	0x20

Bits	Name	Function
7	Force Reset	Used to initiate a device reset 0 – No action 1 – Force a device reset
6	CurrentBank	Identifies the current register bank 0 – Current register bank is Bank 0 1 – Current register bank is Bank 1
5	High-PHY_NotOK	High-PHY option not supported Always reads back a '1'
4:2	-	Reserved
1	ClockStopNow	Informs the slave that the master is stopping the SoundWire clock at the end of the next frame 0 – Normal operation 1 – SoundWire clock will stop at the end of the next frame
0	ClockStop_NotFinished	Indicates whether the device has completed any required shutdown sequence and is ready for SoundWire master to stop the SoundWire clock via asserting ClockStopNow 0 – Device is ready for a clock stop event 1 – Device not finished with necessary clock stop state transitions

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ScP_SYSTEMCTRL **ADDRESS BASE + 0X45**

7	6	5	4	3	2	1	0	Default
			High-PHY_ Select	WakeUP Enable	ClockStop Mode		ClockStop Prepare	
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:5	-	Reserved
4	High-PHY_Select	Option not supported Always reads back a '0'
3	WakeUpEnable	Feature not supported
2	ClockStopMode	It selects between ClockStopMode0 and ClockStopMode1
1	-	Reserved
0	ClockStopPrepare	Feature not supported

ScP_DEVNUMBER **ADDRESS BASE + 0X46**

7	6	5	4	3	2	1	0	Default
		Group ID		Device Number				
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:6	-	Reserved
5:4	Group ID	Indicates whether the device is addressable by a group alias in addition to being addressed by commands targeted to its own device number 00 – Normal, not in a shared group 01 – Group 12. The device responds to any commands directed to DevAddr = 12 10 – Group 13. The device responds to any commands directed to DevAddr = 13 11 – Reserved
3:0	Device Number	Indicates the specific device number assigned to the device. This value is compared against the DevAddr field in the control world to determine if the command is targeted to this device.

ScP_KEEPEREN **ADDRESS BASE + 0X4A**

7	6	5	4	3	2	1	0	Default
KeepEN7	KeepEN6	KeepEN5	KeepEN4	KeepEN3	KeepEN2	KeepEN1	Reserved	
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:1	KeepENn, n=7:1	Unused Hardwired to '0'
0	Reserved	Bus keeper is permanently disabled (single lane device) Hardwired to '0'

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ScP_DEVID_0 **ADDRESS BASE + 0X50**

7	6	5	4	3	2	1	0	Default
SoundWire Version				Unique ID				
RO								
0	0	1	0	X	X	X	X	0x2X

Bits	Name	Function
7:4	SoundWire Version	Indicates which version of the MIPI SoundWire specification is supported by the device b0010 – SoundWire version 1.1 These bits constitute DeviceID [47:44]
3:0	Unique ID	Uniquely identifies the device if there are multiple instances of this device on the SoundWire bus. See Sync & Enumeration section for operational details. These bits constitute DeviceID [43:40]

ScP_DEVID_1 **ADDRESS BASE + 0X51**

7	6	5	4	3	2	1	0	Default
Manufacturer ID [15:8]								
RO								
0	0	0	0	0	0	1	0	0x02

Bits	Name	Function
7:0	Manufacturer ID	Upper byte of the MIPI assigned manufacturers device ID These bits constitute DeviceID [39:32]. TDK's manufacturer id is 0x0235

ScP_DEVID_2 **ADDRESS BASE + 0X52**

7	6	5	4	3	2	1	0	Default
Manufacturer ID [7:0]								
RO								
0	0	1	1	0	1	0	1	0x35

Bits	Name	Function
7:0	Manufacturer ID	Lower byte of the MIPI assigned manufacturers device ID. These bits constitute DeviceID [31:24]. TDK's manufacturer ID is 0x0235

ScP_DEVID_3 **ADDRESS BASE + 0X53**

7	6	5	4	3	2	1	0	Default
Part ID [15:8]								
RO								
0	1	0	1	1	0	0	0	0x58

Bits	Name	Function
7:0	Part ID	Upper byte of the Part ID These bits constitute DeviceID [23:16]. Part ID for this microphone is 0x5808

ScP_DEVID_4 **ADDRESS BASE + 0X54**

7	6	5	4	3	2	1	0	Default
Part ID [7:0]								
RO								
0	0	0	0	1	0	0	0	0x08

Bits	Name	Function
7:0	Part ID	Lower byte of the Part ID. These bits constitute DeviceID [15:8]. Part ID for this microphone is 0x5808

ScP_DEVID_5 **ADDRESS BASE + 0X55**

7	6	5	4	3	2	1	0	Default
Class								
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	Class	MIPI defined class encoding These bits constitute DeviceID [7:0]. 0x00 indicates no further class information

ScP_FRAMECTRL

BANK 0 - ADDRESS BASE + 0X60
BANK 1 - ADDRESS BASE + 0X70

7	6	5	4	3	2	1	0	Default
Row Control					Column Control			
WO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:3	Row Control	Determines the number of rows in the frame Row Control / Number of Rows / Row Control / Number of Rows / Row Control / Number of Rows / Row Control / Number of Rows 0x00 / 48 / 0x08 / 96 / 0x10 / 192 / 0x18-1F / Reserved 0x01 / 50 / 0x09 / 100 / 0x11 / 200 0x02 / 60 / 0x0A / 120 / 0x12 / 240 0x03 / 64 / 0x0B / 128 / 0x13 / 256 0x04 / 75 / 0x0C / 150 / 0x14 / 72 0x05 / 80 / 0x0D / 160 / 0x15 / 144 0x06 / 125 / 0x0E / 250 / 0x16 / 90 0x07 / 147 / 0x0F / Reserved / 0x17 / 180 Automatically updated after frame size is detected upon completion of synchronization phase. Writes to this register update the frame shape at the end of the next frame. Writes to the inactive bank version of this register cause a bank switch at the end of the next frame.
2:0	Column Control	Determines the number of columns in the frame Column Control / Number of Columns / Column Control / Number of Columns 0x0 / 2 / 0x4 / 10 0x1 / 4 / 0x5 / 12 0x2 / 6 / 0x6 / 14 0x3 / 8 / 0x7 / 16 Automatically updated after frame size is detected upon completion of synchronization phase. Writes to this register update the frame shape at the end of the next frame. Writes to the inactive bank version of this register cause a bank switch at the end of the next frame.

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TABLE 19. SLAVE DATA PORT 1-2 REGISTERS

Dp*N*_INTSTAT / DP*N*_INTCLEAR **ADDRESS BASE + 0X00**

7	6	5	4	3	2	1	0	Default
-	-	-	-	-	-	Port Ready Stat	Test Fail Stat	
RO						R/W1C	R/W1C	
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:2	-	Reserved or Unused Hardwired to ‘0’
1	Port Ready Stat	Not implemented Hardwired to ‘0’
0	Test Fail Stat	Not implemented Hardwired to ‘0’

Dp*n*_IntMask **Address Base + 0x01**

7	6	5	4	3	2	1	0	Default
IntMask ImpDef3	IntMask ImpDef2	IntMask ImpDef1	-	-	-	IntMask Port Ready Mask	IntMask Test Fail Mask	
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7	IntMaskImpDef3	Not implemented Hardwired to ‘0’
6	IntMaskImpDef2	Not implemented Hardwired to ‘0’
5	IntMaskImpDef1	Not implemented Hardwired to ‘0’
4-2	-	Reserved
1	Port Ready Mask	Not implemented Hardwired to ‘0’
0	Test Fail Mask	Controls whether the corresponding status bit is able to generate an interrupt 0 – Disable corresponding status bit from generating an interrupt 1 – Enable corresponding status bit to generate an interrupt

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Dp*n*_PortCtrl **Address Base + 0x02**

7	6	5	4	3	2	1	0	Default
-	-	Port Direction	Next InvertBank	PortDataMode		PortFlowMode		
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:6	-	Reserved
5	PortDirection	Always TX Hardwired to '0'
4	NextInvertBank	Controls which DP bank is in use (does not apply to SCP banked registers) 0 – Use the bank targeted in the control word 1 – Use the opposite bank than what is targeted in the control word. Changes takes effect on the next frame
3:2	PortDataMode	Determine the port Payload data mode Decode: Mode Type 00: Normal 01: PRBS Test 10: Static 0 11: Static 1
1:0	PortFlowMode	Not Implemented Hardwire to '00'

Dp*n*_BlockCtrl1 **Address Base + 0x03**

7	6	5	4	3	2	1	0	Default
-	-	-	-	-	Word Length			
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:3	-	Reserved
2:0	Word Length	Determines the Payload length in bits. Must be programmed to 0 otherwise unpredictable behavior can occur

Dp*n*_ChannelEn **Bank 0 - Address Base + 0x20**
Bank 1 - Address Base + 0x30

7	6	5	4	3	2	1	0	Default
-	-	-	-	-	-	-	EnChannel1	
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:1	-	Reserved
0	EnChannel1	Controls whether the data port channel 1 is enabled or disabled 0 – Channel disabled 1 – Channel enabled Gets automatically cleared upon internal reset conditions and frame synchronization loss

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Dp*n*_BlockCtrl2 **Bank 0 - Address Base + 0x21**
Bank 1 - Address Base + 0x31

7	6	5	4	3	2	1	0	Default
						BlockGroupControl		
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:2	-	Reserved
1:0	BlockGroupControl	Not Supported. It should be kept fixed to '00'

Dp*n*_SampleCtrl1 **Bank 0 - Address Base + 0x22**
Bank 1 - Address Base + 0x32

7	6	5	4	3	2	1	0	Default
SampleIntervalLow								
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	SampleIntervalLow	Lower byte of the sample interval. Formula for sample interval: Sample Interval = SampleIntervalLow + (256*SampleIntervalHigh) + 1 For DP1 – Maximum SampleIntervalLow value = 0d7 (3 lsb's) For DP2 – Maximum SampleIntervalLow value = 0d31 (5 lsb's) Note: SampleIntervalHigh is hardwired to '0x00' for the T5808

Dp*n*_OffsetCtrl1 **Bank 0 - Address Base + 0x24**
Bank 1 - Address Base + 0x34

7	6	5	4	3	2	1	0	Default
Offset1								
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	Offset1	Determines the number of bitslots the Payload data is positioned from the start of the transport Payload window of the frame For DP1 – The allowable Offset1 values are 1 to 7. Determined by the ratio between the SoundWire clock and the internal PDM clock for DP1 For DP2 – The allowable Offset1 values are 1 to 31. Determined by the ratio between the SoundWire clock and the internal PDM clock for DP2 Note: Offset2 is hardwired to '0x00' for the T5808

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TABLE 20. DISCOVERABLE DEVICE CAPABILITY REGISTERS

DDC_Overall_Capability_List **Address Base + 0x00**

7	6	5	4	3	2	1	0	Default
		Mic_VAD	Mic_LPLM	Mic_HPF_ Adj	Mic_AOP_ Adj	Mic_SENS_ Adj	Mic_DIR_ Adj	
RO								
0	0	0	1	0	0	0	0	0x10

Bits	Name	Function	
7:6	-	Reserved	
5	Mic_VAD	Microphone voice actitvity detection.	Always reads back a ‘0’
4	Mic_LPLM	Microphone Low Power Listen mode support.	Always reads back a ‘1’
3	Mic_HPF_Adj	Microphone High Pass Filter adjustment.	Always reads back a ‘0’
2	Mic_AOP_Adj	Microphone AOP adjustment.	Always reads back a ‘0’
1	Mic_SENS_Adj	Microphone Sensitivity adjustment.	Always reads back a ‘0’
0	Mic_DIR_Adj	Microphone Directivity adjustment.	Always reads back a ‘0’

DDC_Mic_Directivity **Address Base + 0x01**

7	6	5	4	3	2	1	0	Default
		-	BiDir	Hyper Cardiod	Super Cardiod	Cardiod	OmniDir	
RO								
0	0	0	0	0	0	0	1	0x01

Bits	Name	Function	
7:5	-	Reserved	
4	BiDir	Bidirecational (Notch at 90°).	Always reads back a ‘0’
3	Hyper Cardiod	Hyper Cardiod (Notch at 110°).	Always reads back a ‘0’
2	Super Cardiod	Super Cardiod (Notch at 126°).	Always reads back a ‘0’
1	Cardiod	Cardiod (Notch at 180°).	Always reads back a ‘0’
0	OmniDir	Omnidirectional (Equal sensitivity from all angles).	Always reads back a ‘1’

DDC_Mic_Min_Sensitivity **Address Base + 0x02**

7	6	5	4	3	2	1	0	Default
Min_Sensitivity [7:0]								
RO								
1	0	1	0	0	1	0	0	0xA4

Bits	Name	Function
7:0	Min_Sensitivity	Reflects the minimum supported sensitivity value: 0xA4: idle, hqm and concurrent mode 0x68: lpm

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DDC_Mic_Max_Sensitivity **Address Base + 0x03**

7	6	5	4	3	2	1	0	Default
Max_Sensitivity [7:0]								
RO								
1	0	1	0	0	1	0	0	0xA4

Bits	Name	Function
7:0	Max_Sensitivity	Reflects the maximum supported sensitivity value: 0xA4: idle, hqm and concurrent mode 0x68: lpm

DDC_Mic_AOP **Address Base + 0x04**

7	6	5	4	3	2	1	0	Default
Mic_AOP [7:0]								
RO								
1	0	1	0	1	0	0	0	0xA4

Bits	Name	Function
7:0	Mic_AOP	Reflects the suppported AOP value: 0xA4: idle, hqm and concurrent mode 0x68: lpm

DDC_MIC_MAX_AOP **ADDRESS BASE + 0X05**

7	6	5	4	3	2	1	0	Default
Max_AOP [7:0]								
RO								
1	0	1	0	1	0	0	0	0xA4

Bits	Name	Function
7:0	Max_AOP	Reflects the maximum supported AOP value: 0xA4: idle, hqm and concurrent mode 0x68: lpm

DDC_MIC_CLOCK_SOURCES **ADDRESS BASE + 0X06**

7	6	5	4	3	2	1	0	Default
-	-	-	-	-	-	-	Clock_ Source	
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:1	-	Reserved
0	Clock_Source	Reflects what allowable clock sources can produce audio samples 0 – Only clock that can produce audio samples is the SoundWire bus clock

DDC_Mic_Change_Audio_Rate **Address Base + 0x07**

7	6	5	4	3	2	1	0	Default
-	-	-	-	-	-	-	Change_ Audio_Rate	
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:1	-	Reserved
0	Change_Audio_Rate	Reflects the microphone audio rate change capabilities 0 – Microphone audio rate remains constant as long as the channel is active

DDC_Mic_Min_HPF_Freq **Address Base + 0x08**

7	6	5	4	3	2	1	0	Default
Min_HPF_Freq [7:0]								
RO								
0	0	1	0	0	1	0	0	0x24

Bits	Name	Function
7:0	Min_HPF_Freq	Reflects the minimum value in Hz supported by the HPF, the -3dB point Fixed value of 36Hz in decimal

DDC_Mic_Max_HPF_Freq **Address Base + 0x09**

7	6	5	4	3	2	1	0	Default
Max_HPF_Freq [7:0]								
RO								
0	0	1	0	0	1	0	0	0x24

Bits	Name	Function
7:0	Max_HPF_Freq	Reflects the maximum value in Hz supported by the HPF, the -3dB point Fixed value of 36Hz in decimal

DDC_MIC_ULTRASOUND_RATES **ADDRESS BASE + 0X0A**

7	6	5	4	3	2	1	0	Default
Ultrasound Rate								
RO								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:0	Ultrasound rate	Ultrasound rates not support Hardwired to ‘0x00’

IO PAD Control **Address Base + 0x0B**

7	6	5	4	3	2	1	0	Default
dt_slew_rate_ctrl		dt_drive_strength_ctrl			dt_cap_load_ctrl			
RW								
0	0	0	0	0	0	0	0	0x00

Bits	Name	Function
7:6	dt_slew_rate_ctrl	Not used
5:3	dt_drive_strength_ctrl	Not used
2:0	dt_cap_load_ctrl	Selects the driving capability 000: Cload 30-66 pF (default) 001: Cload 2-11 pf 010: Cload 10-33 pf 011: Cload 30-66 pF Others values not used

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ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 21. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage (V_{DD})	−0.3 V to +1.98 V
Digital Pin Input Voltage	−0.3 V to V_{DD} + 0.3 V or 1.98 V, whichever is less
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	
Operating	−40°C to +85°C
Storage	−55°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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SOLDERING PROFILE

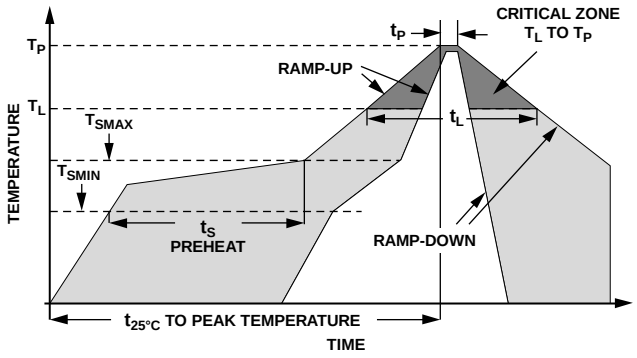

Figure 10. Recommended Soldering Profile Limits

TABLE 22. RECOMMENDED SOLDERING PROFILE*

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Maximum Temperature (T_{SMAX})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C +3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

**The reflow profile in Figure 10. is recommended for board manufacturing with TDK MEMS microphones. All microphones are also compatible with the J-STD-020 profile*

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

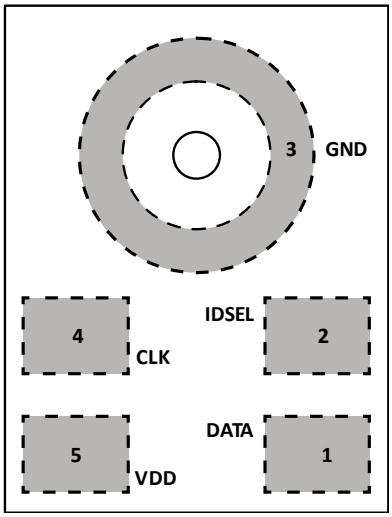

Figure 11. Pin Configuration (Top View, Terminal Side Down)

TABLE 23. PIN FUNCTION DESCRIPTIONS

PIN	NAME	FUNCTION
1	DATA	SoundWire Bi-directional Data Signal
2	IDSEL	Device Identification Input. Impedance of this pin is sensed during the enumeration phase to determine the microphone's unique identification bit field. Connect a resistor between this pin and GND (See Table 7 for operational description and a table of resistor values)
3	GND	Ground
4	CLK	SoundWire Clock Input to Microphone
5	VDD	Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 5 (VDD) and ground. Place the capacitor as close to Pin 5 as possible.

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TYPICAL PERFORMANCE CHARACTERISTICS

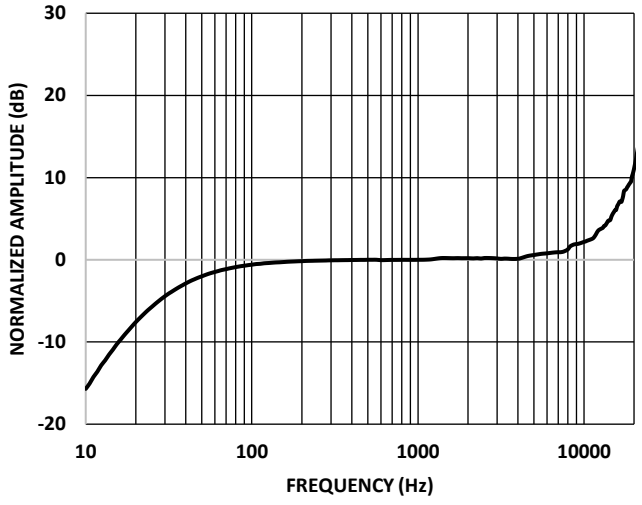

Figure 12. Typical Frequency Response

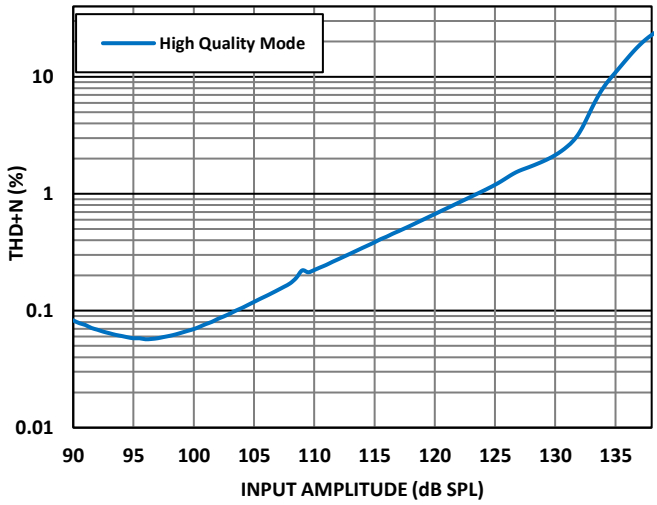

Figure 13. THD + N High Quality Mode

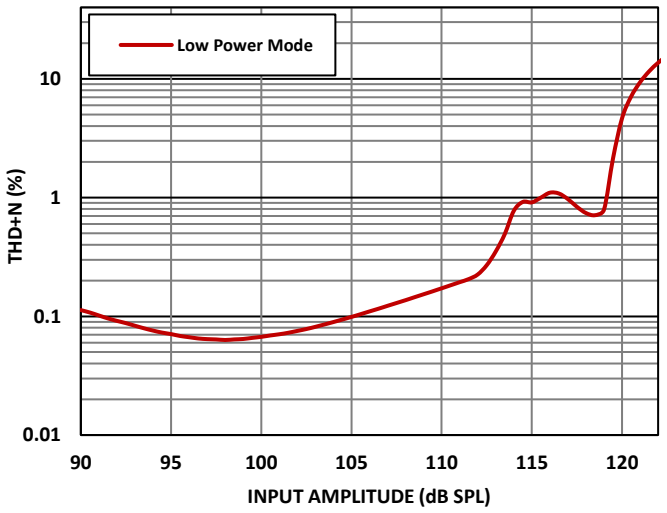

Figure 14. THD + N Low Power Mode

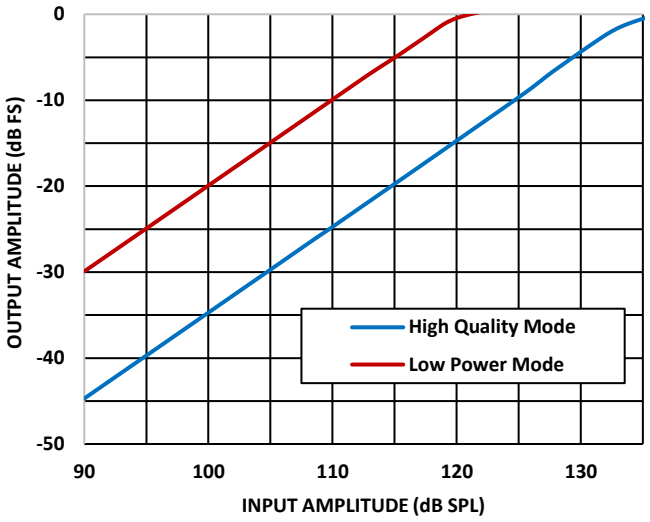

Figure 15. Linearity

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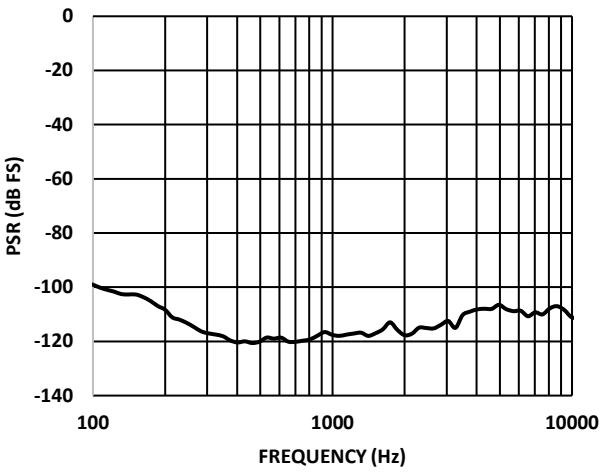

Figure 16. Power Supply Rejection (PSR) vs. Frequency, High Quality Mode

SUPPORTING DOCUMENTS

For additional information, see the following documents.

APPLICATION NOTES – GENERAL

AN-100: MEMS Microphone Handling and Assembly Guide
AN-1003: Recommendations for Mounting and Connecting the TDK, Bottom-Ported MEMS Microphones
AN-1112: Microphone Specifications Explained
AN-1124: Recommendations for Sealing TDK Bottom-Port MEMS Microphones from Dust and Liquid Ingress
AN-1140: Microphone Array Beamforming

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PCB DESIGN AND LAND PATTERN LAYOUT

The recommended PCB land pattern for the T5808 is a 1:1 ratio of the solder pads on the microphone package, as shown in Figure 17. Avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 18.

The response of the T5808 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.375 mm in diameter). A 0.5 mm to 1 mm diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.

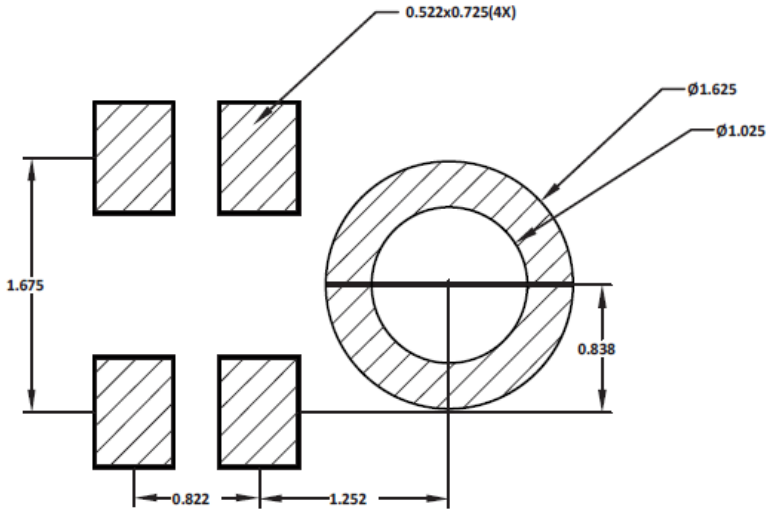

Figure 17. Recommended PCB Land Pattern Layout

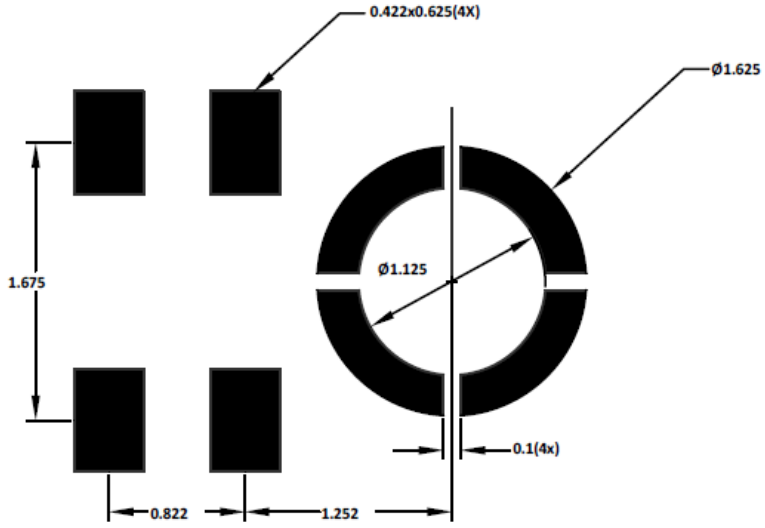

Figure 18. Suggested Solder Paste Stencil Pattern Layout

PCB MATERIAL AND THICKNESS

The T5808 can be mounted on either a rigid or flexible PCB. A microphone's lid can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality. The sound port can also be routed to the device housing through a port in a rubber boot. This boot should be designed to seal the connection between the microphone's lid and the rubber completely.

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HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the top of the package, the pickup tool should not be placed over the microphone port.
- Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 10 and Table 22.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

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OUTLINE DIMENSIONS

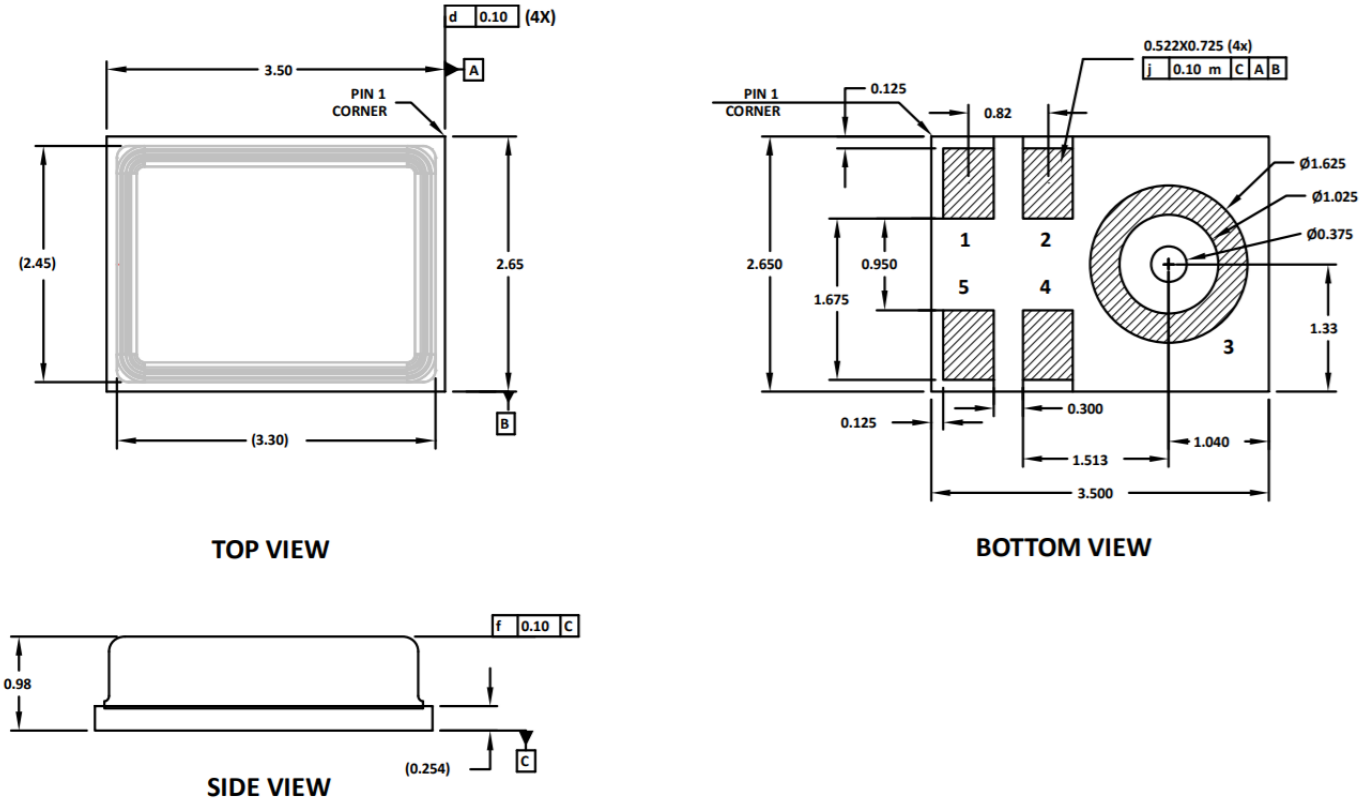

Figure 19: 5 Terminal Chip Array Small Outline No-Lead Cavity

3.50 mm × 2.65 mm × 0.98 mm Body (Dimensions shown in millimeters)

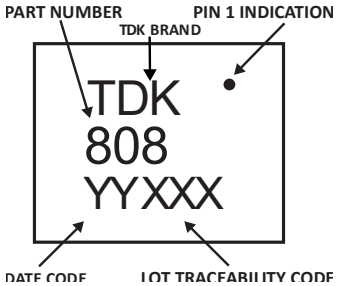

Figure 20. Package Marking Specification (Top View)

ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	QUANTITY	PACKAGING
MMICT5808-00-012	−40°C to +85°C	5-Terminal LGA_CAV	10,000	13” Tape and Reel

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REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
12/13/2019	1.0	Initial version
1/2/2020	1.1	Fixed typos
2/6/2020	1.2	Fixed typo ordering guide part name

COMPLIANCE DECLARATION DISCLAIMER

TDK believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. TDK subcontracts manufacturing, and the information contained herein is based on data received from vendors and suppliers, which has not been validated by TDK.