IAM-20685 Startup Procedure

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1 REFERENCE DOCUMENTS

- IAM-20685 Datasheet (DS-000182)
- IAM-20685 Safety Manual (DS-000342)

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2 OVERVIEW

The purpose of this Application Note is to describe the startup sequence performed by IAM-20685 and to highlight what user is expected to do during the startup and runtime.

3 DEVICE STARTUP

Startup sequence automatically begins when voltage on VDD pin reaches the minimum value stated in datasheet (namely, 3.0V for 3.3V supply range and 4.5V for 5V supply range), or after a Hard reset or a Soft reset.
The device shall automatically perform the operations sequence summarized in the following diagram.

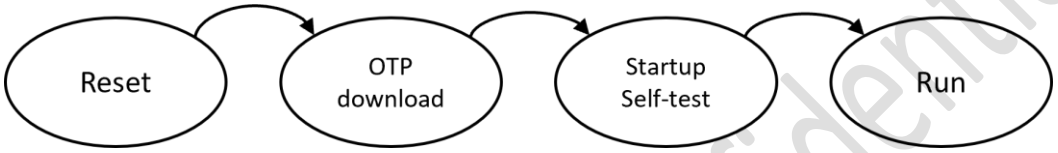

Figure 1. startup sequence macro-operations

During and after the sequence, the host is in charge of executing the safety related tasks included in SM101; details are provided in section 4.
Following figure, shows the startup sequence timing diagram.

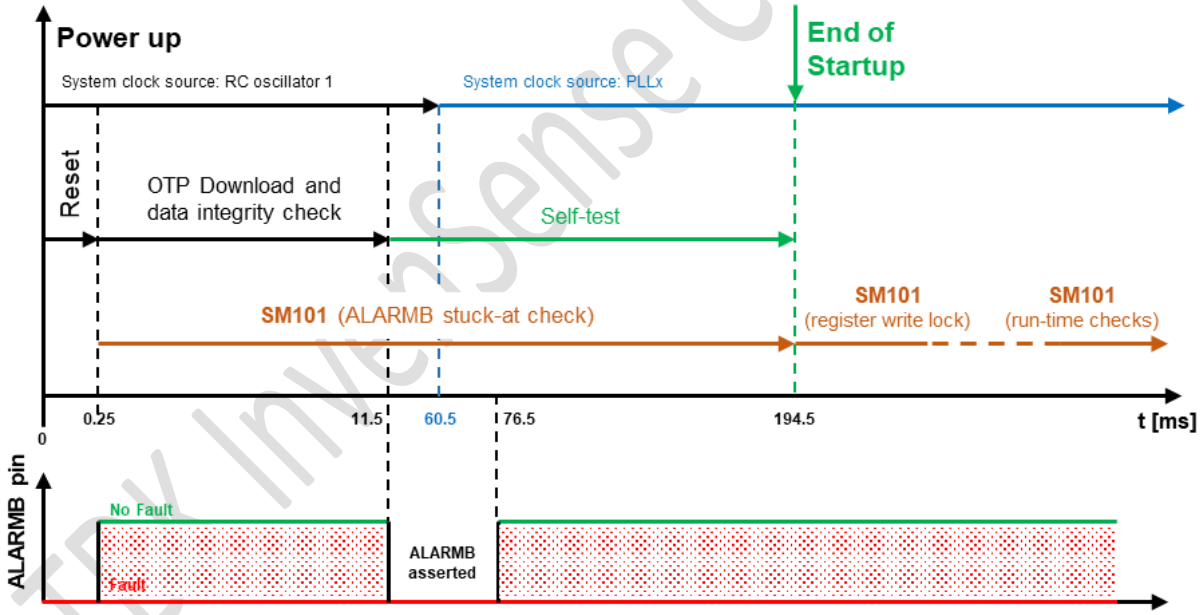

Figure 2. startup sequence timing diagram

NOTE: SPI access is forbidden for the entire duration of the startup sequence (200 ms).

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3.1. SEQUENCE STEPS DETAILS

3.1.1. Reset

IAM-20685 enters Reset state when either of the following events occurs:

- A Power on Reset, triggered by VDD level transition below VDD min value.
- A Hard reset, commanded by setting bit 2 in RESET_CONTROL register (bank 0, offset 0x18).
- A Soft reset, commanded by setting bit 1 in RESET_CONTROL register (bank 0, offset 0x18).
- Putting 0V on the pin RESETN for 30 ms or more will also trigger a hardware reset.

In the timing diagram of Figure 2, t=0 corresponds to the POR signal release. After POR is released, regulators are started up, bias currents for RC oscillators are provided and internal clock that shall be used in the first part of the startup sequence is estabilished.
In case of Soft reset, the startup sequence can be different from the one represented in Figure 1, for OTP download shall be executed only if *en_soft_reset_otp_load* (bank 2, address 0x0B, bit 3), is set to 1.
At the end of Reset phase, ALARMB pin is asserted at high level, to indicate a NO fault status.
System clock source in this phase is RC Oscillator 1.

3.1.2. OTP download

From t=256 µs, data from OTP is downloaded to functional registers; then, data integrity is checked by running SM26 (Correct Register Loading from OTP Check), which computes CRC of downloaded data and compares it with the one stored into OTP. Allow 11 ms for the entire process to complete.
During this phase, all SM are masked except for SM22 (Data Integrity Check) and SM26.
At the end of this phase, ALARMB pin is set to low level, as an indication of the completion of the phase.

3.1.3. Startup Self-test

When OTP download phase is completed, after a fixed time, system clock source switches from RC oscillator 1 to PLL; then, Self-test phase automatically begins. During this phase, the following Safety Mechanisms are run:

- SM16 - Accelerometers Self Test
- SM29 - AHB Matrix Check
- SM36 - Gyroscope DC Self Test

During the phase, ALARMB is asserted back to high level; at the end of SM36, if no alarms are detected, Startup sequence is completed, and the device is ready and functional.
The correct transitions of ALARMB pin during the startup phases, must be checked by the host, as described in section 4.1.

3.1.4. Run

The device has completed the startup sequence and is now in full operational mode; user can access registers through SPI. ALARMB level indicates the final status of the startup sequence (Fault or No Fault); in case of fault presence, checking alarm registers shall help pointing out the failure occurred during the startup.

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4 SAFETY MECHANISM SM101

SM101, also described in IAM-20685 datasheet and in Safety Manual, includes several Safety-related tasks, to be executed either during the startup sequence (in this phase, being SPI not available, the host will monitor ALARMB pin to check the correct outcome of the SM execution), or after the startup sequence (i.e. in "Run" state), with a periodicity at least equal to once every Fault Tolerant Time.
In case of unexpected behaviors (anomalies) or alarms, the transition to Safe State shall be initiated; a reset command could be sent by Host trying to recover it (or power-off/on), Transient failures (if any) will be cleared, while Permanent failures will not be impacted by reset.

4.1. TASK TO BE EXECUTED AT EACH POWER-UP

- [SM101.1] In order to check for potential stuck-at-1/0 on ALARMB, the host shall verify that the intended start-up sequence on ALARMB pin is correctly executed:
  - Rising Edge at T=0 (some hundreds of µs after power-on, depending on power-up ramp)
  - Falling Edge at T=10.8ms (in a time slot between 10.3ms and 11.3ms)
  - Rising Edge at T=79.4ms (in a time slot between 75.6ms and 83.2ms)

  Any deviation from that sequence of edges means an issue is present, is to be considered as an Alarm and managed after the startup sequence interval (200 ms) is expired.
- [SM101.3] After the startup sequence interval (200 ms), when SPI is available, SM30 is to be tested through the following error injections (the presence of errors will be flagged by the indicated alarm bits as well as by bits RS0=1 and RS1=1 in the MISO frame):
  - Sending a 32-bit SPI command with a corrupt CRC to generate a spi_crc alarm (BANK 0, Addr=0x15, bit 2)
  - Sending data over MOSI with an incorrect number of clock cycles to generate a spi_clkcnr alarm (BANK 0, Addr=0x15, bit 4)
- [SM101.11] **Register_Write_Lock** bit (BANK 0, Addr=0x19, bit 15) shall be set as last action of sensor initialization, after start-up. As a consequence of this action, register bank switch is no more effective and only BANK 0 is accessible.

4.2. TASKS TO BE EXECUTED RUN-TIME

Following tasks must have to be executed after the startup sequence, at least once every fault tolerant time.

- [SM101.4a] The host processor shall check the consistency between the non-masked alarm registers and the ALARMB pin, and the correctness of the received CRC values. Any SPI reply with RS=11 corresponds to an internal error, like wrong CRC or wrong Clock cycles.
- [SM101.4b] The host processor shall check:
  - the content of a known register (e.g. FIXED_VALUE, bank 0, offset 0x0B: expected value: 0xAA55);
  - after each write operation the read back of the written register must be performed, as an integrity check.
- [SM101.5] In order to cover the unexpected activation of commanded safety mechanisms, the host shall periodically read the safety mechanisms manual trigger bits (accel_dc_trigger[1:0] and gyro_dc_trigger[1:0]): if the tests haven't been activated, registers read shall be 0x0.
- [SM101.8] The last 30 Gyro/Accel samples shall be compared; 30 consecutive identical values represent an anomaly causing an alarm.
- [SM101.9] In case pin 12 is configured as ODR clock, then the host shall check the period of the signal considering it acceptable when it is 125µs±10%
- [SM101.10] Read of internal alarm registers:
  - SUMMARY STATUS: Addr 0Eh (i_s_ok_c, i_s_ok_a, i_s_ok_r)
  - GYRO_ST_STATUS_1: Addr 10h
  - GYRO_ST_STATUS_2: Addr 11h
  - ACCEL_ST_STATUS_1: Addr 12h
  - ACCEL_ST_STATUS_2: Addr 13h

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- COMMON_ST_STATUS_1: Addr 14h
- COMMON_ST_STATUS_2: Addr 15h

4.3. CHECKS BASED ON EVENTS

- [SM101.6] In case of suspects on accelerometer saturation, the host shall execute SM16 commanded self-test to check whether the expected proof mass movement is executed correctly.

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5 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
07/25/2022	1.0	First release

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