ICM-42607x/42670x FIFO Usage

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Document Number: AN-000324
Revision: 1.0
Date: 10/08/2021

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1 FIFO OVERVIEW

In ICM-42607x/42670x the storage memory consists of the system memory, which is shared with other functions. System memory is a slave peripheral connected to the internal bus (SOI bus) used by APEX and FIFO bus masters. Any FIFO read operation in Accel-Low-Power-only mode or Sleep mode cannot rely on memory access because FIFO memory read/write operations take place only when the system clock is active.

2 FIFO SPECIAL FRAME

There are two special frames:

1. **Empty Frame:** An empty frame is returned each time a byte is read from an empty FIFO.
2. **Invalid Frame: An invalid frame is returned on any of the following conditions:**
    a. The device is in ALP only or Sleep mode, and the host continues to read data even when the cache is emptied, and the system clock is not yet enabled.
    b. Access to the shared storage memory is busy for a long time and the cache cannot be refilled on time while the host is reading the FIFO
    c. The FIFO is in Streaming mode and a FIFO overflow condition takes place. When the host resumes FIFO reading, the frames contained in the cache are invalidated.

3 FIFO OVERFLOW

FIFO overflow has the following two modes:

1. **Stream to FIFO Mode:** A frame written during the FIFO full condition will overwrite the oldest frame in the FIFO while the frames contained in the cache are old, so they are supposed to be discarded by the host. These frames are invalidated by the FIFO Controller at the first overflow to facilitate the host in the process of discarding
2. **Stop On Full Mode:** When both the cache and FIFO Memory are full, no more frames can be written to FIFO and only a host read operation unlock the FIFO state.

The mode for FIFO can be controlled by Bit 1 of register FIFO_CONFIG1 (0x28H).

0 = Stream-to-FIFO
1 = STOP-on-FULL.

4 FIFO IN LOW POWER MODE

Any FIFO read operation in Accel-Low-Power-only mode or Sleep mode cannot rely on memory access because FIFO memory read/write operations take place only when the system clock is active.

Whenever the host wants to fully operate the FIFO in low power mode, a procedure to require the system clock operativity is provided. The following steps must be executed by the host software when no FIFO watermark interrupt is enabled:

1. Host reads FIFO data count register
2. If device power mode is ALP only or Sleep mode, and the number of available FIFO data frames is greater than the cache size for the selected frame format, then the host must wait for the system oscillator wake-up time (100 µsfor ICM-42607x/42670x); otherwise, the host reads the cache content and jump to step 4
3. Host reads the FIFO content in less than 1 ms from step 1 (timeout period)
4. If more than 1 ms has elapsed from step 1, then host must repeat the procedure from step 1 to re-enable the system oscillator

5 INTERRUPTS

Two interrupts are generated by FIFO Controller: FIFO watermark and FIFO full. A FIFO data counter register reports the number of frames contained in the FIFO, while a lost frame counter register keeps track of the number of lost frames when the FIFO overflows.

When FIFO watermark interrupt is enabled, the host knows upon receiving the interrupt the minimum amount of data the FIFO contains, and thus it does not need to read the FIFO data counter register. The FIFO watermark interrupt event triggers the system oscillator wake-up which is kept on until the very next FIFO read operation (single or burst) finishes on the serial interface.

6 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
10/08/2021	1.0	Initial Release

7 DECLARATION DISCLAIMER

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