ICM-42370-P Datasheet

High Performance 3-Axis Accelerometer

ICM-42370-P HIGHLIGHTS

The ICM-42370-P is a high performance MEMS MotionTracking device that has a 3-axis accelerometer. It has a configurable host interface that supports I3C^{SM}, I^{2}C, and SPI serial communication, features up to 2.25 Kbytes FIFO and 2 programmable interrupts with ultra-low-power wake-on-motion support to minimize system power consumption.

The ICM-42370-P supports the lowest accel sensor noise in this IMU class, and has the highest stability against temperature, shock (up to 20,000g) or SMT/bend induced offset as well as immunity against out-of-band vibration induced noise.

Other industry-leading features include on-chip APEX Motion Processing engine for gesture recognition, and pedometer, along with programmable digital filters, and an embedded temperature sensor.

The device supports a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range from 1.71V to 3.6V.

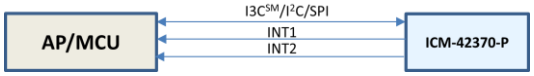
ICM-42370-P FEATURES

- Low-Noise mode current consumption of 0.20 mA
- Low-Power mode support for always-on experience
- Sleep Mode Current Consumption: 3.5µA
- User selectable Accelerometer Full-scale range (g): ± 2/4/8/16
- User-programmable digital filters for accel, and temp sensor
- APEX Motion Functions: Pedometer, Tilt Detection, Low-g Detection, Freefall Detection, Wake on Motion, Significant Motion Detection
- Host interface: 12.5 MHz I3C^{SM}, 1 MHz I^{2}C, 24 MHz SPI

APPLICATIONS

- Cameras
- Appliances
- Consumer and Medical Wearables (IoT)

BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-42370-P†	–40°C to +85°C	2.5x3mm 14-Pin LGA

†Denotes RoHS and Green-Compliant Package

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-42370-P Single-Interface MotionTracking device. The device is housed in a small 2.5x3x0.76 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-42370-P is a MotionTracking device that has a 3-axis accelerometer in a small 2.5x3x0.76 mm (14-pin LGA) package. It also features up to 2.25 Kbytes FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-42370-P, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The accelerometer supports four programmable full-scale range settings from ±2g to ±16g.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C, and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range of 1.71V to 3.6V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.5 MHz (data rates up to 12.5 Mbps in SDR mode, 25 Mbps in DDR mode), the I^{2}C interface supports speeds up to 1 MHz, and the SPI interface supports speeds up to 24 MHz.

The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Cameras
- Appliances
- Consumer and Medical Wearables (IoT)

2 FEATURES

2.1 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-42370-P includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g*
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.2 MOTION FEATURES

ICM-42370-P includes the following motion features, also known as APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen)

- Pedometer: Tracks step count and issues a step detect Interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35 degrees for more than a programmable time.
- Low-g Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Wake on Motion (WoM): Detects motion when accelerometer samples exceed a programmable threshold. This motion event can be used to enable device operation from sleep mode.
- Significant Motion Detector (SMD): Detects significant motion based on accelerometer data.

2.3 ADDITIONAL FEATURES

ICM-42370-P includes the following additional features:

- Up to 2.25 Kbytes FIFO buffer enables the applications processor to read the data in bursts
- User-programmable digital filters for accelerometer, and temperature sensor
- 12.5M Hz I3C^{SM} (data rates up to 12.5 Mbps in SDR mode, 25 Mbps in DDR mode) / 1 MHz I^{2}C / 24 MHz SPI slave host interface
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.76 mm (14-pin LGA)
- 20,000*g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 ACCELEROMETER SPECIFICATIONS

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	ACCEL_UI_FS_SEL=0		±16		*g*	2
	ACCEL_UI_FS_SEL=1		±8		*g*	2
	ACCEL_UI_FS_SEL=2		±4		*g*	2
	ACCEL_UI_FS_SEL=3		±2		*g*	2
ADC Word Length	Output in two's complement format		16		bits	2, 5
Sensitivity Scale Factor	ACCEL_UI_FS_SEL=0		2,048		LSB/*g*	2
	ACCEL_UI_FS_SEL=1		4,096		LSB/*g*	2
	ACCEL_UI_FS_SEL=2		8,192		LSB/*g*	2
	ACCEL_UI_FS_SEL=3		16,384		LSB/*g*	2
Sensitivity Scale Factor Initial Tolerance	25°C		±1		%	1, 7
Sensitivity Change vs. Temperature	-40°C to +85°C; Board-Level		±0.01		%/ºC	3, 6
Nonlinearity	Best Fit Straight Line, ±2g; Board-Level		±0.1		%	3, 6
Cross-Axis Sensitivity	Board-level		±1		%	3, 6
ZERO-G OUTPUT						
Initial Tolerance	25°C		±25		m*g*	1, 7
Zero-G Level Change vs. Temperature	-40°C to +85°C; Board-Level		±0.15		m*g*/ºC	3, 6
OTHER PARAMETERS						
Power Spectral Density	@ 10 Hz		100		µ*g*/√Hz	1
RMS Noise	Bandwidth = 100 Hz		1.0		mg-rms	4
Low Pass Filter Response		16		180	Hz	2
Accelerometer Startup Time	From sleep mode to valid data		10		ms	3, 8
Output Data Rate		1.5625		1600	Hz	2

Table 1. Accelerometer Specifications

Notes:

1. Tested in production at component-level.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not tested in production.
4. Calculated from Power Spectral Density.
5. 20-bits data format supported in FIFO, see section 6.1.
6. Board-level spec values depend on specific board design. For design information of boards used for device characterization, that forms the basis of the spec values reported here, please contact your local TDK InvenSense FAE.
7. Value after factory test and trim.
8. Measurement conditions: Accelerometer ODR = 1600Hz; Register field ACCEL_UI_FILT_BW set to 000 (low pass filter bypassed).

3.2 ELECTRICAL SPECIFICATIONS

3.2.1 D.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	3-Axis Accelerometer		0.20		mA	2
Full-Chip Sleep Mode	At 25ºC		3.5		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 2. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

3.2.2 A.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Valid power-on RESET	0.1		3	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output	Output in two's complement format		0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	1.5625		1600	Hz	2, 4
Room Temperature Offset	25°C	-3		3	°C	3
Stabilization Time (fixed number of clock cycles)				0.64	sec	2
Sensitivity	Trimmed	125	126.9	129	LSB/°C	1
Sensitivity for FIFO data	Trimmed	1.95	1.983	2.01	LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			<10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int_tpulse_duration= 0 , 1 (100us, 8us) ;	8		100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	CLKSEL=`2b00; 25°C	-3		+3	%	1
Frequency Variation over Temperature	CLKSEL=`2b00; -40°C to +85°C			±3	%	1

Table 3. A.C. Electrical Characteristics

Notes:

1. Expected results based on design, will be updated after characterization. Not tested in production.
2. Guaranteed by design.
3. Production tested.
4. Temperature sensor ODR is the same as accelerometer ODR.

3.3 I²C TIMING CHARACTERIZATION

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register DRIVE_CONFIG2.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.5			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.5			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.5			µs	1
C_b, Capacitive Load for each Bus Line				550	pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1

Table 4. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

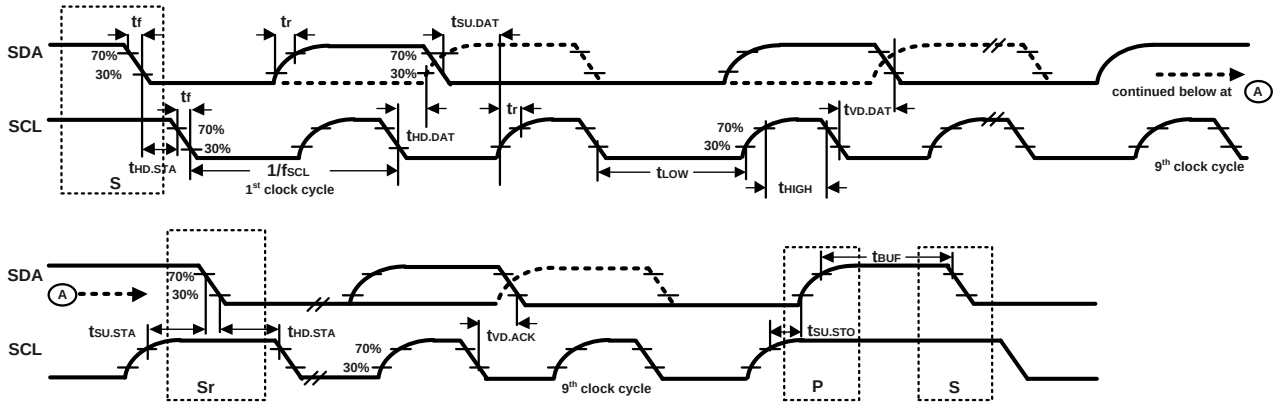

Figure 1. I²C Bus Timing Diagram

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3.4 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register DRIVE_CONFIG3.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		17			ns	1
t_{HIGH}, SCLK High Period		17			ns	1
$t_{SU.CS}$, CS Setup Time		17			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDI}$, SDI Setup Time		13			ns	1
$t_{HD.SDI}$, SDI Hold Time		8			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			18.5	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				18.5	ns	1

Table 5. 4-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

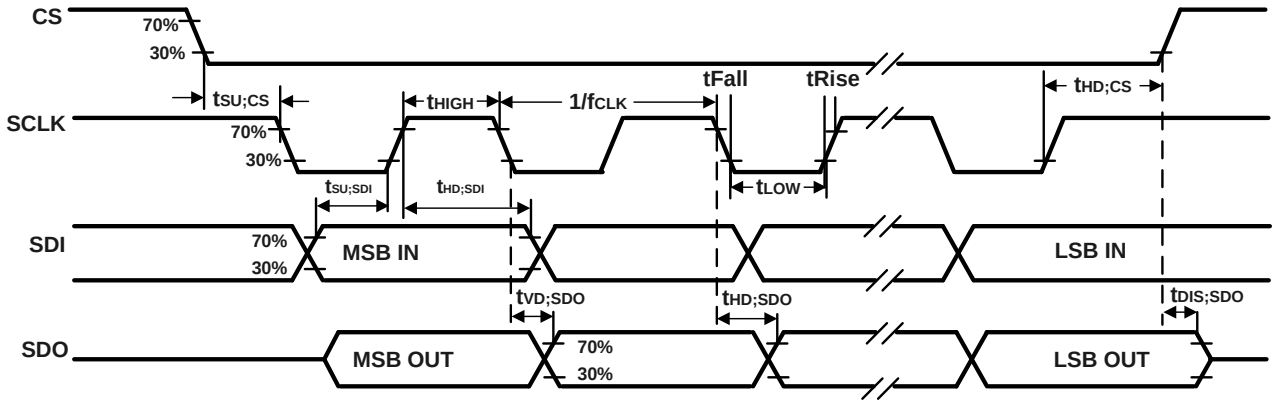

Figure 2. 4-Wire SPI Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register DRIVE_CONFIG3.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		17			ns	1
t_{HIGH}, SCLK High Period		17			ns	1
$t_{SU.CS}$, CS Setup Time		17			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		13			ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8			ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF			18.5	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time				18.5	ns	1

Table 6. 3-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

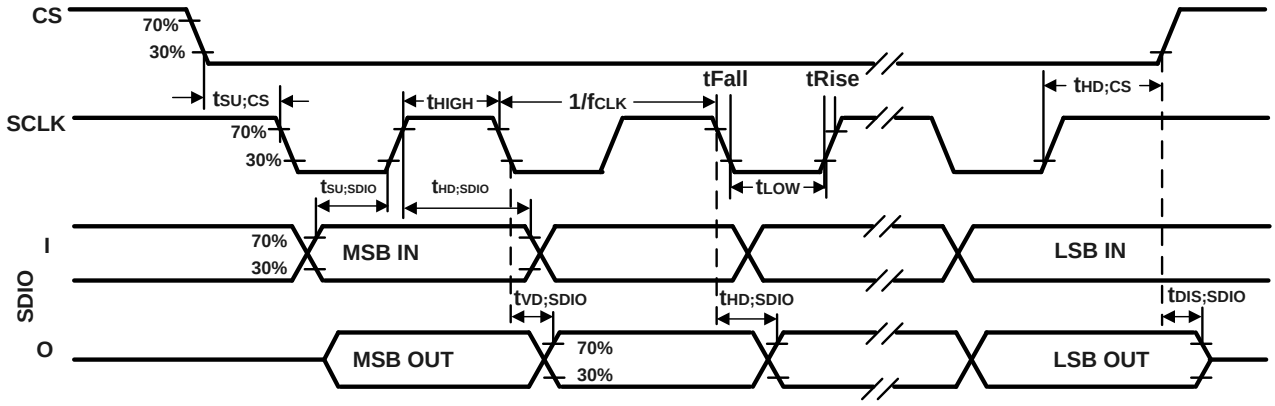

Figure 3. 3-Wire SPI Bus Timing Diagram

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3.6 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to 4V
Supply Voltage, VDDIO	-0.5V to 4V
Input Voltage Level (SCL, SDA)	-0.5V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500V (CDM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 7. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB
2	RESV	No Connect or Connect to GND or Connect to VDDIO
3	RESV	No Connect or Connect to GND or Connect to VDDIO
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain) INT: All interrupts mapped to pin 4
5	VDDIO	IO power supply voltage
6	GND	Power supply ground
7	RESV	Connect to GND
8	VDD	Power supply voltage
9	INT2	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain)
10	RESV	No Connect or Connect to GND or Connect to VDDIO
11	RESV	No Connect or Connect to GND or Connect to VDDIO
12	AP_CS	AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)

Table 8. Signal Descriptions

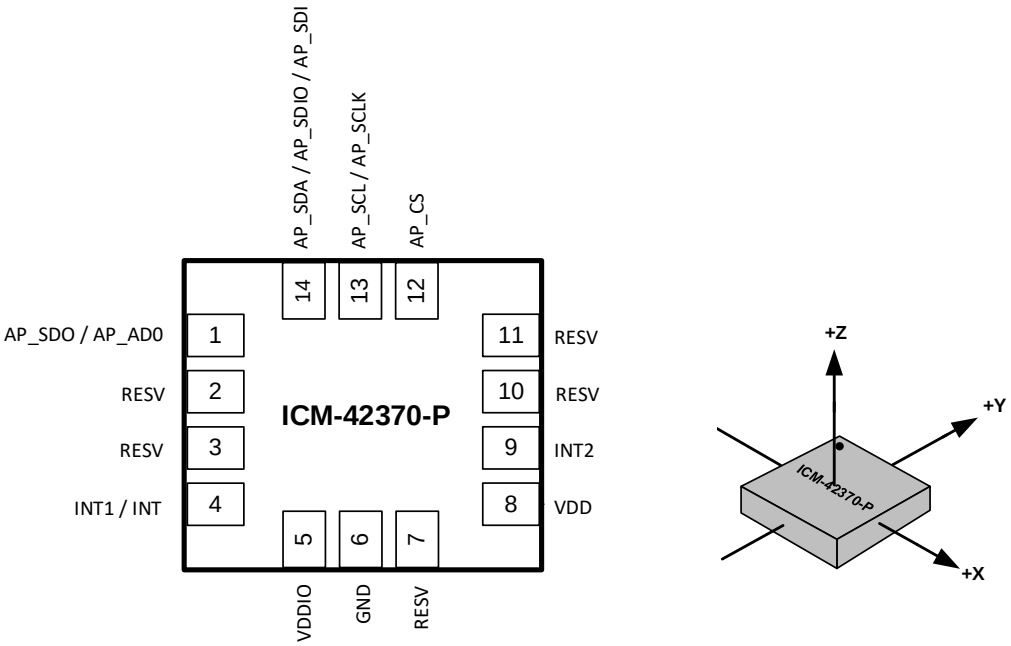

Figure 4. Pin Out Diagram for ICM-42370-P 2.5x3.0x0.76 mm LGA

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4.2 TYPICAL OPERATING CIRCUIT

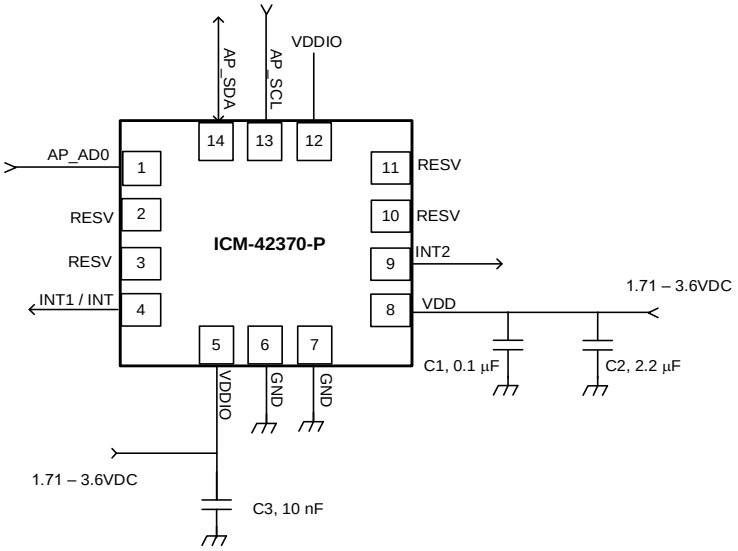

Figure 5. ICM-42370-P Application Schematic (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

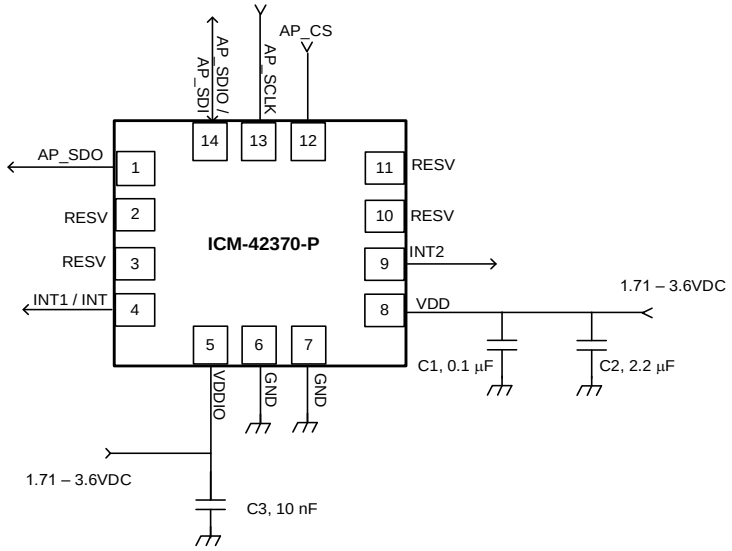

Figure 6. ICM-42370-P Application Schematic (SPI Interface to Host)

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4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
VDD Bypass Capacitors	C1	X7R, 0.1µF ±10%	1
	C2	X7R, 2.2µF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10nF ±10%	1

Table 9. Bill of Materials

4.4 SYSTEM BLOCK DIAGRAM

Figure 7. ICM-42370-P System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.5 OVERVIEW

The ICM-42370-P is comprised of the following key blocks and functions:

- Three-axis MEMS accelerometer
- I3C^{SM}, I^{2}C, and SPI serial communications interfaces to Host
- Self-Test
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS ACCELEROMETER

The ICM-42370-P includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-42370-P architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g* and ±16*g*.

4.7 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The ICM-42370-P communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The ICM-42370-P always acts as a slave when communicating to the application processor.

4.8 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the accelerometer self-test registers. When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response. The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

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When the value of the self-test response is within the specified min/max limits, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.9 SENSOR DATA REGISTERS

The sensor data registers contain the latest accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read any time.

4.10 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) new data is available to be read (from the FIFO and Data registers); (2) accelerometer event interrupts; (3) FIFO watermark; (4) FIFO full. The interrupt status can be read from the Interrupt Status register.

4.11 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-42370-P die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature sensor ODR is the value of the accelerometer.

4.12 BIAS AND LDOS

The bias and LDO section generate the internal supply and the reference voltages and currents required by the ICM-42370-P.

4.13 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-42370-P.

MODE	NAME	ACCEL
1	Sleep Mode	Off
2	Accelerometer Low-Power Mode	Duty-Cycled
3	Accelerometer Low-Noise Mode	On

Table 10. Standard Power Modes for ICM-42370-P

5 SIGNAL PATH

The following figure shows a block diagram of the signal path for ICM-42370-P.

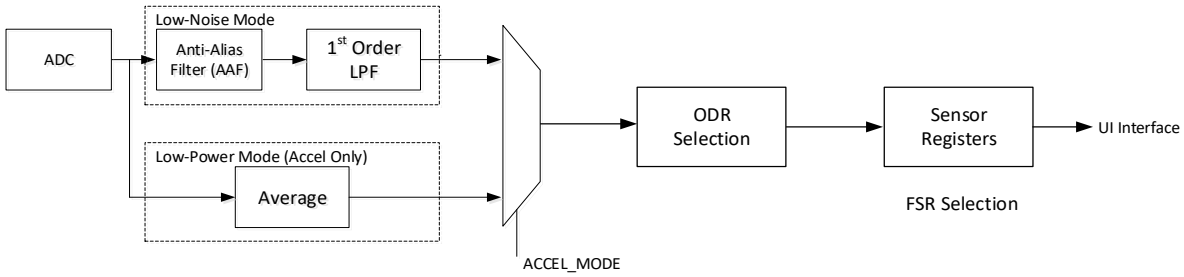

Figure 8. ICM-42370-P Signal Path

The signal path starts with ADCs for the accelerometer. Low-Noise Mode and Low-Power Mode options are available for the accelerometer and are selectable using register field ACCEL_MODE.

In Low-Noise Mode, the ADC output is sent through an Anti-Alias Filter (AAF). The AAF is a filter with fixed coefficients (not user configurable), also the AAF cannot be bypassed. The AAF is followed by a 1st Order Low Pass Filter (LPF) with user selectable filter bandwidth options using register fields ACCEL_UI_FILT_BW.

In Low-Power Mode, the accelerometer ADC output is sent through an Average filter, with user configurable average filter setting using register field ACCEL_UI_AVG.

The output of 1st Order LPF in Low-Noise Mode, or Average filter in Low-Power Mode is subject to ODR selection, with user selectable ODR using register fields ACCEL_ODR. This is followed by Full Scale Range (FSR) selection based on user configurable settings for register fields ACCEL_UI_FS_SEL.

6 FIFO

The ICM-42370-P contains up to 2.25Kbyte FIFO register that is accessible via the serial interface. Shared SRAM is used for FIFO and APEX features. Default configuration of the device provides 1Kbyte FIFO and rest of the SRAM is used for APEX. User may disable APEX features to extend FIFO size to 2.25 Kbytes using register field APEX_DISABLE in register SENSOR_CONFIG3.

User can configure the FIFO Data Rate (FDR) to control the rate at which FIFO packets are written to the FIFO. Register field FDR_SEL in register FDR_CONFIG (register 0x66h in Bank MREG1) provides FDR control, based on settings for FIFO packet rate decimation factor. User must disable sensors when initializing FDR_SEL value or making changes to it.

6.1 PACKET STRUCTURE

Figure 9 shows the FIFO packet structures supported in ICM-42370-P. Base data format for accelerometer is 16-bits per element. 20-bits data format support is included in one of the packet structures. When 20-bits data format is used, accelerometer data consists of 18-bits of actual data and the two lowest order bits are always set to 0. When 20-bits data format is used, the only FSR settings that are operational are and ±16g for accelerometer, even if the FSR selection register settings are configured for other FSR values. The corresponding sensitivity scale factor values are 131 8192 LSB/g for accelerometer.

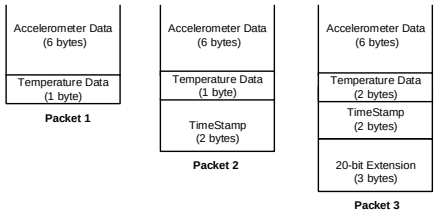

Figure 9. FIFO Packet Structure

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The rest of this sub-section describes how individual data is packaged in the different FIFO packet structures.

Packet 1: Individual data is packaged in Packet 1 as shown below.

BYTE	CONTENT
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Temperature[7:0]

Packet 2: Individual data is packaged in Packet 2 as shown below.

BYTE	CONTENT
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Reserved
0x08	Reserved
0x09	Reserved
0x0A	Reserved
0x0B	Reserved
0x0C	Reserved
0x0D	Temperature[7:0]
0x0E	TimeStamp[15:8]
0x0F	TimeStamp[7:0]

Packet 3: Individual data is packaged in Packet 3 as shown below.

BYTE	CONTENT	
0x00	FIFO Header	
0x01	Accel X [19:12]	
0x02	Accel X [11:4]	
0x03	Accel Y [19:12]	
0x04	Accel Y [11:4]	
0x05	Accel Z [19:12]	
0x06	Accel Z [11:4]	
0x07	Reserved	
0x08	Reserved	
0x09	Reserved	
0x0A	Reserved	
0x0B	Reserved	
0x0C	Reserved	
0x0D	Reserved	
0x0E	Temperature[7:0]	
0x0F	TimeStamp[15:8]	
0x10	TimeStamp[7:0]	
0x11	Accel X [3:0]	Reserved
0x12	Accel Y [3:0]	Reserved
0x13	Accel Z [3:0]	Reserved

6.2 FIFO HEADER

The following table shows the structure of the 1byte FIFO header.

BIT FIELD	ITEM	DESCRIPTION
7	HEADER_MSG	1: FIFO is empty 0: Packet contains sensor data
6	HEADER_ACCEL	1: Packet is sized so that accel data have location in the packet, FIFO_ACCEL_EN must be 1 0: Packet does not contain accel sample
5	-	Reserved
4	HEADER_20	1: Packet has a new and valid sample of extended 20-bit data for accel 0: Packet does not contain a new and valid extended 20-bit data
3:2	HEADER_TIMESTAMP	00: Packet does not contain timestamp data 01: Reserved 10: Packet contains ODR Timestamp 11: Reserved
1	HEADER_ODR_ACCEL	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel
0	-	Reserved

Note at least HEADER_ACCEL must be set for a sensor data packet to be set.

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6.3 MAXIMUM FIFO STORAGE

The maximum number of packets that can be stored in FIFO is a variable quantity depending on the use case. As shown in Figure 10, the physical FIFO size is 1 Kbytes or 2.25 Kbytes (depending on APEX_DISABLE setting as described above). A number of bytes equal to the packet size selected (see section 6.1) is reserved to prevent reading a packet during write operation. Additionally, a read cache 2 packets wide is available.

The total storage available is up to the maximum number of packets that can be accommodated in 1 Kbytes (or 2.25 Kbytes) plus 40 cache bytes. Note: the cache can hold 5 packets instead of 2 in the specific case when the packet size is 8bytes and the FIFO mode is Stop-on-full.

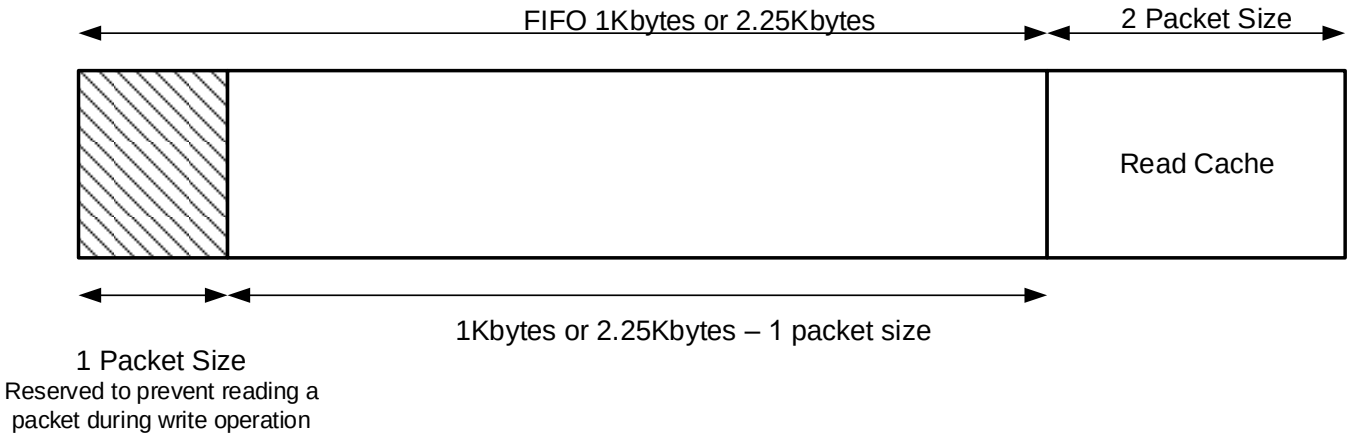

Figure 10. Maximum FIFO Storage

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7 PROGRAMMABLE INTERRUPTS

The ICM-42370-P has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-42370-P includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

8 APEX MOTION FUNCTIONS

The APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen) features of ICM-42370-P consist of:

- Pedometer: Tracks step count and issues a step detect Interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35 degrees for more than a programmable time.
- Low-g Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Wake on Motion (WoM): Detects motion when accelerometer samples exceed a programmable threshold. This motion event can be used to enable device operation from sleep mode.
- Significant Motion Detector (SMD): Detects significant motion based on accelerometer data.

Shared SRAM is used for FIFO and APEX features. Default configuration of the device provides 1Kbyte FIFO and rest of the SRAM is used for APEX. User may disable APEX features to extend FIFO size to 2.25 Kbytes using register field APEX_DISABLE in register SENSOR_CONFIG3.

9 DIGITAL INTERFACE

9.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-42370-P can be accessed using I3C^{SM} at 12.5 MHz (data rates up to 12.5 Mbps in SDR mode, 25 Mbps in DDR mode), I^{2}C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

9.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility. The I3C^{SM} capability of this device is compliant with Version 1.0 of the MIPI Alliance Specification for I3C^{SM}.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-42370-P supports the following features of I3C^{SM}:

- SDR data rate up to 12.5 Mbps
- DDR data rate up to 25 Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-42370-P always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

The following table shows I3C^{SM} Common Command Code (CCC) commands supported by the device.

	CCC Description	Required or Optional per I3C v1.0	Supported by ICM-42370-P
1	ENEC, broadcast mode. (Enable Events)	Required	Yes
2	DISEC, broadcast mode. (Disable Events)	Required	Yes
3	ENTAS0, broadcast mode. (Enter Activity State 0)	Required	Yes
4	ENTAS1, broadcast mode. (Enter Activity State 1)	Optional	No
5	ENTAS2, broadcast mode. (Enter Activity State 0)	Optional	No
6	ENTAS3, broadcast mode. (Enter Activity State 0)	Optional	No
7	RSTDAA, broadcast mode. (Reset dynamic address assignment)	Required	Yes
8	ENTDAA, broadcast mode. (Enter dynamic address assignment)	Required	Yes
9	DEFSLVS, broadcast mode. (Define list of slaves)	Optional	No
10	SETMWL, broadcast mode. (Set Max Write Length)	Required	Yes
11	SETMRL, broadcast mode. (Set Max Read Length)	Required	Yes
12	ENTTM, broadcast mode. (Enter Test Mode)	Optional	No
13	ENTHDR0, broadcast mode. (Enter HDR DDR mode)	Optional	Yes
14	ENTHDR1, broadcast mode. (Enter HDR TSP mode)	Optional	No
15	ENTHDR2, broadcast mode. (Enter HDR TSL mode)	Optional	No
16	SETXTIME, broadcast mode. (Exchange Timing Information)		
	16.1 Defining byte = 0x7F (ST)	Optional	No

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	16.2	Defining byte = 0xBF (DT)	Optional	No
	16.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
	16.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
	16.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
	16.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
	16.7	Defining byte = 0xFD (Async Trigger for Async Mode 3)	Optional	No
	16.8	Defining byte = 0x3F (TPH)	Optional	No
	16.9	Defining byte = 0x9f (TU)	Optional	No
	16.10	Defining byte = 0x8F (ODR)	Optional	No
	16.11	Defining byte = 0xff (disable all timing control function)	Optional	Yes
17	ENEC, direct mode. (Enable Events)		Required	Yes
18	DISEC, direct mode. (Disable Events)		Required	Yes
19	ENTAS0, direct mode. (Enter Activity State 0)		Required	Yes
20	ENTAS1, direct mode. (Enter Activity State 1)		Optional	No
21	ENTAS2, direct mode. (Enter Activity State 2)		Optional	No
22	ENTAS3, direct mode. (Enter Activity State 3)		Optional	No
23	RSTDAA, direct mode. (Reset dynamic address assignment)		Required	Yes
24	SETDASA, direct mode. (Set Dynamic address from static address)		Optional	Yes
25	SETNEWDA, direct mode. (Set new dynamic address)		Required	Yes
26	SETMWL, direct mode. (Set Max Write Length)		Required	Yes
27	SETMRL, direct mode. (Set Max Read length)		Required	Yes
28	GETMWL, direct mode. (Get Max write length)		Required	Yes
29	GETMRL, direct mode. (Get Max Read length)		Required	Yes
30	GETPID, direct mode. (Get provisional ID)		Required	Yes
31	GETBCR, direct mode. (Get Bus Characteristics Register)		Required	Yes
32	GETDCR, direct mode. (Get Device Characteristics Register)		Required	Yes
33	GETSTATUS, direct mode. (Get Device Status)		Required	Yes
34	GETACCMST, direct mode. (Get Accept Mastership)		Optional	No
35	SETBRGTGT, direct mode. (Set Bridge Targets)		Optional	No
36	GETMXDS, direct mod. (Get Max Data Speed)		Optional	Yes
37	GETHDRCAP, direct mode. (Get HDR capability)		Optional	Yes
38	SETXTIME, direct mode. (Set Exchange Timing information)			
	38.1	Defining byte = 0x7F (ST)	Optional	No
	38.2	Defining byte = 0xBF (DT)	Optional	No
	38.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
	38.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
	38.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
	38.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
	38.7	Defining byte = 0xFD (Async Trigger for Async Mode 3)	Optional	No
	38.8	Defining byte = 0x3F (TPH)	Optional	No
	38.9	Defining byte = 0x9f (TU)	Optional	No
	38.10	Defining byte = 0x8F (ODR)	Optional	No

	38.11 Defining byte = 0xff (disable all timing control function)	Optional	Yes
39	GETXTIME, direct mode. (Get Exchange Timing Information)	Optional	Yes

Table 11. I3C^{SM} CCC Commands

9.3 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-42370-P always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-42370-P is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-42370-Ps to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

9.4 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see Figure 11).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

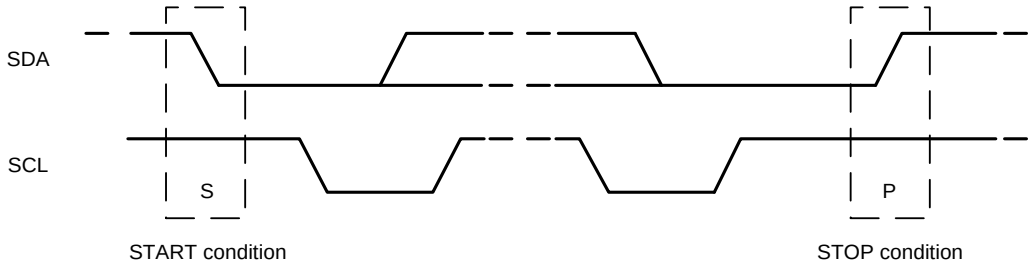

Figure 11. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready and releases the clock line (refer to Figure 12).

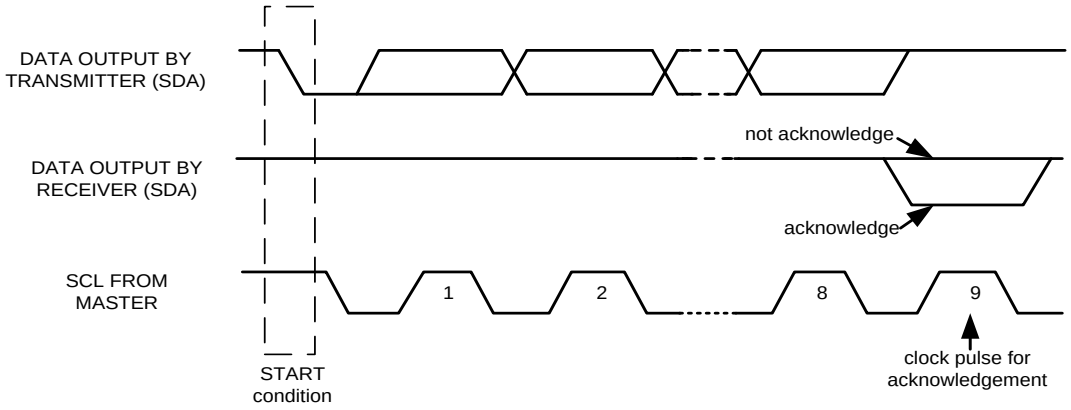

Figure 12. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

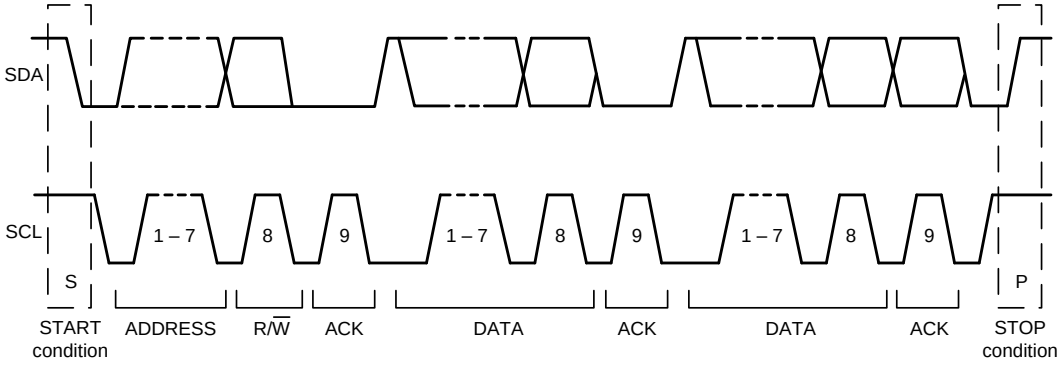

Figure 13. Complete I²C Data Transfer

To write the internal ICM-42370-P registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-42370-P acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-42370-P acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-42370-P automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-42370-P registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-42370-P, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-42370-P sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

9.5 I^2C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-42370-P internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 12. I^2C Terms

9.6 SPI INTERFACE

The ICM-42370-P supports 3-wire or 4-wire SPI for the host interface. The ICM-42370-P always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the Register Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

Register Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

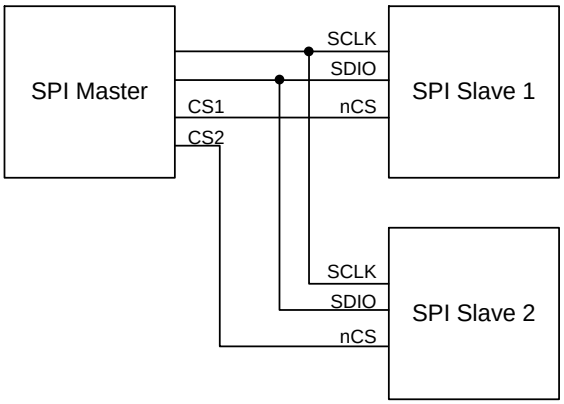

Figure 14. Typical SPI Master/Slave Configuration

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10 ASSEMBLY

This section provides general guidelines for assembling Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

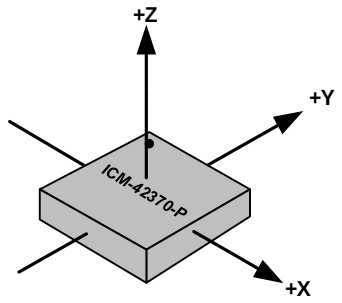
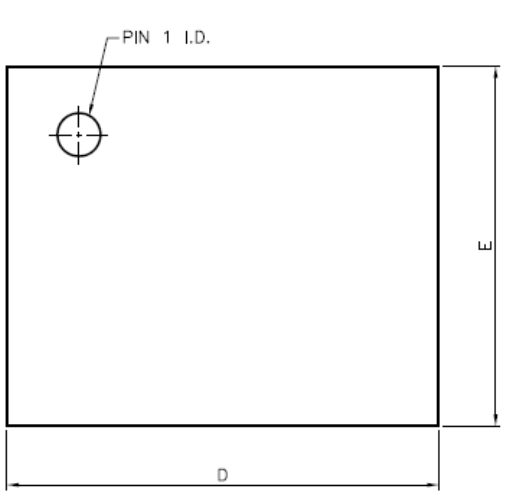


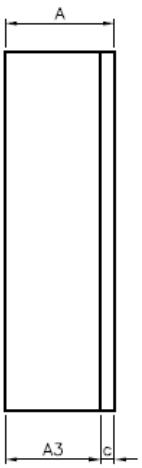
Figure 15. Orientation of Axes of Sensitivity and Polarity of Rotation

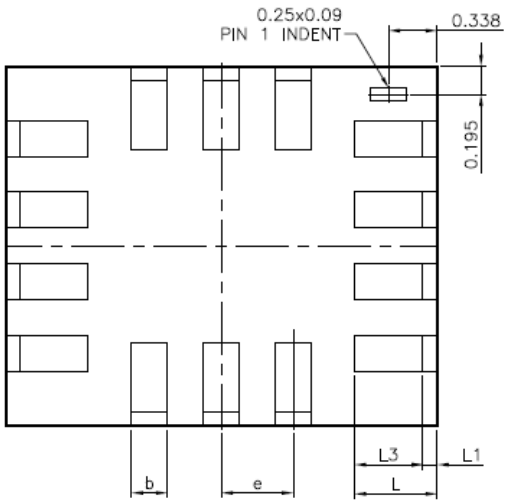
10.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.76) mm NiAu pad finish



TOP VIEW





BOTTOM VIEW

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.71	0.76	0.81
Substrate Thickness	c		0.1 REF	
Mold Thickness	A3		0.65 REF	
Body Size	E	2.45	2.50	2.55
	D	2.95	3.00	3.05
Lead Width	b	0.20	0.25	0.30
Lead Length	L3	0.425	0.475	0.525
Lead Pitch	e		0.5	
Lead Count			14	
Edge Pin Center to Center	e*3		1.5	
	e*2		1	
Body Center to Contact Pin	e/2		0.25	
Package Edge Tolerance			0.05	
Pad-End to Package Tolerance		0.05	0.1	0.15
Mold Flatness				0.1
Coplanarity				0.08

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11 DEVICE PACKAGE IN TAPE AND REEL

ICM-42370-P devices are packaged in the tape and reel as shown in the figures below.

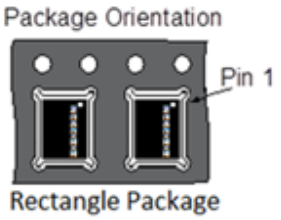

Figure 16. ICM-42370-P Device Package in Tape and Reel

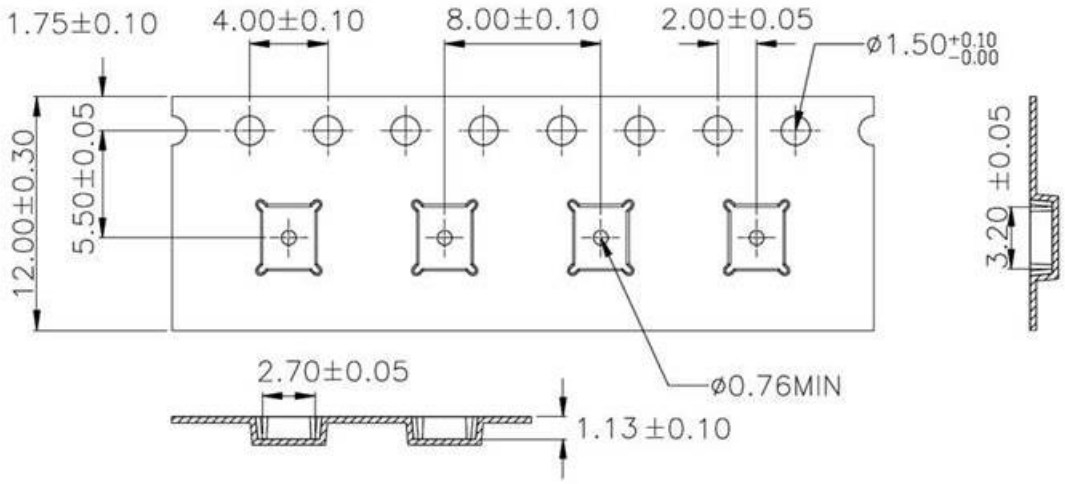

Figure 17. Tape Dimensions with ICM-42370-P Device Package

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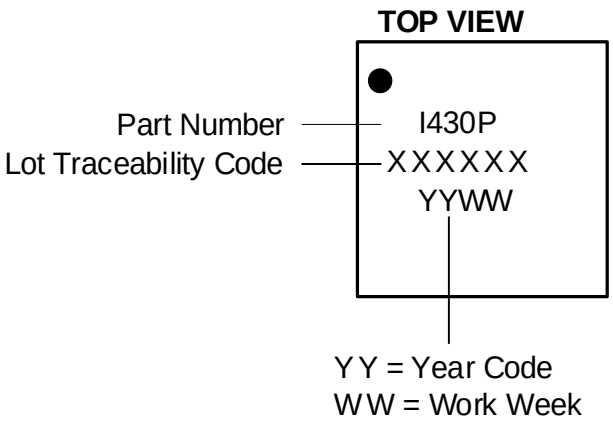
12 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-42370-P devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
ICM-42370-P	I430P



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13 ACCESSING MREG1, MREG2 AND MREG3 REGISTERS

The following procedure must be used to access registers in user banks MREG1, MREG2, and MREG3.

MREG1, MREG2, and MREG3 registers are accessed indirectly, using the following registers in Bank 0 (_W registers for Write, _R registers for Read)

- BLK_SEL_W
- MADDR_W
- M_W
- BLK_SEL_R
- MADDR_R
- M_R

For MREG1 write access, BLK_SEL_W must be set to 0x00. For MREG2 write access, BLK_SEL_W must be set to 0x28. For MREG3 write access, BLK_SEL_W must be set to 0x50.

For MREG1 read access, BLK_SEL_R must be set to 0x00. For MREG2 read access, BLK_SEL_R must be set to 0x28. For MREG3 read access, BLK_SEL_R must be set to 0x50.

User must ensure BLK_SEL_W and BLK_SEL_R are set to 0x00 after completing MREG1, MREG2, or MREG3 access.

Example: To write a value to an MREG1 register at address 0x14 use the following steps:

- BLK_SEL_W must be set to 0
- MADDR_W must be set to 0x14 (address of the MREG1 register being accessed)
- M_W must be set to the desired value
- Wait for 10 µs

Example: To read the value of an MREG1 register at address 0x14 use the following steps:

- BLK_SEL_R must be set to 0
- MADDR_R must be set to 0x14 (address of the MREG1 register being accessed)
- Wait for 10µs
- Read register M_R to access the value in MREG1 register 0x14
- Wait for 10 µs

Host must not access any other register for 10 µs once MREG1, MREG2 or MREG3 access is kicked off.

Additionally, please note the following for MREG1, MREG2 or MREG3 register accesses:

- User must check that register field MCLK_RDY is at value 1, to confirm that internal clock is running before initiating MREG register access.
- MREG1, MREG2, or MREG3 read and write operations cannot happen in all power modes. Sleep mode, and Accelerometer low power mode with WUOSC do not support MREG1, MREG2 or MREG3 access. When in sleep mode or accelerometer LP mode with WUOSC, MREG1, MREG2 or MREG3 read/write operations require the user to power on the RC oscillator using register field IDLE from register PWR_MGMT0.
- It can take up to 10 µs for MREG1, MREG2 or MREG3 read/write operations to be effective. No register access must be performed during this period
- Multiple serial protocol transactions are needed for a single data byte transfer, please refer to the examples provided.
- Data transfers through indirect access are only supported for single byte transfers and burst data transfer is not supported for read or write operations.

14 REGISTER MAP

This section lists the register map for the ICM-42370-P, for user banks 0, MREG1, MREG2 and MREG3.

14.1 USER BANK 0 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	00	MCLK_RDY	R	-				MCLK_RDY	-		
01	01	DEVICE_CONFIG	R/W	-					SPI_AP_4WIRE	-	SPI_MODE
02	02	SIGNAL_PATH_RESET	R/W	-			SOFT_RESET_DEVICE_CONFIG	-	FIFO_FLUSH	-	
03	03	DRIVE_CONFIG1	R/W	-		I3C_DDR_SLEW_RATE			I3C_SDR_SLEW_RATE		
04	04	DRIVE_CONFIG2	R/W	-		I2C_SLEW_RATE			ALL_SLEW_RATE		
05	05	DRIVE_CONFIG3	R/W	-					SPI_SLEW_RATE		
06	06	INT_CONFIG	R/W	-		INT2_MODE	INT2_DRIVE_CIRCUIT	INT2_POLARITY	INT1_MODE	INT1_DRIVE_CIRCUIT	INT1_POLARITY
09	09	TEMP_DATA1	R	TEMP_DATA[15:8]							
0A	10	TEMP_DATA0	R	TEMP_DATA[7:0]							
0B	11	ACCEL_DATA_X1	R	ACCEL_DATA_X[15:8]							
0C	12	ACCEL_DATA_X0	R	ACCEL_DATA_X[7:0]							
0D	13	ACCEL_DATA_Y1	R	ACCEL_DATA_Y[15:8]							
0E	14	ACCEL_DATA_Y0	R	ACCEL_DATA_Y[7:0]							
0F	15	ACCEL_DATA_Z1	R	ACCEL _DATA_Z[15:8]							
10	16	ACCEL _DATA_Z0	R	ACCEL _DATA_Z[7:0]							
1D	29	APEX_DATA4	R	FF_DUR[7:0]							
1E	30	APEX_DATA5	R	FF_DUR[15:8]							
1F	31	PWR_MGMT0	R/W	ACCEL_LP_CLK_SEL	-		IDLE	-		ACCEL_MODE	
21	33	ACCEL_CONFIG0	R/W	-	ACCEL_UI_FS_SEL		-	ACCEL_ODR			
22	34	TEMP_CONFIG0	R/W	-	TEMP_FILT_BW			-			
24	36	ACCEL_CONFIG1	R/W	-	ACCEL_UI_AVG			-	ACCEL_UI_FILT_BW		
25	37	APEX_CONFIG0	R/W	-				DMP_POWER_SAVE_EN	DMP_INIT_EN	-	DMP_MEM_RESET_EN
26	38	APEX_CONFIG1	R/W	-	SMD_ENABLE	FF_ENABLE	TILT_ENABLE	PED_ENABLE	-	DMP_ODR	
27	39	WOM_CONFIG	R/W	-			WOM_INT_DUR		WOM_INT_MODE	WOM_MODE	WOM_EN
28	40	FIFO_CONFIG1	R/W	-						FIFO_MODE	FIFO_BYPASS
29	41	FIFO_CONFIG2	R/W	FIFO_WM[7:0]							
2A	42	FIFO_CONFIG3	R/W	-				FIFO_WM[11:8]			
2B	43	INT_SOURCE0	R/W	ST_INT1_EN	-	PLL_RDY_INT1_EN	RESET_DONE_INT1_EN	DRDY_INT1_EN	FIFO_THS_INT1_EN	FIFO_FULL_INT1_EN	-
2C	44	INT_SOURCE1	R/W	-	I3C_PROTOCOL_ERROR_INT1_EN	-		SMD_INT1_EN	WOM_Z_INT1_EN	WOM_Y_INT1_EN	WOM_X_INT1_EN
2D	45	INT_SOURCE3	R/W	ST_INT2_EN	-	PLL_RDY_INT2_EN	RESET_DONE_INT2_EN	DRDY_INT2_EN	FIFO_THS_INT2_EN	FIFO_FULL_INT2_EN	-
2E	46	INT_SOURCE4	R/W	-	I3C_PROTOCOL_ERROR_INT2_EN	-		SMD_INT2_EN	WOM_Z_INT2_EN	WOM_Y_INT2_EN	WOM_X_INT2_EN
2F	47	FIFO_LOST_PKT0	R	FIFO_LOST_PKT_CNT[7:0]							
30	48	FIFO_LOST_PKT1	R	FIFO_LOST_PKT_CNT[15:8]							
31	49	APEX_DATA0	R	STEP_CNT[7:0]							
32	50	APEX_DATA1	R	STEP_CNT[15:8]							
33	51	APEX_DATA2	R	STEP_CADENCE							
34	52	APEX_DATA3	R	-					DMP_IDLE	ACTIVITY_CLASS	
35	53	INTF_CONFIG0	R/W	-	FIFO_COUNT_FORMAT	FIFO_COUNT_ENDIAN	SENSOR_DATA_ENDIAN	-			
36	54	INTF_CONFIG1	R/W	-				I3C_SDR_EN	I3C_DDR_EN	CLKSEL	
39	57	INT_STATUS_DRDY	R/C	-							DATA_RDY_INT

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
3A	58	INT_STATUS	R/C	ST_INT	-	PLL_RDY_INT	RESET_DONE_INT	-	FIFO_THS_INT	FIFO_FULL_INT	-
3B	59	INT_STATUS2	R/C	-				SMD_INT	WOM_X_INT	WOM_Y_INT	WOM_Z_INT
3C	60	INT_STATUS3	R/C	-		STEP_DET_INT	STEP_CNT_OVF_INT	TILT_DET_INT	FF_DET_INT	LOWG_DET_INT	-
3D	61	FIFO_COUNTH	R	FIFO_COUNT[15:8]							
3E	62	FIFO_COUNTL	R	FIFO_COUNT[7:0]							
3F	63	FIFO_DATA	R	FIFO_DATA							
75	117	WHO_AM_I	R	WHOAMI							
79	121	BLK_SEL_W	R/W	BLK_SEL_W							
7A	122	MADDR_W	R/W	MADDR_W							
7B	123	M_W	R/W	M_W							
7C	124	BLK_SEL_R	R/W	BLK_SEL_R							
7D	125	MADDR_R	R/W	MADDR_R							
7E	126	M_R	R/W	M_R							

14.2 USER BANK MREG1 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	00	TMST_CONFIG1	R/W	-			TMST_ON_SREG_EN	TMST_RES	TMST_DELTA_EN	-	TMST_EN
01	01	FIFO_CONFIG5	R/W	-		FIFO_WM_GT_TH	FIFO_RESUME_PARTIAL_RD	FIFO_HIRES_EN	-		FIFO_ACCEL_EN
02	02	FIFO_CONFIG6	R/W	-			FIFO_EMPTY_INDICATOR_DIS	-			RCOSC_REQ_ON_FIFO_THS_DIS
04	04	INT_CONFIG0	R/W	-		UI_DRDY_INT_CLEAR		FIFO_THS_INT_CLEAR		FIFO_FULL_INT_CLEAR	
05	05	INT_CONFIG1	R/W	-	INT_TPULSE_DURATION	-	INT_ASYNC_RESET	-			
06	06	SENSOR_CONFIG3	R/W	-	APEX_DISABLE	-					
13	19	ST_CONFIG	R/W	-	ST_NUMBER_SAMPLE	ACCEL_ST_LIM		-			
14	20	SELFTEST	R/W	-	ACCEL_ST_EN	-					
23	35	INTF_CONFIG6	R/W	-			I3C_TIMEOUT_EN	I3C_IBI_BYTE_EN	I3C_IBI_EN	-	
25	37	INTF_CONFIG10	R/W	ASYNCTIME0_DIS	-						
28	40	INTF_CONFIG7	R/W	-				I3C_DDR_WR_MODE	-		
2B	43	OTP_CONFIG	R/W	-				OTP_COPY_MODE		-	
2F	47	INT_SOURCE6	R/W	FF_INT1_EN	LOWG_INT1_EN	STEP_DET_INT1_EN	STEP_CNT_OFL_INT1_EN	TILT_DET_INT1_EN	-		
30	48	INT_SOURCE7	R/W	FF_INT2_EN	LOWG_INT2_EN	STEP_DET_INT2_EN	STEP_CNT_OFL_INT2_EN	TILT_DET_INT2_EN	-		
31	49	INT_SOURCE8	R/W	-			PLL_RDY_IBI_EN	UI_DRDY_IBI_EN	FIFO_THS_IBI_EN	FIFO_FULL_IBI_EN	-
32	50	INT_SOURCE9	R/W	I3C_PROTOCOL_ERROR_IBI_EN	FF_IBI_EN	LOWG_IBI_EN	SMD_IBI_EN	WOM_Z_IBI_EN	WOM_Y_IBI_EN	WOM_X_IBI_EN	ST_DONE_IBI_EN
33	51	INT_SOURCE10	R/W	-		STEP_DET_IBI_EN	STEP_CNT_OFL_IBI_EN	TILT_DET_IBI_EN	-		
44	68	APEX_CONFIG2	R/W	LOW_ENERGY_AMP_TH_SEL				DMP_POWER_SAVE_TIME_SEL			
45	69	APEX_CONFIG3	R/W	PED_AMP_TH_SEL				PED_STEP_CNT_TH_SEL			
46	70	APEX_CONFIG4	R/W	PED_STEP_DET_TH_SEL			PED_SB_TIMER_TH_SEL			PED_HI_EN_TH_SEL	
47	71	APEX_CONFIG5	R/W	TILT_WAIT_TIME_SEL		LOWG_PEAK_TH_HYST_SEL			HIGHG_PEAK_TH_HYST_SEL		
48	72	APEX_CONFIG9	R/W	FF_DEBOUNCE_DURATION_SEL				SMD_SENSITIVITY_SEL			SENSITIVITY_MODE
49	73	APEX_CONFIG10	R/W	LOWG_PEAK_TH_SEL					LOWG_TIME_TH_SEL		
4A	74	APEX_CONFIG11	R/W	HIGHG_PEAK_TH_SEL					HIGHG_TIME_TH_SEL		
4B	75	ACCEL_WOM_X_THR	R/W	WOM_X_TH							

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ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
4C	76	ACCEL_WOM_Y_THR	R/W	WOM_Y_TH							
4D	77	ACCEL_WOM_Z_THR	R/W	WOM_Z_TH							
52	82	OFFSET_USER4	R/W	ACCEL_X_OFFUSER[11:8]				-			
53	83	OFFSET_USER5	R/W	ACCEL_X_OFFUSER[7:0]							
54	84	OFFSET_USER6	R/W	ACCEL_Y_OFFUSER[7:0]							
55	85	OFFSET_USER7	R/W	ACCEL_Z_OFFUSER[11:8]				ACCEL_Y_OFFUSER[11:8]			
56	86	OFFSET_USER8	R/W	ACCEL_Z_OFFUSER[7:0]							
63	99	ST_STATUS1	R	-		ACCEL_ST_PASS	ACCEL_ST_DONE	AZ_ST_PASS	AY_ST_PASS	AX_ST_PASS	-
64	100	ST_STATUS2	R	-	ST_INCOMPLETE	-					
66	102	FDR_CONFIG	R/W	-				FDR_SEL			
67	103	APEX_CONFIG12	R/W	FF_MAX_DURATION_SEL				FF_MIN_DURATION_SEL			

14.3 USER BANK MREG2 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
06	06	OTP_CTRL7	R/W	-				OTP_RELOAD	-	OTP_PWR_DOWN	-

14.4 USER BANK MREG3 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	00	XA_ST_DATA	R	XA_ST_DATA							
01	01	YA_ST_DATA	R	YA_ST_DATA							
02	02	ZA_ST_DATA	R	ZA_ST_DATA							

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as can be changed on-the-fly even if sensor is on. These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

15 USER BANK 0 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank 0.

Note: The device powers up in sleep mode.

15.1 MCLK_RDY

Name: MCLK_RDY
Address: 00 (00h)
Serial IF: R
Reset value: 0x00 at power-up, changes to 0x01 after OTP load is completed

BIT	NAME	FUNCTION
7:4	-	Reserved
3	MCLK_RDY	0: Indicates internal clock is currently not running 1: Indicates internal clock is currently running
2:0	-	Reserved

15.2 DEVICE_CONFIG

Name: DEVICE_CONFIG
Address: 01 (01h)
Serial IF: R/W
Reset value: 0x04

BIT	NAME	FUNCTION
7:3	-	Reserved
2	SPI_AP_4WIRE	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode
1	-	Reserved
0	SPI_MODE	SPI mode selection 0: Mode 0 and Mode 3 1: Mode 1 and Mode 2 If device is operating in non-SPI mode, user is not allowed to change the power-on default setting of this register. Change of this register setting will not take effect till AP_CS = 1.

15.3 SIGNAL_PATH_RESET

Name: SIGNAL_PATH_RESET
Address: 02 (02h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	SOFT_RESET_DEVICE_CONFIG	Software Reset (auto clear bit) 0: Software reset not enabled 1: Software reset enabled
3	-	Reserved
2	FIFO_FLUSH	When set to 1, FIFO will get flushed. FIFO flush requires the following programming sequence: • Write FIFO_FLUSH =1 • Wait for 1.5 µs • Read FIFO_FLUSH, it should now be 0 Host can only program this register bit to 1.
1:0	-	Reserved

15.4 DRIVE_CONFIG1

Name: DRIVE_CONFIG1
Address: 03 (03h)
Serial IF: R/W
Reset value: 0x2B

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	I3C_DDR_SLEW_RATE	Controls slew rate for output pin 14 when device is in I3C^{SM} DDR protocol. While in I3C^{SM} operation, the device automatically switches to use I3C_DDR_SLEW_RATE after receiving ENTHDR0 ccc command from the host. The device automatically switches back to I3C_SDR_SLEW_RATE after the host issues HDR_EXIT pattern. 000: MIN: 20 ns; TYP: 40 ns; MAX: 60 ns 001: MIN: 12 ns; TYP: 24 ns; MAX: 36 ns 010: MIN: 6 ns; TYP: 12 ns; MAX: 19 ns 011: MIN: 4 ns; TYP: 8 ns; MAX: 14 ns 100: MIN: 2 ns; TYP: 4 ns; MAX: 8 ns 101: MAX: 2 ns 110: Reserved 111: Reserved This register field should not be programmed in I3C/DDR mode.
2:0	I3C_SDR_SLEW_RATE	Controls slew rate for output pin 14 in I3C^{SM} SDR protocol. After device reset, I2C_SLEW_RATE is used by default. If I3C^{SM} feature is enabled, the device automatically switches to use I3C_SDR_SLEW_RATE after receiving 0x7E+W message (an I3C^{SM} broadcast message). 000: MIN: 20 ns; TYP: 40 ns; MAX: 60 ns 001: MIN: 12 ns; TYP: 24 ns; MAX: 36 ns 010: MIN: 6 ns; TYP: 12 ns; MAX: 19 ns 011: MIN: 4 ns; TYP: 8 ns; MAX: 14 ns 100: MIN: 2 ns; TYP: 4 ns; MAX: 8 ns 101: MAX: 2 ns 110: Reserved 111: Reserved This register field should not be programmed in I3C/DDR mode

15.5 DRIVE_CONFIG2

Name: DRIVE_CONFIG2
Address: 04 (04h)
Serial IF: R/W
Reset value: 0x0D

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	I2C_SLEW_RATE	Controls slew rate for output pin 14 in I^2C mode. After device reset, the I2C_SLEW_RATE is used by default. If the 1st write operation from host is an SPI transaction, the device automatically switches to SPI_SLEW_RATE. If $I3C^{SM}$ feature is enabled, the device automatically switches to I3C_SDR_SLEW_RATE after receiving 0x7E+W message (an I3C broadcast message). 000: MIN: 20 ns; TYP: 40 ns; MAX: 60 ns 001: MIN: 12 ns; TYP: 24 ns; MAX: 36 ns 010: MIN: 6 ns; TYP: 12 ns; MAX: 19 ns 011: MIN: 4 ns; TYP: 8 ns; MAX: 14 ns 100: MIN: 2 ns; TYP: 4 ns; MAX: 8 ns 101: MAX: 2 ns 110: Reserved 111: Reserved This register field should not be programmed in I3C/DDR mode
2:0	ALL_SLEW_RATE	Configure drive strength for all output pins in all modes (SPI3, SPI4, I^2C, $I3C^{SM}$) excluding pin 14. 000: MIN: 20 ns; TYP: 40 ns; MAX: 60 ns 001: MIN: 12 ns; TYP: 24 ns; MAX: 36 ns 010: MIN: 6 ns; TYP: 12 ns; MAX: 19 ns 011: MIN: 4 ns; TYP: 8 ns; MAX: 14 ns 100: MIN: 2 ns; TYP: 4 ns; MAX: 8 ns 101: MAX: 2 ns 110: Reserved 111: Reserved This register field should not be programmed in I3C/DDR mode

15.6 DRIVE_CONFIG3

Name: DRIVE_CONFIG3
Address: 05 (05h)
Serial IF: R/W
Reset value: 0x05

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	SPI_SLEW_RATE	Controls slew rate for output pin 14 in SPI 3-wire mode. In SPI 4-wire mode this register controls the slew rate of pin 1 as it is used as an output in SPI 4-wire mode only. After chip reset, the I2C_SLEW_RATE is used by default for pin 14 pin. If the 1st write operation from the host is an SPI3/4 transaction, the device automatically switches to SPI_SLEW_RATE. 000: MIN: 20 ns; TYP: 40 ns; MAX: 60 ns 001: MIN: 12 ns; TYP: 24 ns; MAX: 36 ns 010: MIN: 6 ns; TYP: 12 ns; MAX: 19 ns 011: MIN: 4 ns; TYP: 8 ns; MAX: 14 ns 100: MIN: 2 ns; TYP: 4 ns; MAX: 8 ns 101: MAX: 2 ns 110: Reserved 111: Reserved This register field should not be programmed in I3C/DDR mode

15.7 INT_CONFIG

Name: INT_CONFIG
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT2_MODE	INT2 interrupt mode 0: Pulsed mode 1: Latched mode
4	INT2_DRIVE_CIRCUIT	INT2 drive circuit 0: Open drain 1: Push pull
3	INT2_POLARITY	INT2 interrupt polarity 0: Active low 1: Active high
2	INT1_MODE	INT1 interrupt mode 0: Pulsed mode 1: Latched mode
1	INT1_DRIVE_CIRCUIT	INT1 drive circuit 0: Open drain 1: Push pull
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low 1: Active high

15.8 TEMP_DATA1

Name: TEMP_DATA1
Address: 09 (09h)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	TEMP_DATA[15:8]	Upper byte of temperature data

15.9 TEMP_DATA0

Name: TEMP_DATA0
Address: 10 (0Ah)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_DATA[7:0]	Lower byte of temperature data

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

- Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

Temperature data stored in FIFO can be an 8-bit or 16-bit quantity, depending on packet format. It can be converted to degrees centigrade by using the following formulas:

- 8-bit quantity: Temperature in Degrees Centigrade = (TEMP_DATA / 2) + 25; where TEMP_DATA refers to the 8 MSBs of the 16-bit word coming from the temperature sensor. In this mode the 8 LSBs are set to '0'.
- 16-bit quantity: Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

15.10 ACCEL_DATA_X1

Name: ACCEL_DATA_X1
Address: 11 (0Bh)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[15:8]	Upper byte of Accel X-axis data

15.11 ACCEL_DATA_X0

Name: ACCEL_DATA_X0
Address: 12 (0Ch)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[7:0]	Lower byte of Accel X-axis data

15.12 ACCEL_DATA_Y1

Name: ACCEL_DATA_Y1
Address: 13 (0Dh)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[15:8]	Upper byte of Accel Y-axis data

15.13 ACCEL_DATA_Y0

Name: ACCEL_DATA_Y0
Address: 14 (0Eh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[7:0]	Lower byte of Accel Y-axis data

15.14 ACCEL_DATA_Z1

Name: ACCEL_DATA_Z1
Address: 15 (0Fh)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[15:8]	Upper byte of Accel Z-axis data

15.15 ACCEL_DATA_Z0

Name: ACCEL_DATA_Z0
Address: 16 (10h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[7:0]	Lower byte of Accel Z-axis data

15.16 APEX_DATA4

Name: APEX_DATA4
Address: 29 (1Dh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_DUR[7:0]	Lower byte of Freefall Duration The duration is given in number of samples and it can be converted to freefall distance in meters by applying the following formula: FF_DISTANCE = 0.5*9.81*(FF_DUR*DMP_ODR_S)^2 Note: DMP_ODR_S is the duration of DMP_ODR expressed in seconds.

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15.17 APEX_DATA5

Name: APEX_DATA5
Address: 30 (1Eh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_DUR[15:8]	Upper byte of Freefall Duration The duration is given in number of samples and it can be converted to freefall distance in meters by applying the following formula: FF_DISTANCE = 0.5*9.81*(FF_DUR*DMP_ODR_S)^2 Note: DMP_ODR_S is the duration of DMP_ODR expressed in seconds.

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15.18 PWR_MGMT0

Name: PWR_MGMT0
Address: 31 (1Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	ACCEL_LP_CLK_SEL	0: Accelerometer LP mode uses Wake Up oscillator clock. This is the lowest power consumption mode and it is the recommended setting. 1: Accelerometer LP mode uses RC oscillator clock This field can be changed on-the-fly even if accel sensor is on
6:5	-	Reserved
4	IDLE	If this bit is set to 1, the RC oscillator is powered on even if Accel is powered off. Nominally this bit is set to 0, so when Accel is powered off, the chip will go to OFF state, since the RC oscillator will also be powered off This field can be changed on-the-fly even if a sensor is on
3:2	-	Reserved
1:0	ACCEL_MODE	00: Turns accelerometer off 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode When selecting LP Mode please refer to ACCEL_LP_CLK_SEL setting, bit[7] of this register. Before entering LP mode and during LP Mode the following combinations of ODR and averaging are not permitted: 1) ODR=1600 Hz or ODR=800 Hz: any averaging. 2) ODR=400 Hz: averaging=16x, 32x or 64x. 3) ODR=200 Hz: averaging=64x. When transitioning from OFF to any of the other modes, do not issue any register writes for 200 µs. This field can be changed on-the-fly even if accel sensor is on

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15.19 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 33 (21h)
Serial IF: R/W
Reset value: 0x06

BIT	NAME	FUNCTION
7	-	Reserved
6:5	ACCEL_UI_FS_SEL	Full scale select for accelerometer UI interface output 00: ±16g 01: ±8g 10: ±4g 11: ±2g This field can be changed on-the-fly even if accel sensor is on
4	-	Reserved
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 1.6 kHz (LN mode) 0110: 800 Hz (LN mode) 0111: 400 Hz (LP or LN mode) 1000: 200 Hz (LP or LN mode) 1001: 100 Hz (LP or LN mode) 1010: 50 Hz (LP or LN mode) 1011: 25 Hz (LP or LN mode) 1100: 12.5 Hz (LP or LN mode) 1101: 6.25 Hz (LP mode) 1110: 3.125 Hz (LP mode) 1111: 1.5625 Hz (LP mode) This field can be changed on-the-fly when accel sensor is on

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15.20 TEMP_CONFIG0

Name: TEMP_CONFIG0
Address: 34 (22h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6:4	TEMP_FILT_BW	Sets the bandwidth of the temperature signal DLPF 000: DLPF bypassed 001: DLPF BW = 180 Hz 010: DLPF BW = 72 Hz 011: DLPF BW = 34 Hz 100: DLPF BW = 16 Hz 101: DLPF BW = 8 Hz 110: DLPF BW = 4 Hz 111: DLPF BW = 4 Hz This field can be changed on-the-fly even if sensor is on
3:0	-	Reserved

15.21 ACCEL_CONFIG1

Name: ACCEL_CONFIG1
Address: 36 (24h)
Serial IF: R/W
Reset value: 0x41

BIT	NAME	FUNCTION
7	-	Reserved
6:4	ACCEL_UI_AVG	Selects averaging filter setting to create accelerometer output in accelerometer low power mode (LPM) 000: 2x average 001: 4x average 010: 8x average 011: 16x average 100: 32x average 101: 64x average 110: 64x average 111: 64x average This field cannot be changed when the accel sensor is in LPM
3	-	Reserved
2:0	ACCEL_UI_FILT_BW	Selects ACCEL UI low pass filter bandwidth 000: Low pass filter bypassed 001: 180 Hz 010: 121 Hz 011: 73 Hz 100: 53 Hz 101: 34 Hz 110: 25 Hz 111: 16 Hz This field can be changed on-the-fly even if accel sensor is on

15.22 APEX_CONFIG0

Name: APEX_CONFIG0
Address: 37 (25h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:4	-	Reserved
3	DMP_POWER_SAVE_EN	When this bit is set to 1, power saving is enabled for DMP algorithms
2	DMP_INIT_EN	When this bit is set to 1, DMP runs DMP SW initialization procedure. Bit is reset by hardware when the procedure is finished. All other APEX features are ignored as long as DMP_INIT_EN is set. This field can be changed on-the-fly even if accel sensor is on.
1	-	Reserved
0	DMP_MEM_RESET_EN	When this bit is set to 1, it clears DMP SRAM for APEX operation or Self-test operation.

15.23 APEX_CONFIG1

Name: APEX_CONFIG1
Address: 38 (26h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7	-	Reserved
6	SMD_ENABLE	0: Significant Motion Detection not enabled 1: Significant Motion Detection enabled This field can be changed on-the-fly even if accel sensor is on
5	FF_ENABLE	0: Freefall Detection not enabled 1: Freefall Detection enabled This field can be changed on-the-fly even if accel sensor is on
4	TILT_ENABLE	0: Tilt Detection not enabled 1: Tilt Detection enabled This field can be changed on-the-fly even if accel sensor is on
3	PED_ENABLE	0: Pedometer not enabled 1: Pedometer enabled This field can be changed on-the-fly even if accel sensor is on
2	-	Reserved
1:0	DMP_ODR	00: 25 Hz 01: 400 Hz 10: 50 Hz 11: 100 Hz The ACCEL_ODR field must be configured to an ODR equal or greater to the DMP_ODR field, for correct device operation. This field can be changed on-the-fly even if accel sensor is on

15.24 WOM_CONFIG

Name: WOM_CONFIG
Address: 39 (27h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4:3	WOM_INT_DUR	Selects Wake on Motion interrupt assertion from among the following options 00: WoM interrupt asserted at first overthreshold event 01: WoM interrupt asserted at second overthreshold event 10: WoM interrupt asserted at third overthreshold event 11: WoM interrupt asserted at fourth overthreshold event This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
2	WOM_INT_MODE	0: Set WoM interrupt on the OR of all enabled accelerometer thresholds 1: Set WoM interrupt on the AND of all enabled accelerometer thresholds This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
1	WOM_MODE	0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample This field can be changed on-the-fly even if accel sensor is on, but it cannot be changed if WOM_EN is already enabled
0	WOM_EN	0: WOM disabled 1: WOM enabled This field can be changed on-the-fly even if accel sensor is on

15.25 FIFO_CONFIG1

Name: FIFO_CONFIG1
Address: 40 (28h)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:2	-	Reserved
1	FIFO_MODE	FIFO mode control 0: Stream-to-FIFO Mode 1: STOP-on-FULL Mode
0	FIFO_BYPASS	FIFO bypass control 0: FIFO is not bypassed 1: FIFO is bypassed

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15.26 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 41 (29h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_WM[7:0]	Lower bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_FORMAT setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source. This field should be changed when FIFO is empty to avoid spurious interrupts.

15.27 FIFO_CONFIG3

Name: FIFO_CONFIG3
Address: 42 (2Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	FIFO_WM[11:8]	Upper bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_FORMAT setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source. This field should be changed when FIFO is empty to avoid spurious interrupts.

15.28 INT_SOURCE0

Name: INT_SOURCE0
Address: 43 (2Bh)
Serial IF: R/W
Reset value: 0x10

BIT	NAME	FUNCTION
7	ST_INT1_EN	0: Self-Test Done interrupt not routed to INT1 1: Self-Test Done interrupt routed to INT1
6	-	Reserved
5	PLL_RDY_INT1_EN	0: PLL ready interrupt not routed to INT1 1: PLL ready interrupt routed to INT1
4	RESET_DONE_INT1_EN	0: Reset done interrupt not routed to INT1 1: Reset done interrupt routed to INT1
3	DRDY_INT1_EN	0: Data Ready interrupt not routed to INT1 1: Data Ready interrupt routed to INT1
2	FIFO_THS_INT1_EN	0: FIFO threshold interrupt not routed to INT1 1: FIFO threshold interrupt routed to INT1
1	FIFO_FULL_INT1_EN	0: FIFO full interrupt not routed to INT1 1: FIFO full interrupt routed to INT1 To avoid FIFO FULL interrupts while reading FIFO, this bit should be disabled while reading FIFO
0	-	Reserved

15.29 INT_SOURCE1

Name: INT_SOURCE1
Address: 44 (2Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT1_EN	0: I3C^{SM} protocol error interrupt not routed to INT1 1: I3C^{SM} protocol error interrupt routed to INT1
5:4	-	Reserved
3	SMD_INT1_EN	0: SMD interrupt not routed to INT1 1: SMD interrupt routed to INT1
2	WOM_Z_INT1_EN	0: Z-axis WOM interrupt not routed to INT1 1: Z-axis WOM interrupt routed to INT1
1	WOM_Y_INT1_EN	0: Y-axis WOM interrupt not routed to INT1 1: Y-axis WOM interrupt routed to INT1
0	WOM_X_INT1_EN	0: X-axis WOM interrupt not routed to INT1 1: X-axis WOM interrupt routed to INT1

15.30 INT_SOURCE3

Name: INT_SOURCE3
Address: 45 (2Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	ST_INT2_EN	0: Self-Test Done interrupt not routed to INT2 1: Self-Test Done interrupt routed to INT2
6	-	Reserved
5	PLL_RDY_INT2_EN	0: PLL ready interrupt not routed to INT2 1: PLL ready interrupt routed to INT2
4	RESET_DONE_INT2_EN	0: Reset done interrupt not routed to INT2 1: Reset done interrupt routed to INT2
3	DRDY_INT2_EN	0: Data Ready interrupt not routed to INT2 1: Data Ready interrupt routed to INT2
2	FIFO_THS_INT2_EN	0: FIFO threshold interrupt not routed to INT2 1: FIFO threshold interrupt routed to INT2
1	FIFO_FULL_INT2_EN	0: FIFO full interrupt not routed to INT2 1: FIFO full interrupt routed to INT2
0	-	Reserved

15.31 INT_SOURCE4

Name: INT_SOURCE4
Address: 46 (2Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT2_EN	0: I3C^{SM} protocol error interrupt not routed to INT2 1: I3C^{SM} protocol error interrupt routed to INT2
5:4	-	Reserved
3	SMD_INT2_EN	0: SMD interrupt not routed to INT2 1: SMD interrupt routed to INT2
2	WOM_Z_INT2_EN	0: Z-axis WOM interrupt not routed to INT2 1: Z-axis WOM interrupt routed to INT2
1	WOM_Y_INT2_EN	0: Y-axis WOM interrupt not routed to INT2 1: Y-axis WOM interrupt routed to INT2
0	WOM_X_INT2_EN	0: X-axis WOM interrupt not routed to INT2 1: X-axis WOM interrupt routed to INT2

15.32 FIFO_LOST_PKT0

Name: FIFO_LOST_PKT0
Address: 47 (2Fh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[7:0]	Low byte, number of packets lost in the FIFO

15.33 FIFO_LOST_PKT1

Name: FIFO_LOST_PKT1
Address: 48 (30h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[15:8]	High byte, number of packets lost in the FIFO

15.34 APEX_DATA0

Name: APEX_DATA0
Address: 49 (31h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CNT[7:0]	Pedometer Output: Lower byte of Step Count measured by pedometer

15.35 APEX_DATA1

Name: APEX_DATA1
Address: 50 (32h)
Serial IF: SYNCR
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CNT[15:8]	Pedometer Output: Upper byte of Step Count measured by pedometer

15.36 APEX_DATA2

Name: APEX_DATA2
Address: 51 (33h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	STEP_CADENCE	Pedometer Output: Walk/run cadency in number of samples. Format is u6.2. e.g. At 50 Hz ODR and 2 Hz walk frequency, the cadency is 25 samples and the register will output 100.

15.37 APEX_DATA3

Name: APEX_DATA3
Address: 52 (34h)
Serial IF: R
Reset value: 0x04

BIT	NAME	FUNCTION
7:3	-	Reserved
2	DMP_IDLE	0: Indicates DMP is running 1: Indicates DMP is idle
1:0	ACTIVITY_CLASS	Pedometer Output: Detected activity 00: Unknown 01: Walk 10: Run 11: Reserved

15.38 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 53 (35h)
Serial IF: R/W
Reset value: 0x30

BIT	NAME	FUNCTION
7	-	Reserved
6	FIFO_COUNT_FORMAT	0: FIFO count is reported in bytes 1: FIFO count is reported in records (1 record = 16 bytes for header accel + temp sensor data + time stamp, or 8 bytes for header + accel + temp sensor data)
5	FIFO_COUNT_ENDIAN	This bit applies to FIFO Count and Lost Packet Count 0: Reported in Little Endian format 1: Reported in Big Endian format
4	SENSOR_DATA_ENDIAN	0: Sensor data is reported in Little Endian format 1: Sensor data is reported in Big Endian format
3:0	-	Reserved

15.39 INTF_CONFIG1

Name: INTF_CONFIG1
Address: 54 (36h)
Serial IF: R/W
Reset value: 0x4D

BIT	NAME	FUNCTION
7:4	-	Reserved
3	I3C_SDR_EN	0: I3C^{SM} SDR mode not enabled 1: I3C^{SM} SDR mode enabled Device will be in pure I^{2}C mode if {I3C_SDR_EN, I3C_DDR_EN} = 00
2	I3C_DDR_EN	0: I3C^{SM} DDR mode not enabled 1: I3C^{SM} DDR mode enabled This bit will not take effect unless I3C_SDR_EN = 1.
1:0	CLKSEL	00: Always select internal RC oscillator 01: Select PLL when available, else select RC oscillator (default) 10: Reserved 11: Disable all clocks

15.40 INT_STATUS_DRDY

Name: INT_STATUS_DRDY
Address: 57 (39h)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved
0	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

15.41 INT_STATUS

Name: INT_STATUS
Address: 58 (3Ah)
Serial IF: R/C
Reset value: 0x10

BIT	NAME	FUNCTION
7	ST_INT	This bit automatically sets to 1 when a Self Test done interrupt is generated. The bit clears to 0 after the register has been read.
6	-	Reserved
5	PLL_RDY_INT	This bit automatically sets to 1 when a PLL Ready interrupt is generated. The bit clears to 0 after the register has been read.
4	RESET_DONE_INT	This bit automatically sets to 1 when software reset is complete. The bit clears to 0 after the register has been read.
3	-	Reserved
2	FIFO_THS_INT	This bit automatically sets to 1 when the FIFO buffer reaches the threshold value. The bit clears to 0 after the register has been read.
1	FIFO_FULL_INT	This bit automatically sets to 1 when the FIFO buffer is full. The bit clears to 0 after the register has been read.
0	-	Reserved

15.42 INT_STATUS2

Name: INT_STATUS2
Address: 59 (3Bh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SMD_INT	Significant Motion Detection Interrupt, clears on read
2	WOM_X_INT	Wake on Motion Interrupt on X-axis, clears on read
1	WOM_Y_INT	Wake on Motion Interrupt on Y-axis, clears on read
0	WOM_Z_INT	Wake on Motion Interrupt on Z-axis, clears on read

15.43 INT_STATUS3

Name: INT_STATUS3
Address: 60 (3Ch)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_INT	Step Detection Interrupt, clears on read
4	STEP_CNT_OVF_INT	Step Count Overflow Interrupt, clears on read
3	TILT_DET_INT	Tilt Detection Interrupt, clears on read
2	FF_DET_INT	Freefall Interrupt, clears on read
1	LOWG_DET_INT	LowG Interrupt, clears on read
0	-	Reserved

15.44 FIFO_COUNTH

Name: FIFO_COUNTH
Address: 61 (3Dh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_COUNT[15:8]	High Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_FORMAT setting. Note: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

15.45 FIFO_COUNTL

Name: FIFO_COUNTL
Address: 62 (3Eh)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_COUNT[7:0]	Low Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

15.46 FIFO_DATA

Name: FIFO_DATA
Address: 63 (3Fh)
Serial IF: R
Reset value: 0xFF

BIT	NAME	FUNCTION
7:0	FIFO_DATA	FIFO data port

15.47 WHO_AM_I

Name: WHO_AM_I
Address: 117 (75h)
Serial IF: R
Reset value: 0x0D

BIT	NAME	FUNCTION
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x0D. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor.

15.48 BLK_SEL_W

Name: BLK_SEL_W
Address: 121 (79h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	BLK_SEL_W	Block address for accessing MREG1 or MREG2 register space for register write operation

15.49 MADDR_W

Name: MADDR_W
Address: 122 (7Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	MADDR_W	To write to a register in MREG1 or MREG2 space, set this register field to the address of the register in MREG1 or MREG2 space.

15.50 M_W

Name: M_W
Address: 123 (7Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	M_W	To write a value to a register in MREG1 or MREG2 space, that value must be written to M_W.

15.51 BLK_SEL_R

Name: BLK_SEL_R
Address: 124 (7Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	BLK_SEL_R	Block address for accessing MREG1 or MREG2 register space for register read operation

15.52 MADDR_R

Name: MADDR_R
Address: 125 (7Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	MADDR_R	To read the value of a register in MREG1 or MREG2 space, set this register field to the address of the register in MREG1 or MREG2 space.

15.53 M_R

Name: M_R
Address: 126 (7Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	M_R	To read the value of a register in MREG1 or MREG2 space, that value is accessed from M_R.

16 USER BANK MREG1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank MREG1. The procedure for accessing MREG1 registers is described in section 13.

16.1 TMST_CONFIG1

Name: TMST_CONFIG1
Address: 00 (00h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:4	-	Reserved
3	TMST_RES	Time Stamp resolution: When set to 0 (default), time stamp resolution is 1 µs. When set to 1, resolution is 16 µs
2	TMST_DELTA_EN	Time Stamp delta enable: When set to 1, the time stamp field contains the measurement of time since the last occurrence of ODR.
1	-	Reserved
0	TMST_EN	0: Time Stamp register disable 1: Time Stamp register enable

16.2 FIFO_CONFIG5

Name: FIFO_CONFIG5
Address: 01 (01h)
Serial IF: R/W
Reset value: 0x20

BIT	NAME	FUNCTION
7:6	-	Reserved
5	FIFO_WM_GT_TH	0: Trigger FIFO Watermark interrupt when FIFO_COUNT = FIFO_WM 1: Trigger FIFO Watermark interrupt on every ODR if FIFO_COUNT = FIFO_WM
4	FIFO_RESUME_PARTIAL_RD	0: FIFO is read in packets. If a partial packet is read, then the subsequent read will start from the beginning of the un-read packet. 1: FIFO can be read partially. When read is resumed, FIFO bytes will continue from last read point. The SW driver is responsible for cascading previous read and present read and for maintaining frame boundaries.
3	FIFO_HIRES_EN	0: 20-bit resolution not enabled in the FIFO packet readout 1: 20-bit resolution enabled in the FIFO packet readout
2:1	-	Reserved
0	FIFO_ACCEL_EN	0: Accel packets not enabled to go to FIFO 1: Enables Accel packets to go to FIFO

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16.3 FIFO_CONFIG6

Name: FIFO_CONFIG6
Address: 02 (02h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	FIFO_EMPTY_INDICATOR_DIS	0: 0xFF is sent out as FIFO data when FIFO is empty. 1: The last FIFO data is sent out when FIFO is empty.
3:1	-	Reserved
0	RCOSC_REQ_ON_FIFO_THS_DIS	0: When the FIFO is operating in ALP+WUOSC mode and the watermark (WM) interrupt is enabled, the FIFO wakes up the system oscillator (RCOSC) as soon as the watermark level is reached. The system oscillator remains enabled until a Host FIFO read operation happens. This will temporarily cause a small increase in the power consumption due to the enabling of the system oscillator. 1: The system oscillator is not automatically woken-up by the FIFO/INT when the WM interrupt is triggered. The side effect is that the host can receive invalid packets until the system oscillator is off after it has been turned on for other reasons not related to a WM interrupt. The recommended setting of this bit is '1' before entering and during all power modes excluding ALP with WUOSC. This is in order to avoid having to do a FIFO access/flush before entering sleep mode. During ALP with WUOSC it is recommended to set this bit to '0'. It is recommended to reset this bit back to '1' before exiting ALP+WUOSC with a wait time of 1 ODR or higher.

16.4 INT_CONFIG0

Name: INT_CONFIG0
Address: 04 (04h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	UI_DRDY_INT_CLEAR	Data Ready Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read 01: Clear on Status Bit Read 10: Clear on Sensor Register Read 11: Clear on Status Bit Read OR on Sensor Register read
3:2	FIFO_THS_INT_CLEAR	FIFO Threshold Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read OR on FIFO data 1 byte read
1:0	FIFO_FULL_INT_CLEAR	FIFO Full Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read OR on FIFO data 1 byte read

16.5 INT_CONFIG1

Name: INT_CONFIG1
Address: 05 (05h)
Serial IF: R/W
Reset value: 0x10

BIT	NAME	FUNCTION
7	-	Reserved
6	INT_TPULSE_DURATION	Interrupt pulse duration 0: Interrupt pulse duration is 100 µs 1: Interrupt pulse duration is 8 µs
5	-	Reserved
4	INT_ASYNC_RESET	0: The interrupt pulse is reset as soon as the interrupt status register is read if the pulse is still active. 1: The interrupt pulse remains high for the intended duration independent of when the interrupt status register is read. This is the default and recommended setting. In this case, when in ALP with the WUOSC clock, the clearing of the interrupt status register requires up to one ODR period after reading.
3:0	-	Reserved

16.6 SENSOR_CONFIG3

Name: SENSOR_CONFIG3
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	APEX_DISABLE	1: Disable APEX features to extend FIFO size to 2.25 Kbytes
5:0	-	Reserved

16.7 ST_CONFIG

Name: ST_CONFIG
Address: 19 (13h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	ST_NUMBER_SAMPLE	This bit selects the number of sensor samples that should be used to process self-test 0: 16 samples 1: 200 samples
5:3	ACCEL_ST_LIM	These bits control the tolerated ratio between self-test processed values and reference (fused) ones for accelerometer 000 to 110: Reserved 111: 50%
2:0	-	Reserved

16.8 SELFTEST

Name: SELFTEST
Address: 20 (14h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	ACCEL_ST_EN	1: Enable accel self-test operation. Host needs to program this bit to 0 to move device out of self-test mode. If host programs this bit to 0 while ST_BUSY = 1 and ST_DONE = 0, the current running self-test operation is terminated by host.
5:0	-	Reserved

16.9 INTF_CONFIG6

Name: INTF_CONFIG6
Address: 35 (23h)
Serial IF: R/W
Reset value: 0x7C

BIT	NAME	FUNCTION
7:5	-	Reserved
4	I3C_TIMEOUT_EN	0: I2C/I3C^{SM} timeout function not enabled 1: I2C/I3C^{SM} timeout function enabled
3	I3C_IBI_BYTE_EN	0: I3C^{SM} IBI payload function not enabled 1: I3C^{SM} IBI payload function enabled
2	I3C_IBI_EN	0: I3C^{SM} IBI function not enabled 1: I3C^{SM} IBI function enabled
1:0	-	Reserved

16.10 INTF_CONFIG10

Name: INTF_CONFIG10
Address: 37 (25h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	ASYNCTIME0_DIS	0: I3C^{SM}Asynchronous Mode 0 timing control is enabled 1: I3C^{SM} Asynchronous Mode 0 timing control is disabled
6:0	-	Reserved

16.11 INTF_CONFIG7

Name: INTF_CONFIG7
Address: 40 (28h)
Serial IF: R/W
Reset value: 0x0C

BIT	NAME	FUNCTION
7:4	-	Reserved
3	I3C_DDR_WR_MODE	This bit controls how I3C^{SM} slave treats the 1st 2-byte data from host in a DDR write operation. 0: (a) The 1st-byte in DDR-WR configures the starting register address where the write operation should occur. (b) The 2nd-byte in DDR-WR is ignored and dropped. (c) The 3rd-byte in DDR-WR will be written into the register with address specified by the 1st-byte. Or, the next DDR-RD will be starting from the address specified by the 1st-byte of previous DDR-WR. 1: (a) The 1st-byte in DDR-WR configures the starting register address where the write operation should occur. (b) The 2nd-byte in DDR-WR will be written into the register with address specified by the 1st-byte.
2:0	-	Reserved

16.12 OTP_CONFIG

Name: OTP_CONFIG
Address: 43 (2Bh)
Serial IF: R/W
Reset value: 0x06

BIT	NAME	FUNCTION
7:4	-	Reserved
3:2	OTP_COPY_MODE	00: Reserved 01: Enable copying OTP block to SRAM 10: Reserved 11: Enable copying self-test data from OTP memory to SRAM
1:0	-	Reserved

16.13 INT_SOURCE6

Name: INT_SOURCE6
Address: 47 (2Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	FF_INT1_EN	0: Freefall interrupt not routed to INT1 1: Freefall interrupt routed to INT1
6	LOWG_INT1_EN	0: Low-g interrupt not routed to INT1 1: Low-g interrupt routed to INT1
5	STEP_DET_INT1_EN	0: Step detect interrupt not routed to INT1 1: Step detect interrupt routed to INT1
4	STEP_CNT_OFL_INT1_EN	0: Step count overflow interrupt not routed to INT1 1: Step count overflow interrupt routed to INT1
3	TILT_DET_INT1_EN	0: Tilt detect interrupt not routed to INT1 1: Tile detect interrupt routed to INT1
2:0	-	Reserved

16.14 INT_SOURCE7

Name: INT_SOURCE7
Address: 48 (30h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	FF_INT2_EN	0: Freefall interrupt not routed to INT2 1: Freefall interrupt routed to INT2
6	LOWG_ INT2_EN	0: Low-g interrupt not routed to INT2 1: Low-g interrupt routed to INT2
5	STEP_DET_INT2_EN	0: Step detect interrupt not routed to INT2 1: Step detect interrupt routed to INT2
4	STEP_CNT_OFL_INT2_EN	0: Step count overflow interrupt not routed to INT2 1: Step count overflow interrupt routed to INT2
3	TILT_DET_INT2_EN	0: Tilt detect interrupt not routed to INT2 1: Tile detect interrupt routed to INT2
2:0	-	Reserved

16.15 INT_SOURCE8

Name: INT_SOURCE8
Address: 49 (31h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	PLL_RDY_IBI_EN	0: PLL ready interrupt not routed to IBI 1: PLL ready interrupt routed to IBI
3	UI_DRDY_IBI_EN	0: UI data ready interrupt not routed to IBI 1: UI data ready interrupt routed to IBI
2	FIFO_THS_IBI_EN	0: FIFO threshold interrupt not routed to IBI 1: FIFO threshold interrupt routed to IBI
1	FIFO_FULL_IBI_EN	0: FIFO full interrupt not routed to IBI 1: FIFO full interrupt routed to IBI
0	-	Reserved

16.16 INT_SOURCE9

Name: INT_SOURCE9
Address: 50 (32h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	I3C_PROTOCOL_ERROR_IBI_EN	0: I3C^{SM} protocol error interrupt not routed to IBI 1: I3C^{SM} protocol error interrupt routed to IBI
6	FF_IBI_EN	0: Freefall interrupt not routed to IBI 1: Freefall interrupt routed to IBI
5	LOWG_IBI_EN	0: Low-g interrupt not routed to IBI 1: Low-g interrupt routed to IBI
4	SMD_IBI_EN	0: SMD interrupt not routed to IBI 1: SMD interrupt routed to IBI
3	WOM_Z_IBI_EN	0: Z-axis WOM interrupt not routed to IBI 1: Z-axis WOM interrupt routed to IBI
2	WOM_Y_IBI_EN	0: Y-axis WOM interrupt not routed to IBI 1: Y-axis WOM interrupt routed to IBI
1	WOM_X_IBI_EN	0: X-axis WOM interrupt not routed to IBI 1: X-axis WOM interrupt routed to IBI
0	ST_DONE_IBI_EN	0: Self-test done interrupt not routed to IBI 1: Self-test done interrupt routed to IBI

16.17 INT_SOURCE10

Name: INT_SOURCE10
Address: 51 (33h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_IBI_EN	0: Step detect interrupt not routed to IBI 1: Step detect interrupt routed to IBI
4	STEP_CNT_OFL_IBI_EN	0: Step count overflow interrupt not routed to IBI 1: Step count overflow interrupt routed to IBI
3	TILT_DET_IBI_EN	0: Tilt detect interrupt not routed to IBI 1: Tile detect interrupt routed to IBI
2:0	-	Reserved

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16.18 APEX_CONFIG2

Name: APEX_CONFIG2
Address: 68 (44h)
Serial IF: R/W
Reset value: 0xA2

BIT	NAME	FUNCTION
7:4	LOW_ENERGY_AMP_TH_SEL	Threshold to select a valid step. Used to increase step detection for slow walk use case. 0000: 30 mg 0001: 35 mg 0010: 40 mg 0011: 45 mg 0100: 50 mg 0101: 55 mg 0110: 60 mg 0111: 65 mg 1000: 70 mg 1001: 75 mg 1010: 80 mg (default) 1011: 85 mg 1100: 90 mg 1101: 95 mg 1110: 100 mg 1111: 105 mg
3:0	DMP_POWER_SAVE_TIME_SEL	Duration of the period while the DMP stays awake after receiving a WOM event. 0000: 0 seconds 0001: 4 seconds 0010: 8 seconds (default) 0011: 12 seconds 0100: 16 seconds 0101: 20 seconds 0110: 24 seconds 0111: 28 seconds 1000: 32 seconds 1001: 36 seconds 1010: 40 seconds 1011: 44 seconds 1100: 48 seconds 1101: 52 seconds 1110: 56 seconds 1111: 60 seconds

16.19 APEX_CONFIG3

Name: APEX_CONFIG3
Address: 69 (45h)
Serial IF: R/W
Reset value: 0x85

BIT	NAME	FUNCTION
7:4	PED_AMP_TH_SEL	Threshold of step detection sensitivity. Low values increase detection sensitivity: reduce miss-detection. High values reduce detection sensitivity: reduce false-positive. 0000: 30 mg 0001: 34 mg 0010: 38 mg 0011: 42 mg 0100: 46 mg 0101: 50 mg 0110: 54 mg 0111: 58 mg 1000: 62 mg (default) 1001: 66 mg 1010: 70 mg 1011: 74 mg 1100: 78 mg 1101: 82 mg 1110: 86 mg 1111: 90 mg
3:0	PED_STEP_CNT_TH_SEL	Minimum number of steps that must be detected before step count is incremented. Low values reduce latency but increase false positives. High values increase step count accuracy but increase latency. 0000: 0 steps 0001: 1 step 0010: 2 steps 0011: 3 steps 0100: 4 steps 0101: 5 steps (default) 0110: 6 steps 0111: 7 steps 1000: 8 steps 1001: 9 steps 1010: 10 steps 1011: 11 steps 1100: 12 steps 1101: 13 steps 1110: 14 steps 1111: 15 steps

16.20 APEX_CONFIG4

Name: APEX_CONFIG4
Address: 70 (46h)
Serial IF: R/W
Reset value: 0x51

BIT	NAME	FUNCTION
7:5	PED_STEP_DET_TH_SEL	Minimum number of steps that must be detected before step event is signaled. Low values reduce latency but increase false positives. High values increase step event validity but increase latency. 000: 0 steps 001: 1 step 010: 2 steps (default) 011: 3 steps 100: 4 steps 101: 5 steps 110: 6 steps 111: 7 steps
4:2	PED_SB_TIMER_TH_SEL	Duration before algorithm considers that user has stopped taking steps. 000: 50 samples 001: 75 sample 010: 100 samples 011: 125 samples 100: 150 samples (default) 101: 175 samples 110: 200 samples 111: 225 samples
1:0	PED_HI_EN_TH_SEL	Threshold to classify acceleration signal as motion not due to steps. High values improve vibration rejection. Low values improve detection. 00: 87.89 mg 01: 104.49 mg (default) 10: 132.81 mg 11: 155.27 mg

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16.21 APEX_CONFIG5

Name: APEX_CONFIG5
Address: 71 (47h)
Serial IF: R/W
Reset value: 0x80

BIT	NAME	FUNCTION
7:6	TILT_WAIT_TIME_SEL	Minimum duration for which the device should be tilted before signaling event. 00: 0s 01: 2s 10: 4s (default) 11: 6s
5:3	LOWG_PEAK_TH_HYST_SEL	Hysteresis value added to the low-g threshold after exceeding it. 000: 31 mg (default) 001: 63 mg 010: 94 mg 011: 125 mg 100: 156 mg 101: 188 mg 110: 219 mg 111: 250 mg
2:0	HIGHG_PEAK_TH_HYST_SEL	Hysteresis value subtracted from the high-g threshold after exceeding it. 000: 31 mg (default) 001: 63 mg 010: 94 mg 011: 125 mg 100: 156 mg 101: 188 mg 110: 219 mg 111: 250 mg

16.22 APEX_CONFIG9

Name: APEX_CONFIG9
Address: 72 (48h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	FF_DEBOUNCE_DURATION_SEL	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. 0000: 0 ms 0001: 1250 ms 0010: 1375 ms 0011: 1500 ms 0100: 1625 ms 0101: 1750 ms 0110: 1875 ms 0111: 2000 ms 1000: 2125 ms (default) 1001: 2250 ms 1010: 2375 ms 1011: 2500 ms 1100: 2625 ms 1101: 2750 ms 1110: 2875 ms 1111: 3000 ms
3:1	SMD_SENSITIVITY_SEL	Parameter to tune SMD algorithm robustness to rejection, ranging from 0 to 4 (values higher than 4 are reserved). Low values increase detection rate but increase false positives. High values reduce false positives but reduce detection rate (especially for transport use cases). Default value is 0.
0	SENSITIVITY_MODE	Pedometer sensitivity mode 0: Normal (default) 1: Slow walk Slow walk mode improves slow walk detection (<1 Hz) but the number of false positives may increase.

16.23 APEX_CONFIG10

Name: APEX_CONFIG10
Address: 73 (49h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	LOWG_PEAK_TH_SEL	Threshold for accel values below which low-g state is detected. 00000: 31 mg (default) 00001: 63 mg 00010: 94 mg 00011: 125 mg 00100: 156 mg 00101: 188 mg 00110: 219 mg 00111: 250 mg 01000: 281 mg 01001: 313 mg 01010: 344 mg 01011: 375 mg 01100: 406 mg 01101: 438 mg 01110: 469 mg 01111: 500 mg 10000: 531 mg 10001: 563 mg 10010: 594 mg 10011: 625 mg 10100: 656 mg 10101: 688 mg 10110: 719 mg 10111: 750 mg 11000: 781 mg 11001: 813 mg 11010: 844 mg 11011: 875 mg 11100: 906 mg 11101: 938 mg 11110: 969 mg 11111: 1000 mg
2:0	LOWG_TIME_TH_SEL	Number of samples required to enter low-g state. 000: 1 sample (default) 001: 2 samples 010: 3 samples 011: 4 samples 100: 5 samples 101: 6 samples 110: 7 samples 111: 8 samples

16.24 APEX_CONFIG11

Name: APEX_CONFIG11
Address: 74 (4Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	HIGHG_PEAK_TH_SEL	Threshold for accel values above which high-g state is detected. 00000: 250 mg (default) 00001: 500 mg 00010: 750 mg 00011: 1000 mg 00100: 1250 mg 00101: 1500 mg 00110: 1750 mg 00111: 2000 mg 01000: 2250 mg 01001: 2500 mg 01010: 2750 mg 01011: 3000 mg 01100: 3250 mg 01101: 3500 mg 01110: 3750 mg 01111: 4000 mg 10000: 4250 mg 10001: 4500 mg 10010: 4750 mg 10011: 5000 mg 10100: 5250 mg 10101: 5500 mg 10110: 5750 mg 10111: 6000 mg 11000: 6250 mg 11001: 6500 mg 11010: 6750 mg 11011: 7000 mg 11100: 7250 mg 11101: 7500 mg 11110: 7750 mg 11111: 8000 mg
2:0	HIGHG_TIME_TH_SEL	Number of samples required to enter high-g state. 000: 1 sample (default) 001: 2 samples 010: 3 samples 011: 4 samples 100: 5 samples 101: 6 samples 110: 7 samples 111: 8 samples

16.25 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR
Address: 75 (4Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_X_TH	Threshold value for the Wake on Motion Interrupt for X-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9 mg

16.26 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR
Address: 76 (4Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_Y_TH	Threshold value for the Wake on Motion Interrupt for Y-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9 mg

16.27 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR
Address: 77 (4Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_Z_TH	Threshold value for the Wake on Motion Interrupt for Z-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9 mg

16.28 OFFSET_USER4

Name: OFFSET_USER4
Address: 82 (52h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_X_OFFUSER[11:8]	Upper bits of X-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.
3:0	Reserved	Reserved

16.29 OFFSET_USER5

Name: OFFSET_USER5
Address: 83 (53h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_X_OFFUSER[7:0]	Lower bits of X-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.

16.30 OFFSET_USER6

Name: OFFSET_USER6
Address: 84 (54h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Y_OFFUSER[7:0]	Lower bits of Y-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.

16.31 OFFSET_USER7

Name: OFFSET_USER7
Address: 85 (55h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_Z_OFFUSER[11:8]	Upper bits of Z-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.
3:0	ACCEL_Y_OFFUSER[11:8]	Upper bits of Y-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.

16.32 OFFSET_USER8

Name: OFFSET_USER8
Address: 86 (56h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Z_OFFUSER[7:0]	Lower bits of Z-accel offset programmed by user. Max value is ±1g, resolution is 0.5 mg.

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16.33 ST_STATUS1

Name: ST_STATUS1
Address: 99 (63h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	ACCEL_ST_PASS	1: Accel self-test passed for all the 3 axes
4	ACCEL_ST_DONE	1: Accel self-test done for all the 3 axes
3	AZ_ST_PASS	1: Accel Z-axis self-test passed
2	AY_ST_PASS	1: Accel Y-axis self-test passed
1	AX_ST_PASS	1: Accel X-axis self-test passed
0	-	Reserved

16.34ST_STATUS2

Name: ST_STATUS2
Address: 100 (64h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	ST_INCOMPLETE	1: Self-test is incomplete. This bit is set to 1 if the self-test was aborted.
5:0	-	Reserved

16.35 FDR_CONFIG

Name: FDR_CONFIG
Address: 102 (66h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	FDR_SEL	FIFO packet rate decimation factor. Sets the number of discarded FIFO packets. User must disable sensors when initializing FDR_SEL value or making changes to it. 0xxx: Decimation is disabled, all packets are sent to FIFO 1000: 1 packet out of 2 is sent to FIFO 1001: 1 packet out of 4 is sent to FIFO 1010: 1 packet out of 8 is sent to FIFO 1011: 1 packet out of 16 is sent to FIFO 1100: 1 packet out of 32 is sent to FIFO 1101: 1 packet out of 64 is sent to FIFO 1110: 1 packet out of 128 is sent to FIFO 1111: 1 packet out of 256 is sent to FIFO

16.36 APEX_CONFIG12

Name: APEX_CONFIG12
Address: 103 (67h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	FF_MAX_DURATION_SEL	Maximum freefall length. Longer freefalls are ignored. 0000: 102 cm (default) 0001: 120 cm 0010: 139 cm 0011: 159 cm 0100: 181 cm 0101: 204 cm 0110: 228 cm 0111: 254 cm 1000: 281 cm 1001: 310 cm 1010: 339 cm 1011: 371 cm 1100: 403 cm 1101: 438 cm 1110: 473 cm 1111: 510 cm
3:0	FF_MIN_DURATION_SEL	Minimum freefall length. Shorter freefalls are ignored. 0000: 10 cm (default) 0001: 12 cm 0010: 13 cm 0011: 16 cm 0100: 18 cm 0101: 20 cm 0110: 23 cm 0111: 25 cm 1000: 28 cm 1001: 31 cm 1010: 34 cm 1011: 38 cm 1100: 41 cm 1101: 45 cm 1110: 48 cm 1111: 52 cm

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17 USER BANK MREG2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank MREG2. The procedure for accessing MREG2 registers is described in section 13.

17.1 OTP_CTRL7

Name: OTP_CTRL7
Address: 06 (06h)
Serial IF: RWS
Reset value: 0x06 (initial reset value is 0x0C, it changes to 0x06 after OTP load completes)

BIT	NAME	FUNCTION
7:4	-	Reserved
3	OTP_RELOAD	Setting this bit to 1 triggers OTP copy operation.
2	-	Reserved
1	OTP_PWR_DOWN	0: Power up OTP to copy from OTP to SRAM 1: Power down OTP This bit is automatically set to 1 when OTP copy operation is complete.
0	-	Reserved

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18 USER BANK MREG3 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank MREG3. The procedure for accessing MREG3 registers is described in section 13.

18.1 XA_ST_DATA

Name: XA_ST_DATA
Address: 00 (00h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	XA_ST_DATA	Accel X-axis factory trimmed self-test response.

18.2 YA_ST_DATA

Name: YA_ST_DATA
Address: 01 (01h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	YA_ST_DATA	Accel Y-axis factory trimmed self-test response.

18.3 ZA_ST_DATA

Name: ZA_ST_DATA
Address: 02 (02h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ZA_ST_DATA	Accel Z-axis factory trimmed self-test response.

19 SMARTMOTION PRODUCT FAMILY

ICM-42370-P is a member of the SmartMotion™ family of MEMS motion sensors with 1-, 2-, 3-, 7-, and 9-axis IMU platforms addressing the emerging need of many mass-market consumer applications via improved performance, accuracy, and intuitive motion and gesture-based interfaces.

For more information, please visit invensense.tdk.com.

20 REFERENCE

Please refer to the following application notes for additional information.

- IMU PCB Design and MEMS Assembly Guidelines (AN-000393)
- Understanding IMU Sensor Offset (AN-000257)
- ICM-42607x DMP Mode Accelerometer
- ICM-42607x/42670x Products PCB Board Design Guide (AN-000262)
- TDK InvenSense IMU Calibration Application Note (AN-000265)
- ICM-42607x/42670x Accelerometer Low Power Mode Implementation (AN-000266)
- ICM-42607x and ICM-42670x Errata (AN-000273)

21 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
07/31/2023	1.0	Initial Release

TDK InvenSense