ICM-42607x, ICM-42670x and ICM-42370x Accelerometer Low Power Mode Implementation

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1 INTRODUCTION

In addition to low noise (LN) mode, ICM-42607x, ICM-42670x and ICM-42370x support low power (LP) mode. The LP mode consumes very little power, which is a useful mode for power sensitive applications, such as always-on wearable devices.

This application note describes how to bring the accel to LP mode, how to switch from LP mode to LN mode, and LP mode performance.

2 ACCELEROMETER LP MODE CONFIGURATIONS AFTER RESET

Accel LP mode operates as duty cycle mode. There are two internal clock sources that can be selected for the Accel LP mode inactive time, Wake-Up oscillator clock (6.4 kHz) and RC oscillator clock (4 MHz).

Before enabling Accel LP mode, ACCEL_UI_AVG must be selected for averaging filter setting to create Accelerometer output.

After part soft reset, the configuration register settings are listed as below.

2.1 ACCEL_UI_AVG (BANK0 REGISTER 0X24 BIT 6:4)

The ACCEL_UI_AVG cannot be changed when Accel LP mode is selected. It must be set before LP mode is enabled.

The higher the averaging number is, the lower the noise level and the higher the power consumption are.

Name: ACCEL_CONFIG1 **Address: 36 (24h)** **OTP: 1** **Reset value: 1h 00000001b**			
BIT	ACCESS	NAME	DESCRIPTION
[6:4]	read-write	accel_ui_avg_ind	LPM number of averaged ADC samples to generate output sample 0 -: 2 averaged samples 1 -: 4 averaged samples 2 -: 8 averaged samples 3 -: 16 averaged samples 4 -: 32 averaged samples 5 -: 64 averaged samples 6 -: 64 averaged samples 7 -: 64 averaged samples This field cannot be changed when the accel sensor is in LPM

2.2 ACCEL_ODR (BANK0 REGISTER 0X21 BIT 3:0)

The highest ODR for Accel LP mode is 400 Hz.

When using APEX function, the ACCEL_ODR must be configured to an ODR equal or greater to the DMP_ODR (Bank0, register 0x26, bit 1:0) for correct device operation.

Name: ACCEL_CONFIG0
Address: 33 (21h)
OTP: 0
Reset value: 6h 00000110b

BIT	ACCESS	NAME	DESCRIPTION
[3:0]	read-write	accel_odr	0 : N/A 1 -: N/A 2 -: N/A 3 -: N/A 4 -: N/A 5 -: 1.6k (LN only) 6 -: 800 (default, LN only) 7 -: 400 8 -: 200 9 -: 100 10 -: 50 11 -: 25 12 -: 12.5 13 -: 6.25 (LP only) 14 -: 3.125 (LP only) 15 -: 1.5625 (LP only) This field can be changed on-the-fly when accel sensor is already on

2.3 ACCEL_LP_CLK_SEL (BANK0 REGISTER 0X1F BIT 7)

Configure Accel LP mode clock source from Wake-Up oscillator clock or RC oscillator clock. Using Wake-Up oscillator will consume less power than using RC oscillator. But when using Wake-Up oscillator, a special sequence is required to switch the mode from LP to LN. This will be discussed in section 3.

Name: PWR_MGMT_0
Address: 31 (1fh)
OTP: 1
Reset value: 0h 00000000b

BIT	ACCESS	NAME	DESCRIPTION
[7]	read-write	accel_lp_clk_sel	0: Accelerometer LP mode uses Wake Up oscillator clock. This is the lowest power consumption mode and it is the recommended setting. 1: Accelerometer LP mode uses RC oscillator clock. This field can be changed on-the-fly even if accel sensor is already on

2.4 ACCEL_MODE (BANK0 REGISTER 0X1F BIT 1:0)

Set the ACCEL_MODE with binary 10 to place the Accel to LP mode.

Name: PWR_MGMT_0 **Address: 31 (1fh)** **OTP: 1** **Reset value: 0h 00000000b**			
BIT	ACCESS	NAME	DESCRIPTION
[1:0]	read-write	accel_mode	Accel_mode[1:0] 00: OFF 01: OFF 10: LPM 11: LNM Notes: - when selecting LP Mode please refer to “accel_lp_clk_sel” setting, bit[7] of this register. - before entering and during LP Mode the following combinations of ODR and averaging are not permitted: 1) ODR=1600 Hz and ODR=800 Hz: any averaging. 2) ODR=400 Hz: averaging=16, 32 or 64. 3) ODR=200 Hz: averaging=64. - when transitioning from OFF to LPM/LNM, do not issue any register writes for 200 µs. For details, please see use notes. This field can be changed on-the-fly even if accel sensor is already on

3 CHANGE ACCEL MODE FROM LP TO LN WHEN USING WAKE-UP OSCILLATOR

If accel is in LP with RCosc, the user can trigger a change toward accel LN mode at any time. The mode change will take effect on the next ODR.

When accel is in LP mode with WUosc, before changing it to LN mode, it is necessary to change the LP mode clock source from WUosc to RCosc and wait for 1 ODR period.

ALP+WUosc mode ➔ ALP+RCosc mode ➔ wait for one Accel ODR period **➔ all other power modes**

3.1 ENABLE IDLE (BANK0 REGISTER 0X1F BIT 4)

Set IDLE bit to 1 and keep the LP mode setting (ACCEL_MODE=10).

Name: PWR_MGMT_0
Address: 31 (1fh)
OTP: 1
Reset value: 0h 00000000b

BIT	ACCESS	NAME	DESCRIPTION
[4]	read-write	idle	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state since the RC oscillator will also be powered off. This field can be changed on-the-fly even if a sensor is already on
[1:0]	read-write	accel_mode	Accel mode[1:0] 00: OFF 01: OFF 10: LPM 11: LNM When transitioning from OFF to LPM/LNM, do not issue any register writes for 200 µs. For details, please see use notes. This field can be changed on-the-fly even if accel sensor is already on

3.2 INT_SOURCE0 (BANK0 REGISTER 0X2B BIT 7:0)

Disable all interrupt sources. Set 0x00 to the INT_SOURCE0 register.

Name: INT_SOURCE0
Address: 43 (2bh)
OTP: 1
Reset value: 10h 00010000b

BIT	ACCESS	NAME	DESCRIPTION
[7]	read-write	int_st_done_int1_en	Self-Test Done interrupt source enable – Interrupt output 1 0 : Disabled 1 : Enabled
[6]	read-write	int_fsync_int1_en	UI FSYNC Interrupt source enable for int1
[5]	read-write	int_pll_rdy_int1_en	PLL RDY Interrupt source enable for int1
[4]	read-write	int_reset_done_int1_en	RESET DONE Interrupt source enable for int1
[3]	read-write	int_drdy_int1_en	UI DRDY Interrupt source enable for int1
[2]	read-write	int_fifo_ths_int1_en	FIFO THS Interrupt source enable for int1
[1]	read-write	int_fifo_full_int1_en	FIFO FULL Interrupt source enable for int1 To avoid FIFO interrupts while reading FIFO, this bit needs to be disabled while reading FIFO. Please see use notes for details
[0]	read-write	int_agc_rdy_int1_en	AGC RDY Interrupt source enable for int1

3.3 ACCEL_ODR (BANK0 REGISTER 0X21 BIT 3:0)

Change ACCEL_ODR for LN mode ODR based on customer application.

Name: ACCEL_CONFIG0 **Address: 33 (21h)** **OTP: 0** **Reset value: 6h 00000110b**			
BIT	ACCESS	NAME	DESCRIPTION
[3:0]	read-write	accel_odr	0 -: N/A 1 -: N/A 2 -: N/A 3 -: N/A 4 -: N/A 5 -: 1.6k (LN only) 6 -: 800 (default, LN only) 7 -: 400 8 -: 200 9 -: 100 10 -: 50 11 -: 25 12 -: 12.5 13 -: 6.25 (LP only) 14 -: 3.125 (LP only) 15 -: 1.5625 (LP only) This field can be changed on-the-fly when accel sensor is already on

3.4 ACCEL_MODE (BANK0 REGISTER 0X1F BIT 1:0)

Set ACCEL_MODE=11 (LN mode) and keep IDLE bit to 1.

Name: PWR_MGMT_0 **Address: 31 (1fh)** **OTP: 1** **Reset value: 0h 00000000b**			
BIT	ACCESS	NAME	DESCRIPTION
[4]	read-write	idle	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state since the RC oscillator will also be powered off. This field can be changed on-the-fly even if a sensor is already on
[1:0]	read-write	accel_mode	Accel_mode[1:0] 00: OFF 01: OFF 10: LPM 11: LNM When transitioning from OFF to LPM/LNM, do not issue any register writes for 200 µs. For details, please see use notes. This field can be changed on-the-fly even if accel sensor is already on

3.5 INT_SOURCE0 (BANK0 REGISTER 0X2B BIT 7:0)

Enable interrupt source based on customer application.

Name: INT_SOURCE0 **Address: 43 (2bh)** **OTP: 1** **Reset value: 10h 00010000b**			
BIT	ACCESS	NAME	DESCRIPTION
[7]	read-write	int_st_done_int1_en	Self-Test Done interrupt source enable – Interrupt output 1 0 : Disabled 1 : Enabled
[6]	read-write	int_fsync_int1_en	UI FSYNC Interrupt source enable for int1
[5]	read-write	int_pll_rdy_int1_en	PLL RDY Interrupt source enable for int1
[4]	read-write	int_reset_done_int1_en	RESET DONE Interrupt source enable for int1
[3]	read-write	int_drdy_int1_en	UI DRDY Interrupt source enable for int1
[2]	read-write	int_fifo_ths_int1_en	FIFO THS Interrupt source enable for int1
[1]	read-write	int_fifo_full_int1_en	FIFO FULL Interrupt source enable for int1 To avoid FIFO full interrupts while reading FIFO, this bit needs to be disabled while reading FIFO. Please see use notes for details
[0]	read-write	int_agc_rdy_int1_en	AGC RDY Interrupt source enable for int1

3.6 DISABLE IDLE (BANK0 REGISTER 0X1F BIT 4)

Set IDLE bit to 0 and keep the LN mode setting (ACCEL_MODE=11).

Name: PWR_MGMT_0 **Address: 31 (1fh)** **OTP: 1** **Reset value: 0h 00000000b**			
BIT	ACCESS	NAME	DESCRIPTION
[4]	read-write	idle	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state since the RC oscillator will also be powered off. This field can be changed on-the-fly even if a sensor is already on
[1:0]	read-write	accel_mode	Accel_mode[1:0] 00: OFF 01: OFF 10: LPM 11: LNM When transitioning from OFF to LPM/LNM, do not issue any register writes for 200 µs. For details, please see use notes. This field can be changed on-the-fly even if accel sensor is already on

3.7 AN EXAMPLE

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1.  SIGNAL_PATH_RESET (0x02)  <- 0x10 (SIGNAL_PATH_RESET=1)
2.  ACCEL_CONFIG1 (0x24)      <- 0x01 (ACCCEL_UI_AVG=2x, ACCEL_UI_FILT_BW=180Hz)
3.  ACCEL_CONFIG0 (0x21)      <- 0x4E (ACCEL_UI_FS_SEL=4g, ACCEL_ODR=3.125Hz)
4.  INT_SOURCE0 (0x2B)        <- 0x08 (DRDY_INT1_EN=1)
5.  PWR_MGMT0 (0x1F)          <- 0x02 (ACCEL_MODE=LP)
6.  <Wait for 3 sec>
7.  PWR_MGMT0 (0x1F)          <- 0x12 (ACCEL_MODE=LP, IDLE=1)
8.  INT_SOURCE0 (0x2B)        <- 0x00 (All interrupt source off)
9.  ACCEL_CONFIG0 (0x21)      <- 0x46 (ACCEL_UI_FS_SEL=4g, ACCEL_ODR=800Hz)
10. PWR_MGMT0 (0x1F)          <- 0x13 (ACEL_MODE=LN, IDLE=1)
11. INT_SOURCE0 (0x2B)        <- 0x08 (DRDY_INT1_EN=1)
12. PWR_MGMT0 (0x1F)          <- 0x03 (ACEL_MODE=LN)
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4 ACCELEROMETER LP MODE POWER CONSUMPTION AND NOISE LEVEL

The table below shows Accel LP mode setting and performance. The power consumption value is derived from validation or characterization of parts with ACCEL_LP_CLK_SEL set to 0.

	ACCEL_UI_AVG	000	001	010	011	100	101
	Averages	2	4	8	16	32	64
	Noise (mg-rms)	6.2	4.4	3.1	2.2	1.56	1.1
ACCEL_ODR	ODR (Hz)	Power consumption, Idd (uA)					
1111	1.5625	4.4	4.4	4.5	4.7	5.2	6.1
1110	3.125	4.8	4.9	5.1	5.5	6.4	8.2
1101	6.25	5.5	5.7	6.1	7	8.8	12.5
1100	12.5	6.9	7.4	8.3	10.1	13.7	20.9
1011	25	9.8	10.7	12.5	16.1	23.3	37.8
1010	50	15.6	17.4	21	28.2	42.7	71.6
1001	100	27.2	30.8	38	52.5	81.3	139.1
1000	200	50.5	58	72	101	159	NA
0111	400	97	111	140	NA	NA	NA

5 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
01/05/2021	1.0	Initial Release
10/17/2023	1.1	Included part number ICM-42370x
01/24/2024	1.2	Removed ‘L2 Internal’ from the header and updated the legal information