IAM-20680XX FIFO usage

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1 FIFO OVERVIEW

The IAM-20680XX devices contain a 4096-byte FIFO register that is accessible via the Serial Interface (either SPI or I^2C). The FIFO configuration register determines which data are written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data are available.

1.1. FIFO SIZE

FIFO size can be selected by bit 7:6 in register ACCEL_CONFIG2 (0x1D), according to the following coding:

ACCEL_CONFIG2 Bit	Signal	Value
[7:6]	FIFO_SIZE[1:0]	00b = 512 Byte 01b = 1 kByte 10b = 2 kByte 11b = 4 kByte

Table 1. FIFO size selection bit

Note: In IAM-20680, the usage of FIFO size larger than 512 bytes is not recommended.

1.2. FIFO COUNTER

FIFO counter is split into two registers, FIFO_COUNTH (0x72) and FIFO_COUNTL (0x73), containing namely the high and the low bits of the total number of written bytes in the FIFO. When data is read from FIFO, counter value decrements, while it increments when new data are being written in the FIFO.

1.3. FIFO READ

Data stored in the FIFO is available in register FIFO_R_W (0x74). Data is written to the FIFO in the same order of sensor's registers addresses (from lowest to highest). If all the FIFO enable flags (see section 2) are enabled, the contents of registers 0x3B through 0x48 will be written in the same order, at the Sample Rate. The contents of the sensors data registers (Registers 0x3B to 0x48) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN register (0x23).
If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0x00 until new data is available.

1.4. FIFO OVERFLOW

FIFO overflow has the following two modes, selectable by Bit 6 in register CONFIG (0x1A):

- **FIFO_MODE = 0:** when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data (oldest data lost).
- **FIFO_MODE = 1:** when the FIFO is full, additional writes will not be written to the FIFO (newest data lost).

1.4.1. FIFO Overflow interrupt

When FIFO is full, an interrupt signal on INT pin can be generated if the relative enable signal - bit 4 in register INT_ENABLE (0x38) – is set:

- **FIFO_OFLOW_EN=0:** function is disabled.
- **FIFO_OFLOW_EN=1:** Enables a FIFO buffer overflow to generate an interrupt.

If the FIFO buffer has overflowed, the status bit FIFO_OFLOW_INT – bit 4 in INT_STATUS (0x3A) - is automatically set to 1 and will be reset on read.

2 REGISTERS SUMMARY

This section provides a summary of the registers involved in the FIFO usage, listed in address order.

Register	address	bit	Signal	Function
CONFIG	0x1A	6	FIFO_MODE	When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.
ACCEL_CONFIG2[1]	0x1D	7:6	FIFO_SIZE	0 = 512 Byte 1 = 1 kByte 2 = 2 kByte 3 = 4 kByte
FIFO_EN[2]	0x23	7	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate. 0 – Function is disabled.
		6	XG_FIFO_EN	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
		5	YG_FIFO_EN	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
		4	ZG_FIFO_EN	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate. 0 – Function is disabled
		3	ACCEL_FIFO_EN	1 – Write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate; 0 – Function is disabled.
INT_ENABLE	0x38	4	FIFO_OFLOW_EN	1 – Enables a FIFO buffer overflow to generate an interrupt. 0 – Function is disabled.
INT_STATUS	0x3A	4	FIFO_OFLOW_INT	This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read.
USER_CTRL	0x6A	6	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register.
		2	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
PWR_MGMT_2	0x6C	7	FIFO_LP_EN	1 – Enable FIFO in low-power/WoM accelerometer mode. Default setting is 0.
FIFO_COUNTH	0x72	4:0	FIFO_COUNT[12:8]	High Bits; count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.
FIFO_COUNTL	0x73	7:0	FIFO_COUNT[7:0]	Low Bits; count indicates the number of written bytes in the FIFO. Note: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.
FIFO_R_W	0x74	7:0	FIFO_DATA	Read/Write command provides Read or Write operation for the FIFO.

Table 2. FIFO related registers summary

[1] In IAM-20680, the usage of FIFO size larger than 512 bytes is not recommended.

[2] Enabling any one of the bits corresponding to the Gyros or Temp data paths, data are buffered into the FIFO even though that data path is not enabled.

2.1. NORMAL MODE REGISTERS SETUP

The setup proposed hereafter allows IAM-20680XX to store all sensors data in a 4kbytes FIFO[3] with ODR=1kHz; when FIFO is full, new data shall not be written (FIFO_MODE=1). Prerequisite is the device being already powered up, not in SLEEP mode and all sensors (Gyros, Accelerometers and Temperature) are correctly operating with ODR=1kHz. FIFO overflow time shall be ~0.29s; an interrupt pulse will be generated on INT pin and INT_STATUS register will flag the overflow in bit 4.

Address	***Value***	***Name***	***Comment***
0x23	0x00	FIFO_EN	disable all FIFO buffering
0x1D	0xC0	ACCEL_CONFIG_2	set FIFO size=4k
0x6A	0x45	USER_CTRL	enable FIFO operation mode, reset FIFO, reset all sensors
0x1A	0x42	CONFIG	set FIFO mode=1 (no additional write on overflow)
0x38	0x10	INT_ENABLE	enable FIFO_OVERFLOW interrupt
0x23	0xFE	FIFO_EN	enable FIFO buffering (all sensors)

2.2. LOW POWER MODE REGISTERS SETUP

The setup proposed hereafter allows IAM-20680XX to store all sensors data in a 4kbytes FIFO[4] with ODR=1kHz in Low Power Mode. Prerequisite is the device being already powered up, not in SLEEP mode and all sensors (Gyros, Accelerometers and Temperature) are correctly operating with ODR=1kHz and WoM function enabled. When the Accelerometers detect activity, data are stored in the FIFO at the programmed ODR. The interval before the interrupt generator cannot be foreseen.

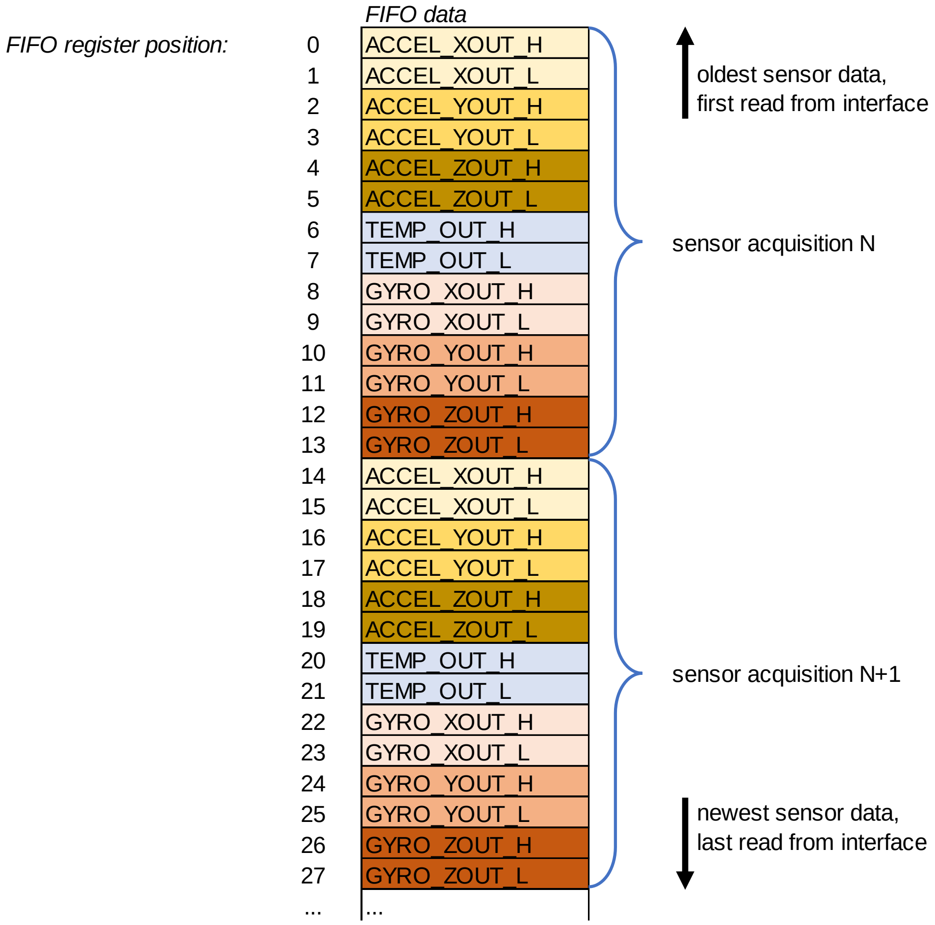
Address	***Value***	***Name***	***Comment***
0x23	0x00	FIFO_EN	disable all FIFO buffering
0x6C	0x80	PWR_MGMT_2	enable FIFO in Low Power mode
0x6A	0x45	USER_CTRL	enable FIFO operation mode, reset FIFO, reset all sensors
0x1A	0x42	CONFIG	set FIFO mode=1 (no additional write on overflow)
0x38	0x10	INT_ENABLE	enable FIFO_OVERFLOW interrupt
0x23	0xF8	FIFO_EN	enable FIFO buffering (all sensors)
0x6B	0x21	PWR_MGMT_1	enable Accelerometer Cycle mode

[3] In IAM-20680, FIFO size >512bytes is not tested nor guaranteed

[4] In IAM-20680, FIFO size >512bytes is not tested nor guaranteed

2.3. DATA STORED IN FIFO

Data from sensors is written in the FIFO according to the following figure:



FIFO register position:	FIFO data
0	ACCEL_XOUT_H
1	ACCEL_XOUT_L
2	ACCEL_YOUT_H
3	ACCEL_YOUT_L
4	ACCEL_ZOUT_H
5	ACCEL_ZOUT_L
6	TEMP_OUT_H
7	TEMP_OUT_L
8	GYRO_XOUT_H
9	GYRO_XOUT_L
10	GYRO_YOUT_H
11	GYRO_YOUT_L
12	GYRO_ZOUT_H
13	GYRO_ZOUT_L
14	ACCEL_XOUT_H
15	ACCEL_XOUT_L
16	ACCEL_YOUT_H
17	ACCEL_YOUT_L
18	ACCEL_ZOUT_H
19	ACCEL_ZOUT_L
20	TEMP_OUT_H
21	TEMP_OUT_L
22	GYRO_XOUT_H
23	GYRO_XOUT_L
24	GYRO_YOUT_H
25	GYRO_YOUT_L
26	GYRO_ZOUT_H
27	GYRO_ZOUT_L
...	...

Figure 1. FIFO data structure

3 FIFO READING STRATEGY

FIFO content can be read in any moment through the serial interface, either I2C or SPI. However, if the sensors are generating data during the reading process, and thus storing it in the FIFO, concurrent accesses to the structure might generate conflict, leading to unpredictable results (i.e.: data corruption, data loss, etc.).
Moreover, when FIFO overflow interrupt occurs and sensors are still generating data, some data bytes might possibly be lost (according to the selected FIFO_MODE, they can be either the newest or the oldest ones) if the FIFO isn't flushed in time.
For these reasons, strongly suggested applicative solution is to always empty the FIFO completely within 1 ODR period; however, being reading duration limited by the interface speed, restrictions shall be defined on ODR frequency and/or FIFO depth.
Sections 3.2 and 3.3 will describe some possible implementations.

3.1. FIFO BURST READ

Emptying FIFO requires multiple accesses to FIFO_R_W register (0x74). Normally, this would mean to send a Read command, followed by the register address. Burst read feature allows to save interface time and thus speed up FIFO dumping process, by avoiding the MCU to continuously repeat the address register. This is realized by sending, under a single low-CS pulse, the read + address frame, followed by as many 0x00 bytes as the FIFO size, as illustrated in Figure 2 and Figure 3.

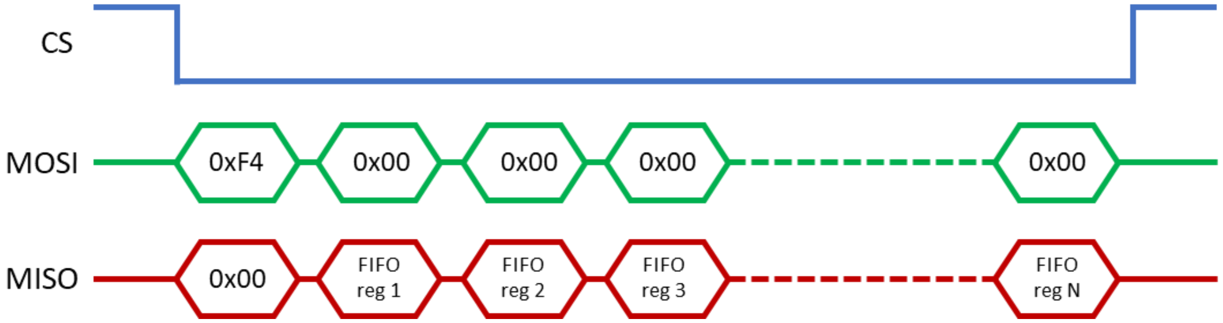
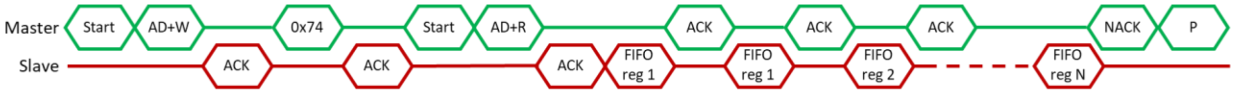


Figure 2. FIFO burst read, SPI interface



Start = start condition (SDA goes from H to L while SCL is H)
AD = I^{2}C slave address
W = write bit (0); R = read bit (1)
ACK = Acknowledge (SDA is low while SCL is H at the 9-th clock cycle)
NACK = Not Acknowledge (SDA is H at the 9-th clock cycle)
P = stop condition (SDA goes from L to H while SCL is H)

Figure 3. FIFO burst read, I2C interface

3.2. OVERFLOW READING, NO FIFO INTERRUPTION

An external MCU can be triggered by Overflow interrupt signal, through INT pin, to start FIFO dump process. Using SPI interface and according to the burst read strategy described in section 3.1, if N is the FIFO size, a complete dump shall require the exchange of N+1 bytes of data. Following table summarizes the expected reading time assuming usage of the maximum allowed interface speed (8 MHz), and the corresponding maximum allowed ODR value to allow FIFO emptying before new data are generated (red squares indicates the ODR value isn't allowed).

FIFO size [bytes]	FIFO dump time [ms]	ODR [Hz]						
		1000	500	100	50	10	5	
512	0.513	1	2	10	20	100	200	ODR period [ms]
1024	1.025	1	2	10	20	100	200	
2048	2.049	1	2	10	20	100	200	
4096	4.097	1	2	10	20	100	200	

Table 3. maximum allowed ODR using 8MHz SPI interface

In the same way, following table summarizes the maximum allowed ODR values, when using I2C interface at the maximum supported speed (400 kHz).

FIFO size [bytes]	FIFO dump time [ms]	ODR [Hz]						
		1000	500	100	50	10	5	
512	11.595	1	2	10	20	100	200	ODR period [ms]
1024	23.115	1	2	10	20	100	200	
2048	46.155	1	2	10	20	100	200	
4096	92.235	1	2	10	20	100	200	

Table 4. maximum allowed ODR using 400kHz I2C interface

3.3. OVERFLOW READING, FIFO INTERRUPTION

When Overflow interrupt signal arises, to have more time fro FIFO content dumping, and only if sensors data interruption is acceptable for the application, an easy solution is to temporarily stop FIFO population until the dump process is complete.

This can be achieved by resetting all the sensors enable bits in register FIFO_EN:

- TEMP_FIFO_EN
- XG_FIFO_EN
- YG_FIFO_EN
- ZG_FIFO_EN
- ACCEL_FIFO_EN

At the completion of reading process, the above signals must be re-enabled to keep using FIFO functionality.

4 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/03/2022	1.0	Template change 1st release

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