IAM-20680xx - WoM User Guide

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1 PURPOSE AND SCOPE

An application of TDK-InvenSense motion sensors is motion detection for low power operation of applications processor. The products of the IAM-20680xx 6-Axes family have a programmable interrupt system which can generate an interrupt signal on the INT pin. One of the interrupt system provides motion detection capability, Wake-on-Motion (WoM).

This document will explain the details on how to use WoM with IAM-20680xx and supplement to the WoM functions to provide the base understanding that customers need.

2 WHY USING WAKE-ON-MOTION

WoM detects motion when accelerometer data exceeds a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
For example, a possible Automotive application (*theft-attempt detection*) is represented in Figure 1. When the car is parked, host processor generally wants to enter standby mode to save power consumption. In case of a theft attempt, car might be lifted, thus inducing an acceleration on any of the IMU axes. As a wake-event, if an acceleration is detected compared to any time frame, then IMU asserts interruption signal from INT pin as an event. By receiving the signal, HOST can be enabled and then can read IMU information or other processing can be implemented.

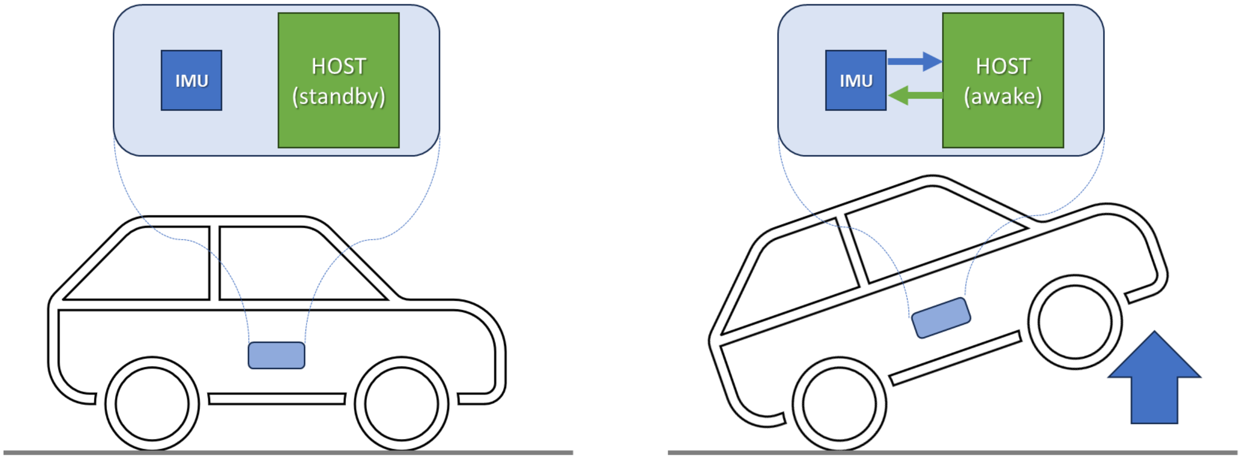

Figure 1. WOM mode for anti-theft application

3 WAKE-ON-MOTION ENABLE SEQUENCE

This section describes the necessary steps to enable WOM functionality in IAM-20680xx products. For details concerning the typical application schematic and necessary components, please refer to the product datasheet.

Step 1: Initialize all configurations

- In PWR_MGMT_1 register (0x6B) set DEVICE_RESET = 1 (the bit will reset to 0 automatically)

Step 2: Ensure that Accelerometers, Gyroscopes and WOM function are disabled

- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = STBY_XG = STBY_YG = STBY_ZG = 1

Step 3: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D):
  - ➢ set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = b111
  - ➢ set DEC2_CFG according to the desired averaging factor (refer to datasheet for DEC2_CFG values)

Step 4: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_INT_EN[2:0] = b111 to enable motion interrupt

Once triggered, WOM interrupt is generated on INT pin (if INT2_EN bit is set to 0 for IAM-20680HT) or on INT2 pin (if INT2_EN is set to 1 for IAM-20680HT)

Step 5: Set Motion Threshold

- In ACCEL_WOM_THR register (0x1F) set the desired motion threshold (1lsb = 4mg, regardless of the selected full-scale)

Step 6: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69):
  - ➢ set ACCEL_INTEL_EN = 1 to enable the Wake-on-Motion detection logic
  - ➢ choose ACCEL_INTEL_MODE = 0 or 1 to select the detection mode. (see sections 4.1.1, 4.1.2)
  - ➢ ensure bit 0 is set to 0.

Step 7: Set Accelerometer WoM ODR Selection

- In LP_MODE_CFG register (0x1E) set ACCEL_WOM_ODR_CTRL[3:0] (refer to datasheet for ACCEL_WOM_ODR_CTRL values)

Step 8: Enable Accelerometers and WoM Mode

- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1
- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 1

4 WAKE-ON-MOTION CONFIGURATIONS

Some of key behavior for Wake-on-Motion are described in this section for better understanding.

4.1. WOM TRIGGERING MODE SETTING BY ACCEL_INTEL_MODE

Wake-On-Motion interrupt is generated when, on any of the three axes, the difference between acceleration measured by the axis and a reference value exceeds the threshold specified in the configuration phase. User can select between two detection modes, based on the reference value considered:

- Mode 0: Absolute acceleration (measured acceleration value is compared to the value sampled at the activation of WOM functionality)
- Mode 1: Relative acceleration (measured acceleration value is compared to the immediately previous value sampled)

4.1.1. ACCEL_INTEL_MODE[6] = 0

Compares the current sample to the first sample taken when entering in WoM by ACCEL_INTEL_EN = 1.

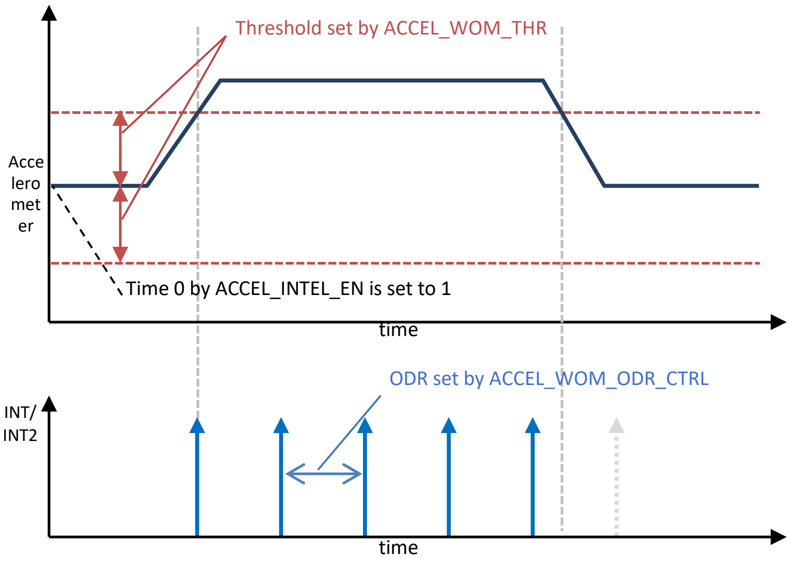
Threshold set by ACCEL_WOM_THR
Acce
lero
met
er
Time 0 by ACCEL_INTEL_EN is set to 1
time
ODR set by ACCEL_WOM_ODR_CTRL
INT/
INT2
time

Figure 2. waveform at ACCEL_INTEL_MODE = 0

4.1.1.1. reset accelerometer first sample value

To re-initialize the reference accelerometer value to be compared with the current sample, it is required to repeat the enabling sequence described in section 3.

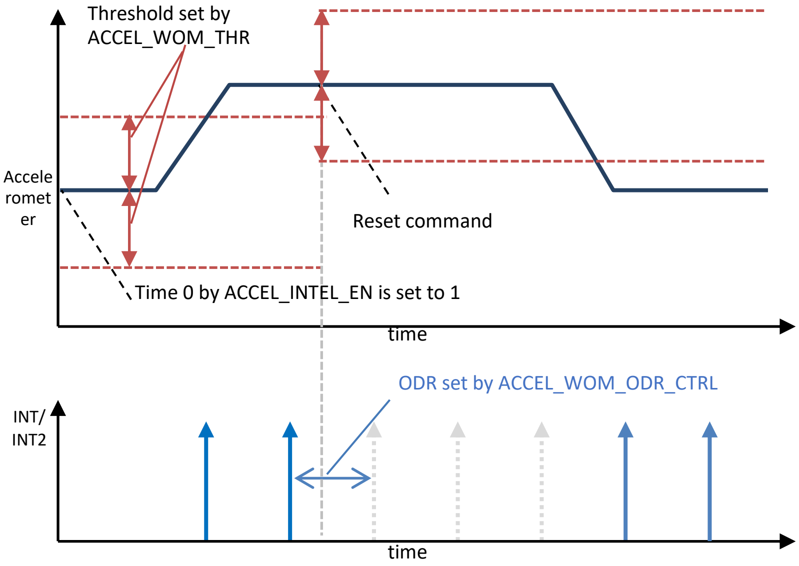

Figure 3. waveform at ACCEL_INTEL_MODE = 0

4.1.2. ACCEL_INTEL_MODE[6] = 1

Compares the current sample with the previous sample.

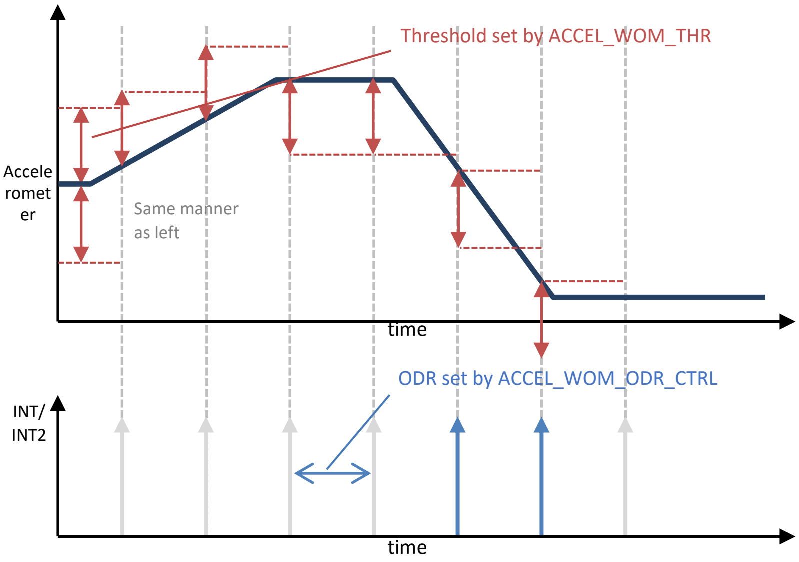

Figure 4. waveform at ACCEL_INTEL_MODE = 1

4.2. INT PIN STATUS LATCH

By setting LATCH_INT_EN = 1, the device's INT pin status can be latched to avoid passing over the signal in case of periodical INT monitoring from HOST. Then, INT pin status can be cleared by register read command, and read clear condition is programmable by INT_RD_CLEAR bit in register INT_PIN_CFG (0x37).

Key conditions at INT_PIN_CFG(0x37) in example below:
Bit 7 (INT_LEVEL) = 0 (The logic level for INT/INT2 pin is active high.)
Bit 6 (INT_OPEN) = 0 (INT/INT2 pin is configured as push-pull.)
Bit 5 (LATCH_INT_EN) = 1 (INT/INT2 pin level held until interrupt status is cleared.)

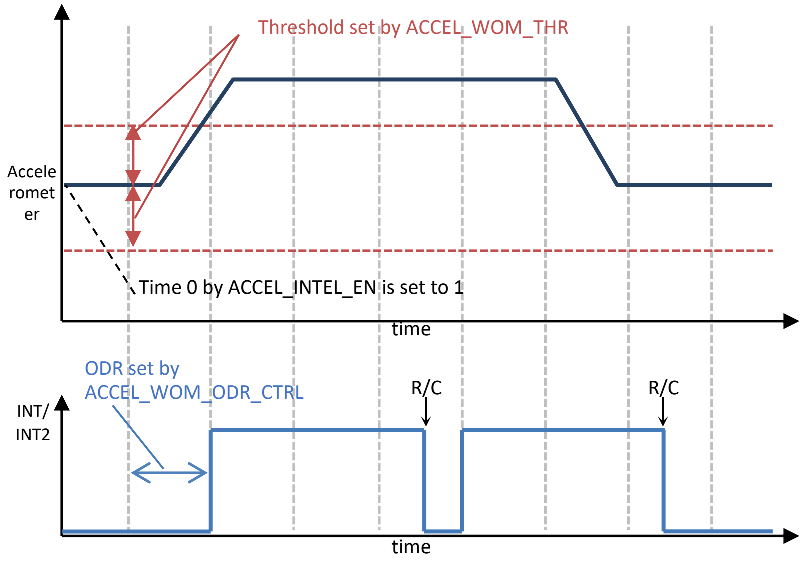
Threshold set by ACCEL_WOM_THR
Accele romet er
Time 0 by ACCEL_INTEL_EN is set to 1
time
ODR set by ACCEL_WOM_ODR_CTRL
INT/ INT2
R/C
R/C
time

Figure 5. waveform at ACCEL_INTEL_MODE = 0

(Note: R/C stands for "read clear")

5 STATUS REGISTER UPDATE

The serial interface allows detailed interrupt status information to be read from the Status register any time regardless of the INT pin status. If any interrupt event is happened, the status register is flagged immediately. The interrupt status can be read at address 0x3A (INT_STATUS). Also, the status register bit information is cleared once the INT status register (INT_STATUS) is read regardless the INT_RD_CLEAR bit condition.

If the INT_RD_CLEAR bit is set to b’1, any register read command affects INT_STATUS register to be cleared. (See details in datasheet about INT_RD_CLEAR bit. Below table is a summary of read clear.

INT_RD_CLEAR bit	0		1	
Read at	INT_STATUS	Other registers	INT_STATUS	Other registers
INT pin status	Cleared	Keep condition	Cleared	Cleared
INT_STATUS register	Cleared	Keep condition	Cleared	Cleared

In case of INT_RD_CLEAR = 1, if HOST is aware that the INT signal is generated by only WoM event from an INT_ENABLE register setting standpoint, the HOST can directly read sensor values to clear the INT pin status when the HOST receive the INT signal.

On the other hand, in case of INT_RD_CLEAR bit is set to b’0, it is required to read INT_STATUS register to clear the INT pin status. Otherwise, next INT flagged timing could be not updated due to INT pin flag is maintained.

5.1. WOM FLAG BITS DETAIL

The Wake-on-Motion status register information is updated on bit [7:5] at address 0x3A (INT_STATUS).

If the WOM_INT_EN[2:0] at address 0x38 (INT_ENABLE) is set to b’111 to enable Wake-on-Motion interrupt on accelerometer and then a Wake-on-Motion event is detected, INT pin asserts high or low depending on address 0x37 (INT_PIN_CFG) configuration. Please see datasheet for details. Once Wake-on-Motion event is happened, WOM_INT[2:0] in address 0x37 (INT_STATUS) indicates b’010 regardless to which axis detects WoM event. For example, if X & Z axes detect WoM event, then the WOM_INT[2:0] indicates b’010. See below summary table to help understanding the behavior.

Also, the status register can be flagged even if the WOM_INT_EN[2:0] bit is NOT enabled (= b’000). That means the device is capable to detect and report WoM events without INT pin signal flag.

	Flag bit		
Motion on axis:	WOM_INT[2]	WOM_INT[1]	WOM_INT[0]
X	0	1	0
Y	0	1	0
Z	0	1	0
X+Y	0	1	0
X+Z	0	1	0
Y+Z	0	1	0
X+Y+Z	0	1	0

6 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/27/2023	1.0	Initial release

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