# Bottom Port I²S Digital Output Multi-Mode Microphone

## GENERAL DESCRIPTION

The T5848 is a multi-mode, low noise digital MEMS microphone in a small package. The T5848 consists of a MEMS microphone element and an impedance converter amplifier followed by an analog-to-digital converter, decimation and antialiasing filters, power management, and an industry standard 24-bit I²S interface. The I²S interface allows the T5848 to connect directly to digital processors, such as DSPs and microcontrollers, without the need for an audio codec in the system.

The T5848 has multiple modes of operation: High Quality, Low Power (AlwaysOn), and Sleep along with new AlwaysOn modes: Acoustic Activity Detect (AAD) Analog and Digital. The T5848 has high SNR in all operational modes. It has 133 dB SPL AOP in High Quality Mode and 119 dB SPL AOP in Low Power Mode.

The T5848 is available in a standard 3.5 × 2.65 × 0.98 mm surface-mount package. It is reflow solder compatible.

## APPLICATIONS

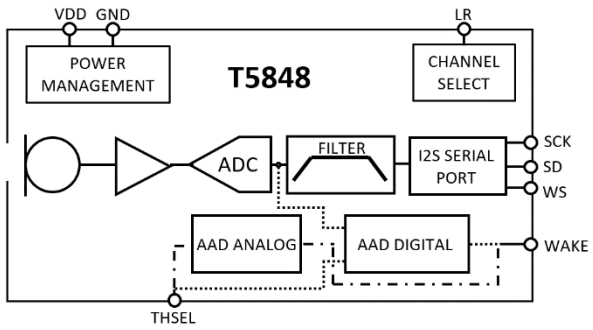
- Wearables
- Smart Televisions
- Remote Controls
- IoT Devices
- Teleconferencing Systems
- Gaming Consoles
- Security Systems

## FEATURES

| SPEC | HIGH QUALITY MODE | LOW POWER MODE |
|---|---|---|
| **Sensitivity** | −37 dB FS ±1 dB | −26 dB FS ±1 dB |
| **SNR** | 68 dBA | 64 dBA |
| **Current** | 310 µA | 120 µA |
| **AOP** | 133 dB SPL | 119 dB SPL |
| **Clock** | 2.0 MHz to 3.7 MHz | 600 kHz to 800 kHz |

- Digital I²S interface with high precision 20-bit data
- 3.5 × 2.65 × 0.98 mm surface-mount package
- Extended frequency response from 27 Hz to 18 kHz
- Sleep Mode: 9 µA
- AAD Analog Mode: 20uA
- Compatible with Sn/Pb and Pb-free solder processes
- RoHS/WEEE compliant

## FUNCTIONAL BLOCK DIAGRAM




## ORDERING INFORMATION

| PART | TEMP RANGE | PACKAGING |
|---|---|---|
| **MMICT5848-00-012** | -40°C to +85°C | 13” Tape and Reel |
| **EV_T5848-FX2** | - | Flex Evaluation Board |



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# 1. SPECIFICATIONS

## 1.1. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – GENERAL

$T_A$ = 25°C, $V_{DD}$ = 1.8 V, SCK = 2.4 MHz, $C_{LOAD}$ = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **PERFORMANCE** | | | | | | |
| Directionality | | | Omni | | | |
| Output Polarity | Input acoustic pressure vs. output data | | Non-Inverted | | | |
| Output DC Offset | Percent of Full Scale | | 3 | | % | |
| Supply Voltage ($V_{DD}$) | | 1.62 | 1.8 | 1.98 | V | |
| Sleep Mode Current ($I_S$) | SCK < 200 kHz | | 9 | | µA | |
| | SCK = OFF | | 0.8 | | µA | |

**Table 1. Acoustic/Electrical Characteristics – General**

## 1.2. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – HIGH QUALITY MODE

$T_A$ = 25°C, $V_{DD}$ = 1.8 V, SCK = 2.4 MHz, $C_{LOAD}$ = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Sensitivity | 1 kHz, 94 dB SPL | −38 | −37 | −36 | dB FS | 1 |
| Signal-to-Noise Ratio (SNR) | 20 kHz bandwidth, A-weighted | | 68 | | dBA | |
| Equivalent Input Noise (EIN) | 20 kHz bandwidth, A-weighted | | 26 | | dBA SPL | |
| Acoustic Dynamic Range | Derived from EIN and acoustic overload point | | 107 | | dB | |
| Total Harmonic Distortion (THD) | 94 dB SPL<br>105 dB SPL | | 0.05<br>0.1 | | % | |
| Low Frequency Roll Off | -3dB, relative to 1kHz Sensitivity | | 27 | | Hz | |
| Power Supply Rejection (PSR) | 20 Hz, 100 $mV_{pp}$ applied to $V_{DD}$<br>1 kHz, 100 $mV_{pp}$ applied to $V_{DD}$<br>5 kHz, 100 $mV_{pp}$ applied to $V_{DD}$<br>10 kHz, 100 $mV_{pp}$ applied to $V_{DD}$<br>20 kHz, 100 $mV_{pp}$ applied to $V_{DD}$ | | -82<br>-123<br>-109<br>-99<br>-102 | | dB FS(A) | |
| Power Supply Rejection (PSR) | 217 Hz, 100 mV p-p square wave superimposed on $V_{DD}$ = 1.8 V, A-weighted | | -109 | | dB FS (A) | |
| Power Supply Rejection—Swept Sine | 1 kHz sine wave | | -119 | | dB FS | |
| Acoustic Overload Point | 10% THD | | 133 | | dB SPL | |
| Supply Current ($I_S$) | $V_{DD}$ = 1.8 V, no load | | 310 | | µA | |

**Note 1:** Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to digital full-scale.

**Table 2. Acoustic/Electrical Characteristics – High Quality Mode**

## 1.3. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – LOW POWER MODE

$T_A$ = 25°C, $V_{DD}$ = 1.8 V, SCK = 768 kHz, 48x Decimation, 16-bit data, $C_{LOAD}$ = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Sensitivity | 1 kHz, 94 dB SPL | −27 | −26 | −25 | dB FS | 1 |
| Signal-to-Noise Ratio (SNR) | 8 kHz bandwidth, A-weighted | | 64 | | dBA | |
| Equivalent Input Noise (EIN) | 8 kHz bandwidth, A-weighted | | 30 | | dBA SPL | |
| Acoustic Dynamic Range | Derived from EIN and acoustic overload point | | 89 | | dB | |
| Total Harmonic Distortion (THD) | 94 dB SPL<br>105 dB SPL | | 0.05<br>0.1 | | % | |
| Power Supply Rejection (PSR) | 217 Hz, 100 mV p-p square wave superimposed on $V_{DD}$ = 1.8 V, A-weighted | | −91 | | dB FS | |
| Power Supply Rejection—Swept Sine | 1 kHz sine wave | | −102 | | dB FS | |
| Acoustic Overload Point | 10% THD | | 119 | | dB SPL | |
| Supply Current ($I_S$) | $V_{DD}$ = 1.8 V, no load | | 120 | | µA | |

**Note 1:** Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to digital full-scale.

**Table 3. Acoustic/Electrical Characteristics – Low Power Mode**

## 1.4. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – AAD MODES

$T_A$ = 25°C, VDD = 1.8 V, SCK = OFF, $C_{LOAD}$ = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **AAD ANALOG PARAMETERS** | | | | | | |
| Min AAD Analog Threshold | 1kHz Level, AAD A_TH [3:0] = 0x0; | | 60 | | dB SPL | |
| Max AAD Analog Threshold | 1kHz Level, AAD A_TH [3:0] = 0xF; | | 97.5 | | dB SPL | |
| AAD A Supply Current ($I_S$) | CLK OFF | | 20 | | µA | |
| **AAD DIGITAL PARAMETERS** | | | | | | |
| Min AAD Digital Absolute Threshold | 230Hz Level, AADD_TH [12:0] = 0x00F; | | 40 | | dB SPL | |
| Max AAD Digital Absolute Threshold | 230Hz Level, AADD_TH [12:0] = 0x7BC; | | 87 | | dB SPL | |
| AAD D1 Supply Current ($I_S$) | CLK = 768kHz | | 137 | | µA | |
| AAD D2 Supply Current ($I_S$) | CLK OFF | | 110 | | µA | |

**Table 4. Acoustic/Electrical Characteristics – AAD Modes**

## 1.5. DIGITAL FILTER CHARACTERISTICS

$T_A$ = 25°C, VDD = 1.8 V unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Group Delay | Acoustic input to digital output – includes filter and $I^2S$ serial output | | $2/f_S$ | | sec. | |
| Pass Band Ripple | | | | ±0.3 | dB | |
| Stop Band Attenuation | | | 60 | | dB | |
| Pass Band | Fs = 48 kHz | | 15 | | kHz | |

**Table 5. Digital Input/Output Characteristics**



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## 1.6. DIGITAL INPUT/OUTPUT CHARACTERISTICS

$T_A$ = 25°C, VDD = 1.8 V unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Voltage High ($V_{IH}$) | | 0.65 × $V_{DD}$ | | | V | |
| Input Voltage Low ($V_{IL}$) | | | | 0.35 × $V_{DD}$ | V | |
| Output Voltage High ($V_{OH}$) | $I_{LOAD}$ = 0.5 mA | 0.7 × $V_{DD}$ | $V_{DD}$ | | V | |
| Output Voltage Low ($V_{OL}$) | $I_{LOAD}$ = 0.5 mA | | 0 | 0.3 × $V_{DD}$ | V | |

**Table 6. Digital Input/Output Characteristics**

## 1.7. I²S DIGITAL INPUT/OUTPUT

$T_A$ = 25°C, VDD = 1.8 V, unless otherwise noted. Typical specifications are not guaranteed.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **MODE SWITCHING** | | | | | | |
| Sleep Time | Time from $f_{CLK}$ falling <200 kHz | | 1 | | ms | |
| Wake-Up Time | High Quality mode, Sleep Mode to $f_{CLK}$ >2 MHz, output within 0.5 dB of final sensitivity, power on | | 6 | | ms | |
| Wake-Up Time | Low Power Mode, Sleep Mode to $f_{CLK}$ >400 kHz, output within 0.5 dB of final sensitivity, power on | | 6 | | ms | |
| Switching time | Between Low Power and High Quality Mode | | 3.5 | | ms | |
| **INPUT** | | | | | | |
| $t_{SCP}$ | Input clock period | 270 | | 1667 | ns | |
| Clock Frequency (CLK) | AAD Write Operation | 50 | | | kHz | |
| | Sleep Mode | | | 200 | kHz | |
| | Low Power Mode | 600 | | 800 | kHz | |
| | High Quality Mode | 2.0 | | 3.7 | MHz | |
| Clock Duty Cycle | $f_{CLK}$ <3.7 MHz | 45 | | 55 | % | |
| $t_{RISE}$ | CLK rise time (10% to 90% level) | | | 25 | ns | 1 |
| $t_{FALL}$ | CLK fall time (90% to 10% level) | | | 25 | ns | 1 |
| $t_{SCH}$ | SCK high | 50 | | | ns | 1 |
| $t_{SCL}$ | SCK low | 50 | | | ns | 1 |
| $t_{WSS}$ | WS setup | 50 | | | ns | 1 |
| $t_{WSH}$ | WS hold | 50 | | | ns | 1 |
| **OUTPUT** | | | | | | |
| $t_{SDV}$ | Serial Data Valid, From SCK falling to valid SD data | | | 75 | ns | 1 |
| $t_{SDD}$ | Serial Data Disable, From SCK falling to SD output tristated | | | 76 | ns | 1 |

**Note 1:** Guaranteed by design

**Table 7. I²S Digital Input/Output**

## 1.8. TIMING DIAGRAM

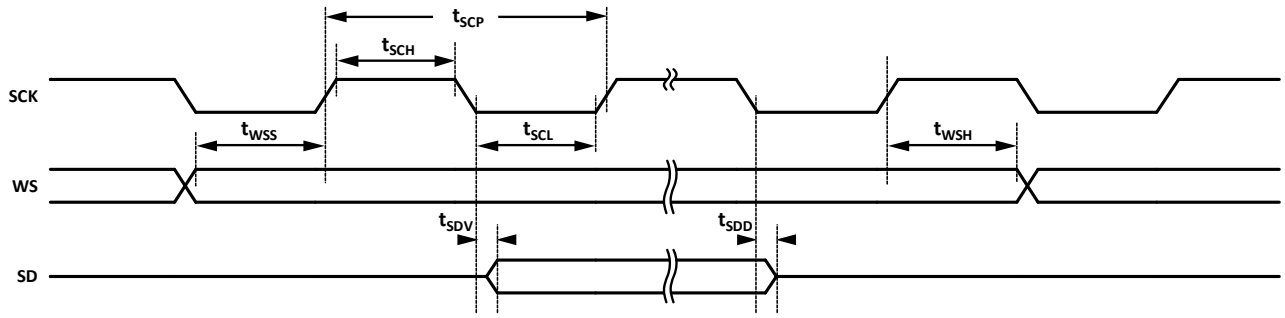


**Figure 1. I²S Output Timing**



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# 2. ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

## 2.1. ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.3 V to +1.98 V |
| Digital Pin Input Voltage | −0.3 V to $V_{DD}$ + 0.3 V or 1.98 V, whichever is less |
| Mechanical Shock | 10,000 *g* |
| Vibration | Per MIL-STD-883 Method 2007, Test Condition B |
| **Temperature Range** | |
| Operating | −40°C to +85°C |
| Storage | −55°C to +150°C |

**Table 8. Absolute Maximum Ratings**

## 2.2. ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## 2.3. SOLDERING PROFILE

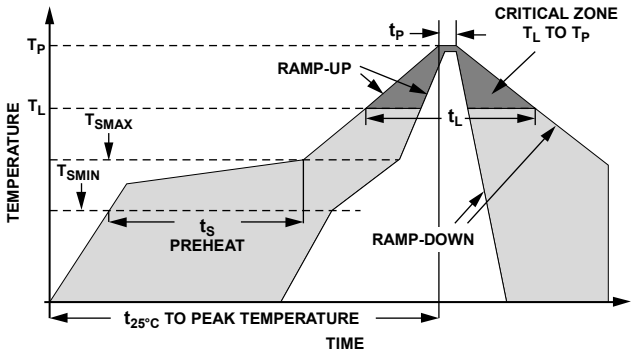


**Figure 2. Recommended Soldering Profile Limits**

## 2.4. RECOMMENDED SOLDERING PROFILE*

| PROFILE FEATURE | | Sn63/Pb37 | Pb-Free |
|---|---|---|---|
| Average Ramp Rate ($T_L$ to $T_P$) | | 1.25°C/sec max | 1.25°C/sec max |
| Preheat | Minimum Temperature ($T_{SMIN}$) | 100°C | 100°C |
| | Maximum Temperature ($T_{SMAX}$) | 150°C | 200°C |
| | Time ($T_{SMIN}$ to $T_{SMAX}$), $t_S$ | 60 sec to 75 sec | 60 sec to 75 sec |
| Ramp-Up Rate ($T_{SMAX}$ to $T_L$) | | 1.25°C/sec | 1.25°C/sec |
| Time Maintained Above Liquidous ($t_L$) | | 45 sec to 75 sec | ~50 sec |
| Liquidous Temperature ($T_L$) | | 183°C | 217°C |
| Peak Temperature ($T_P$) | | 215°C +3°C/−3°C | 260°C +0°C/−5°C |
| Time Within +5°C of Actual Peak Temperature ($t_P$) | | 20 sec to 30 sec | 20 sec to 30 sec |
| Ramp-Down Rate | | 3°C/sec max | 3°C/sec max |
| Time +25°C ($t_{25°C}$) to Peak Temperature | | 5 min max | 5 min max |

**The reflow profile in Table 9 is recommended for board manufacturing with TDK MEMS microphones. All microphones are also compatible with the J-STD-020 profile*

**Note**: After 3 reflows, microphone sensitivity may deviate by up to 2 dB.

**Table 9. Recommended Soldering Profile**



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# 3. PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

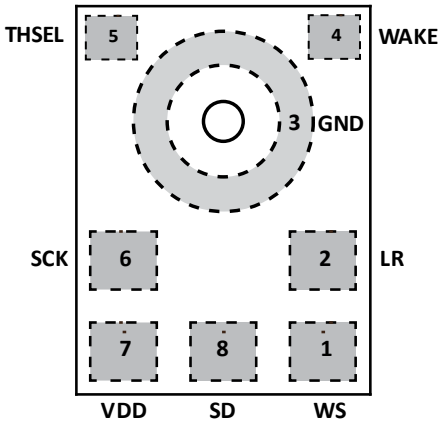


**Figure 3. Pin Configuration (Top View, Terminal Side Down)**

## 3.1. PIN FUNCTION DESCRIPTIONS

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | WS | Serial Data Word Select for $I^2S$ Interface |
| 2 | LR | Left Channel or Right Channel Select:<br>Left: LR tied to GND<br>Right: LR tied to VDD. In this setting, LR should be tied to the same voltage source as the VDD pin. |
| 3 | GND | Ground |
| 4 | WAKE | Wake Output Pin. Interrupt pin for Acoustic Activity Detect (AAD) Modes. Outputs HIGH state to indicate the acoustic stimulus exceeds AAD conditions, returns LOW when the stimulus no longer exceeds them.<br>For operation without AAD modes, this pin can be tied to Gnd or left as No Connect. |
| 5 | THSEL | Threshold Select Input Pin. Used to both enable and configure AAD Modes.<br>No connection for operation without AAD modes. |
| 6 | SCK | Clock Input to Microphone |
| 7 | VDD | Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 7 (VDD) and ground. Place the capacitor as close to Pin 7 as possible. |
| 8 | SD | Serial Data Output for $I^2S$ Interface. This pin tristates when not actively driving the appropriate output channel. The SD trace should have a 100 kΩ pull-down resistor to discharge the line during the time that all the microphones on the bus have tristated their outputs. |

**Table 10. Pin Function Descriptions**

## 4. TYPICAL PERFORMANCE CHARACTERISTICS

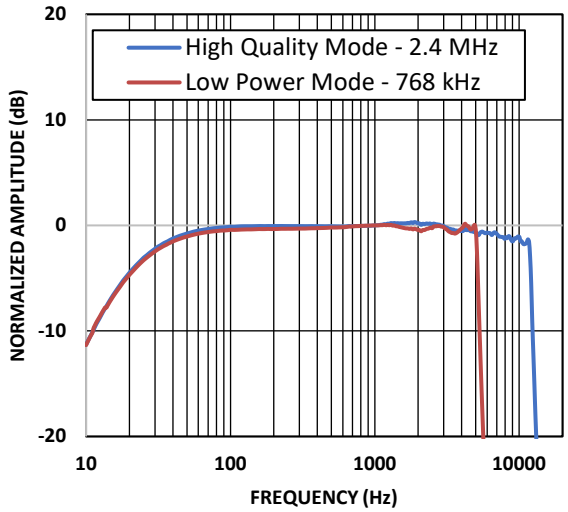


Figure 4. Typical Audio Frequency Response

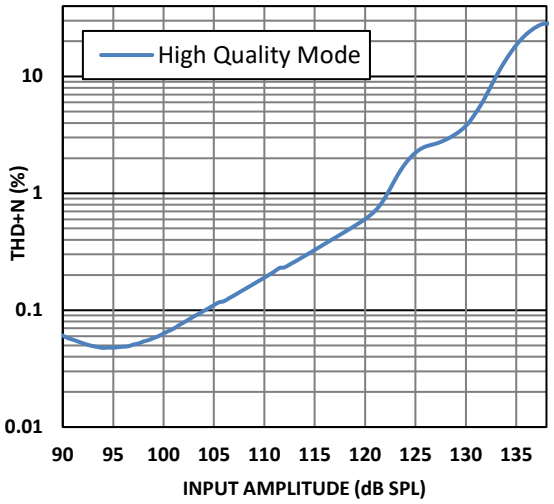


Figure 5. THD + N High Quality Mode – 1 kHz Input

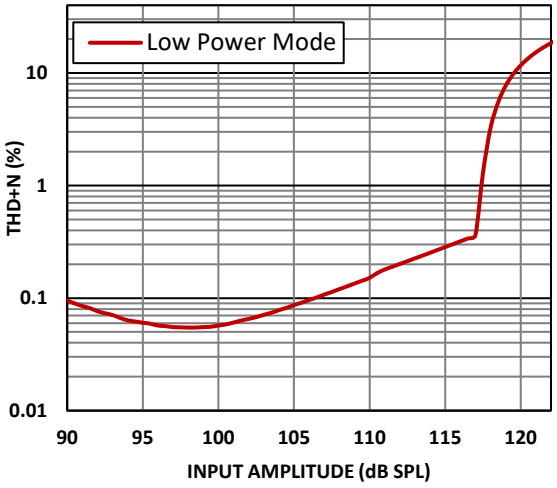


Figure 6. THD + N Low Power Mode – 1 kHz Input

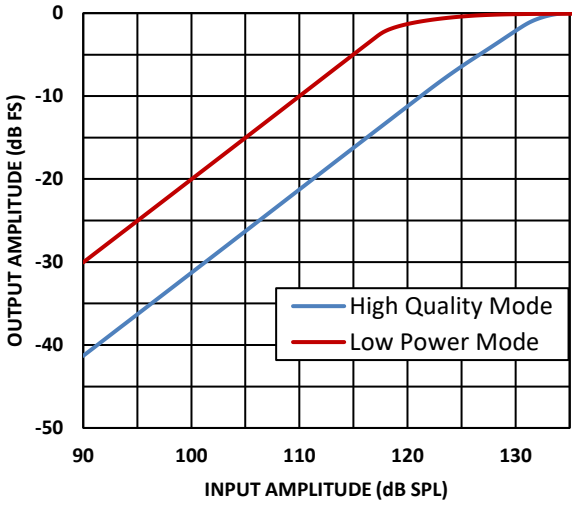


Figure 7. Linearity



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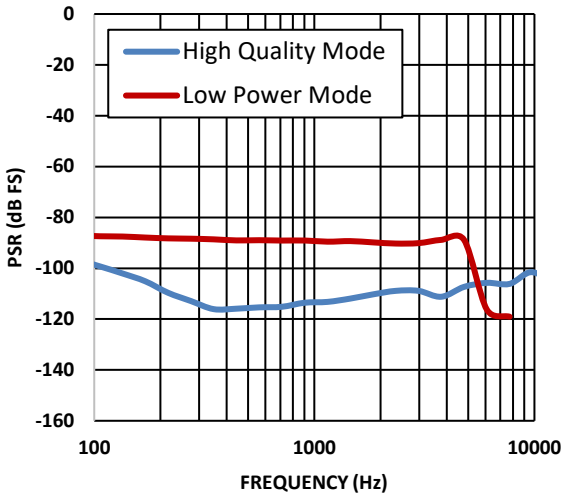


Figure 8. Power Supply Rejection (PSR) vs. Frequency

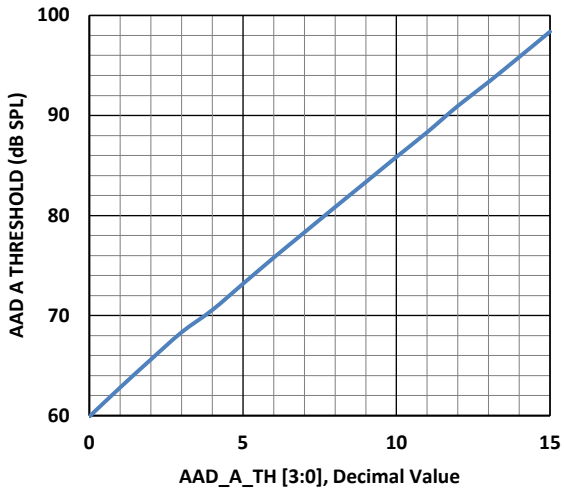


Figure 9. AAD Analog Threshold vs Register Value

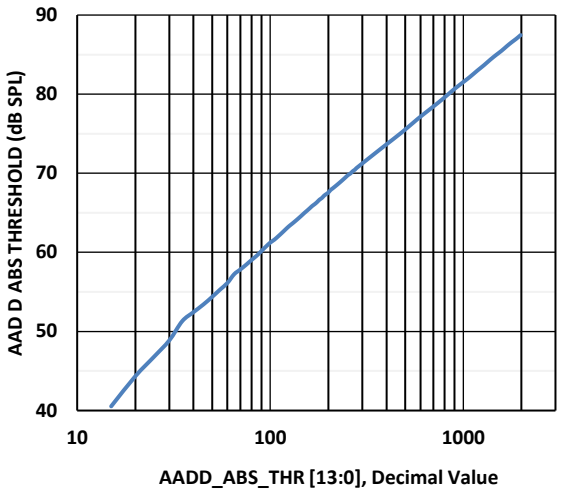


Figure 10. AAD Digital 1,2 Absolute Threshold vs Register Value

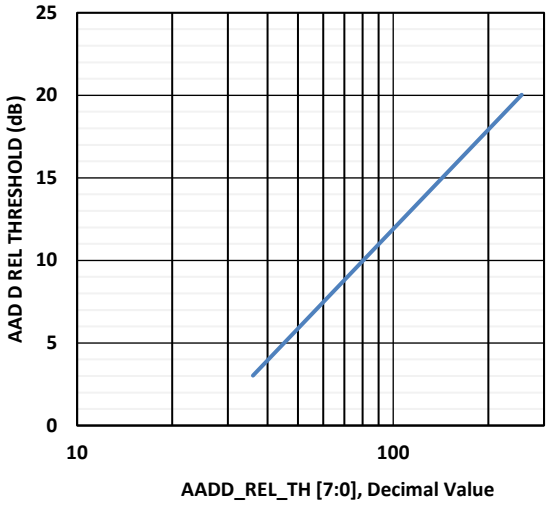


Figure 11. AAD Digital 1,2 Relative Threshold vs Register Value



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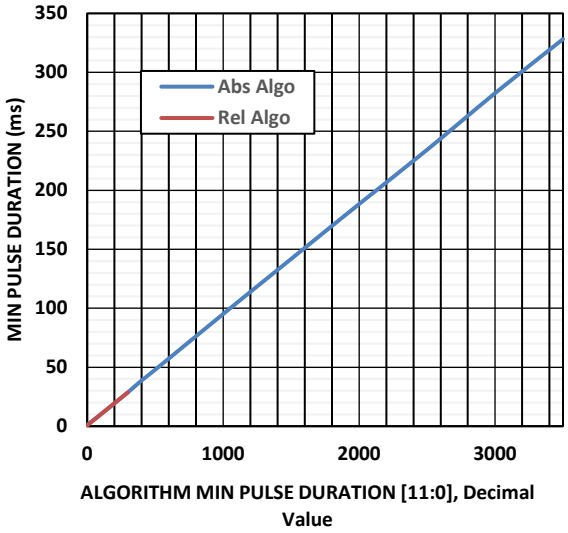


**Figure 12. AAD Digital Min Pulse Duration vs Register Value**



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# 5. MODES OF OPERATION

## 5.1. EXISTING MICROPHONE MODES

Commonly used digital MEMS microphone operating modes are offered on T5848: Sleep, Low Power, and High Quality Mode. They are selected via the CLK frequency.

## 5.2. ACOUSTIC ACTIVITY DECTECT MICROPHONE MODES

T5848 introduces Acoustic Activity Detect (AAD) Modes which are parallel processing features which operate within Sleep and Low Power Modes. The on-chip processing of these AAD Modes determine if acoustic activity has occurred or not. There are three different types: AAD Analog, AAD Digital 1 and AAD Digital 2 as outlined in the table below. The activation and configuration for all AAD Modes is carried out via a one wire write on the THSEL pin. When the activity detect conditions are met, the WAKE pin is set HIGH, when the conditions are no longer met the WAKE pin automatically returns LOW (without any type of reset required from the SoC/master).

### 5.2.1. AAD MODES AND DESCRIPTION

| MICROPHONE POWER MODE (IN PARALLEL) | ACOUSTIC ACTIVITY DETECT (AAD) MODE NAME | DESCRIPTION | CONFIGURABLE OPTIONS |
|---|---|---|---|
| Sleep Mode | AAD Analog (AAD A) | Analog activity detect, lowest power | Absolute Threshold (60-97.5dB SPL), LPF (1.1kHz-4.4kHz) |
| Low Power Mode | AAD Digital 1 (AAD D1) | Digital activity detect with $I^2S$ bitstream | Absolute Threshold (40-87dB SPL), Relative Threshold (3dB-20dB), Pulse Duration |
| Sleep Mode | AAD Digital 2 (AAD D2) | Digital activity detect without $I^2S$ bitstream | Absolute Threshold (40-87dB SPL), Relative Threshold (3dB-20dB), Pulse Duration |

**Table 11. AAD Modes and Description**

Figure 13 shows the required sequence for transitioning between modes of operation. In order to ensure proper functionality when the system transitions from either Low Power Mode or High Quality Mode, it must pass through an interim Sleep Mode before entering Sleep Mode with AAD active. To enter this intermediate state the clock frequency must be changed to be between the range of 50 kHz and 200 kHz for a minimum of 2 ms. This allows time for the system to correctly power-down blocks before it moves to Sleep Mode with AAD Active.

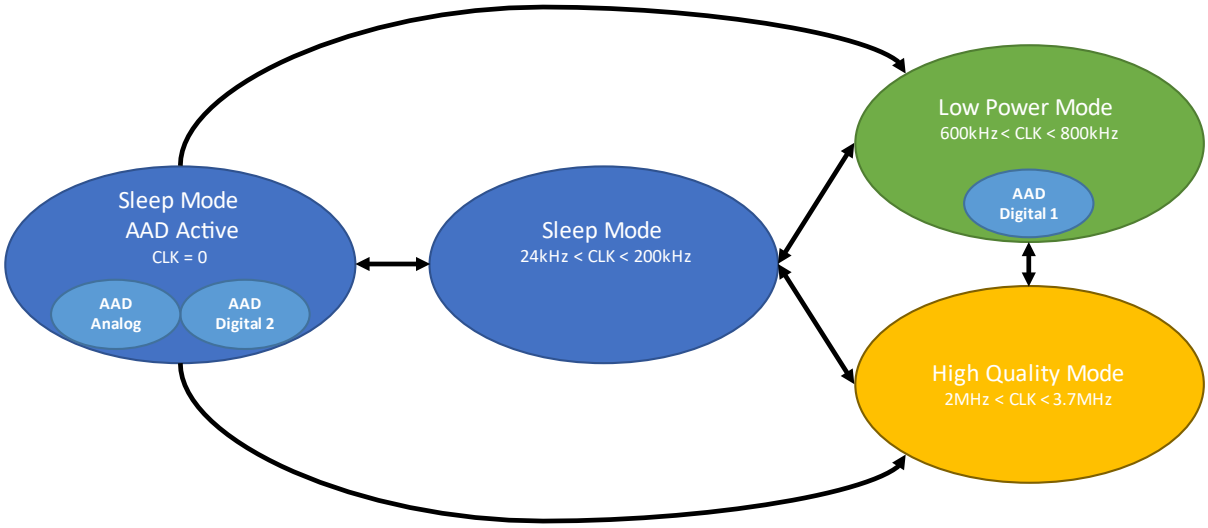


**Figure 13. T5848 Mode Transitions**



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### 5.2.2. ACOUSTIC ACTIVITY DETECT ANALOG

AAD Analog takes the signal from the MEMS after the pre-amp and compares it to the preselected conditions, Absolute Threshold and Low Pass Filter Frequency. If the signal is above the Absolute Threshold and is below the LPF cutoff, the WAKE Pin will be set high. The WAKE pin will continue to remain high while these conditions are met and will return low when the signal level returns below this level. AAD_A_EN bit needs to be set and CLK needs to be OFF for AAD Analog (AAD A) to operate. The microphone consumes only 20uA in this mode.

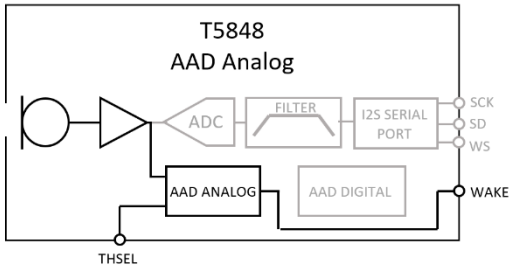


**Figure 14. Block Diagram for AAD Analog Operation**

### 5.2.3. ACOUSTIC ACTIVITY DETECT DIGITAL 1

AAD Digital 1 is an add on to Low Power Mode where the digital bitstream is analyzed by the AAD Digital logic to see if it meets the preselected conditions Absolute Threshold, Relative Threshold and Pulse Duration. If the conditions are met the WAKE Pin will be set high. The WAKE pin will remain high while these conditions are met and will return low when the signal level returns below this level. The I²S bitstream is running throughout, which allows the Application Processor to buffer the bitstream and carry out 2nd stage verification or further analysis of the signal which triggered the AAD Digital 1 (AAD D1) event.

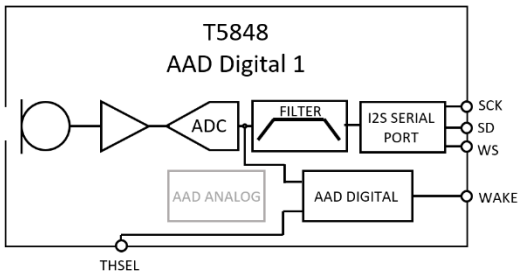


**Figure 15. Block Diagram for AAD Digital 1 Operation**

### 5.2.4. ACOUSTIC ACTIVITY DETECT DIGITAL 2

AAD Digital 2, like AAD D1 analyzes the digital bitstream to check for activity meeting the preselected conditions (same configurable options as AAD D1). However, AAD D2 does not require an external CLK (by using an internal CLK) allowing power savings at the microphone and at the system level but does not facilitate the I²S bitstream like AAD D1. Like the other AAD modes the WAKE pin is set high when the AAD D2 conditions are met and returns low when the conditions are no longer met.



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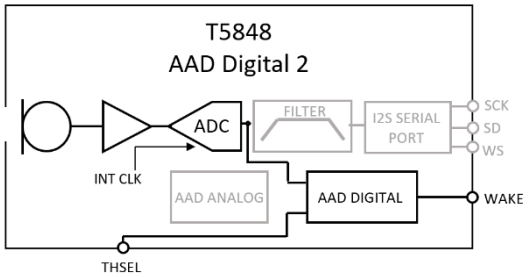


**Figure 16. Block Diagram for AAD Digital 2 Operation**

### 5.2.5. MODE SELECTION AND MODE CHANGES BEFORE AAD ACTIVATION

AAD A or AAD D1/2 can be configured and enabled while the microphone is in any of its modes (sleep mode one wire writes require CLK active for communication to function i.e. 50kHz<CLK<200kHz). After configuration and enabling, AAD will go active (represented by activity on the WAKE pin) when the microphone enters its corresponding mode (decided by the CLK frequency). AAD A and AAD D2 are run when the device is in Sleep mode (CLK=OFF), AAD D1 is run when the device is in Low Power mode (CLK=768kHz).

### 5.2.6. AAD STATUS AND DISABLE

After an AAD mode has been enabled it will remain enabled as long as power is maintained to the microphone or until it has been specifically disabled by setting the AADx_EN bit to 0.

## 5.3. ACOUSTIC ACTIVITY DETECT CONFIGURATION PROTOCOL

A serial one wire protocol on the THSEL pin controls all the Acoustic Activity Detect modes, AAD A, AAD D1 and AAD D2. The protocol requires the standard $I^2S$ CLK to be running at a speed >50kHz and the THSEL pin is modulated proportional to the CLK cycles to create the following symbols for logic zeros or ones which in turn form the device address, register address and data of the command. There are also unique symbols for start/pilot and stop to terminate each write. The start/pilot pulse width is important as it defines the pulse width of the *Zero*, *One*, *Space* and *Stop* symbols. The *Zero* and *One* symbols are a form of encoding to represent bit values of 0 and 1 values respectively. See below for details.

### 5.3.1. ONE WIRE SERIAL PROTOCOL SYMBOLS

| SYMBOL NAME | DESCRIPTION | THSEL CONDITION | SYMBOL PULSE WIDTH | | |
|---|---|---|---|---|---|
| | | | MIN | TYPICAL | MAX |
| Start/Pilot | Start symbol which also defines the PILOT width $T_P$ | HIGH | 8 CLK cycles | 10 CLK cycles | 20 CLK cycles |
| Zero | Symbol for bit value = 0 | HIGH | | 1 x $T_P$ | 1.5 x $T_P$ |
| One | Symbol for bit value = 1 | HIGH | 2 x $T_P$ | 3 x $T_P$ | 3.5 x $T_P$ |
| Stop | Stop symbol | HIGH | 128 x CLK | | |
| Space | Separate individual symbols above | LOW | 1 x $T_P$ | 1 x $T_P$ | 2 x $T_P$ |

*Although operation is guaranteed within the min max ranges it is recommended to use the typical values shown in the table above

**Table 12. One Wire Serial Protocol Symbols**



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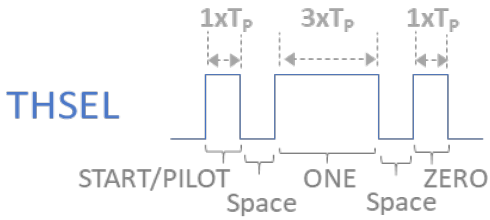



**Figure 17. Example write on THSEL followed by a single bit Zero and One relative to the PILOT**

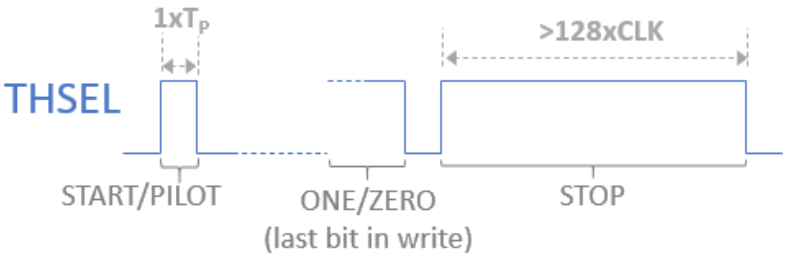
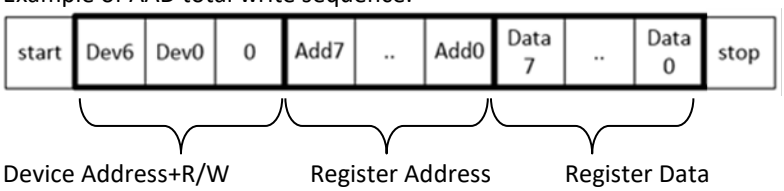



**Figure 18. Write termination with Stop**

The total write sequence consists of START/PILOT + 24 bits of payload + STOP. The payload consists of three 8 bit fields:

- Device Address + RW = 7'b1010011 (Constant for this device) + 1'b0 (0 = write, constant for this device)
- Register Address = 8-bit value, determined by AAD function lookup table
- Data = 8-bit value, determined by AAD function lookup table

Example of AAD total write sequence:




Example Write:
Device Addr+R/W = 10100110 (Constant for this device)
Register Address = 00000001 (Example Reg Addr only, not an option)
Register Data = 00000010 (Example data)
CLK = 100kHz
$T_{CLK}$ = 10us
The write calculations based on 100kHz CLK, 10 CLK cycle PILOT are shown below:



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### 5.3.2. EXAMPLE ONE WIRE WRITE

| SYMBOL NAME | DESCRIPTION | THSEL CONDITION | CALCULATION | WIDTH |
|---|---|---|---|---|
| Start/Pilot | Start/Pilot which indicates start of write and defines logic pulse widths | HIGH | 10 X $T_{CLK}$ | 100us = $T_P$ |
| Zero | Single bit Zero | HIGH | 1 x $T_P$ | 100us |
| One | Single bit One | HIGH | 3 x $T_P$ | 300us |
| Stop | Stop Signal | HIGH | >128 x CLK period | >1280us |
| Space | Separate individual symbols above | LOW | 1 x $T_P$ | 100us |

**Table 13. Example One Wire Write**

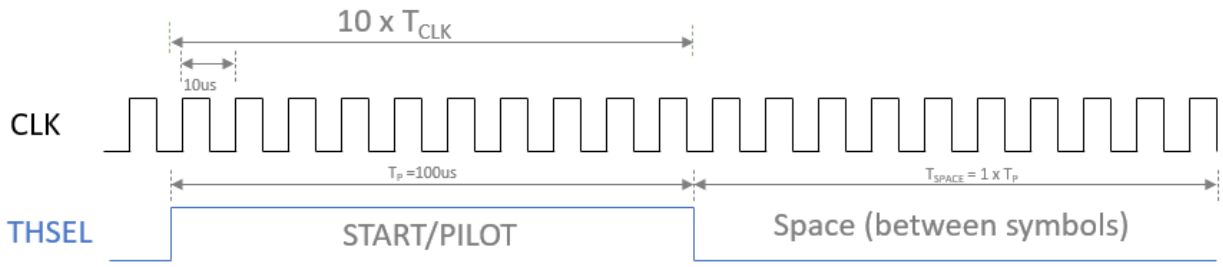
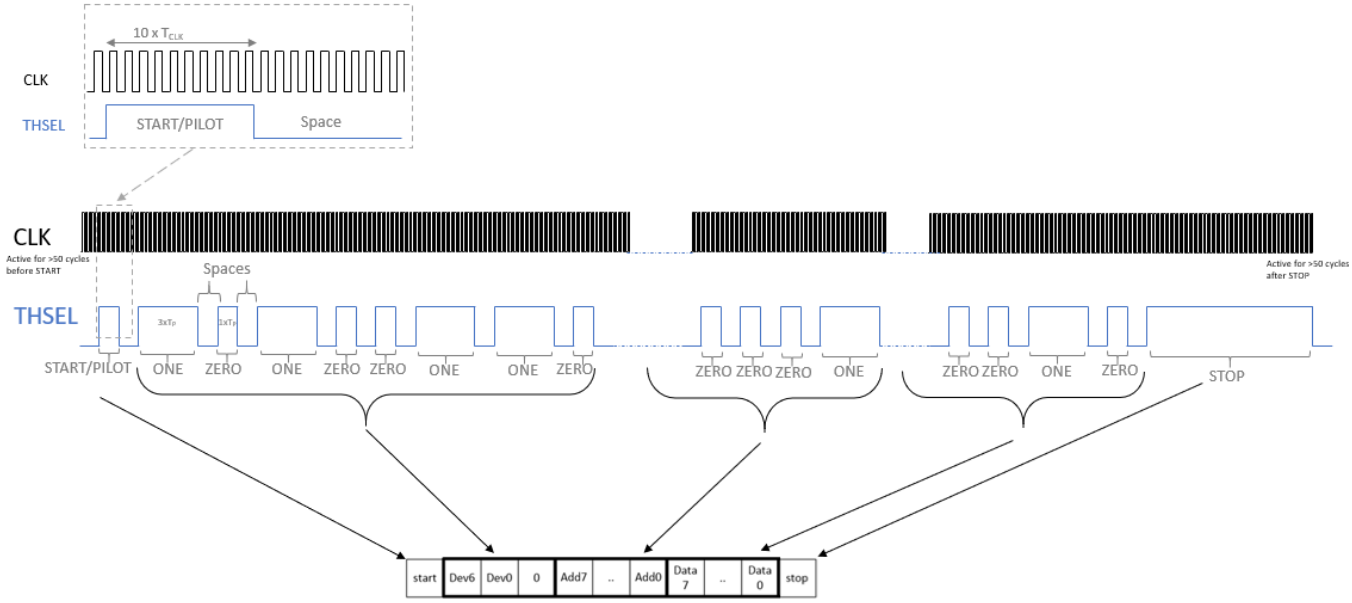



**Figure 19. Timing diagram for example above showing relationship between THSEL pilot and CLK**




START + 10100110 + 00000001 + 00000010 + STOP

**Figure 20. Expanded Timing diagram example showing start, 3 x 8 bit values and stop being written to the device, with the low level translation of each bit to their respective symbols.**



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## 5.4. AAD ENABLE SEQUENCE

Using the write sequence above, the Acoustic Activity Detect (for all 3 modes) is enabled using the following five writes in this sequence:

### 5.4.1. AAD ENABLE SEQUENCE WRITES

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 1 | 0x5C | 0x00 |
| 2 | 0x3E | 0x00 |
| 3 | 0x6F | 0x00 |
| 4 | 0x3B | 0x00 |
| 5 | 0x4C | 0x00 |

**Table 14. AAD Enable Sequence Writes**

For example, sequence write #1 from above with Address 0x5C (b01011100) and Data 0x00 (b00000000) would be:

**START + 10100110 + 01011100 + 00000000 + STOP**

After this sequence has been completed any of the configuration settings for the AAD Analog or AAD Digital modes can be adjusted. The enable sequence can be written once to the microphone and will remain valid as long as power is maintained to the microphone. If the mic goes through a power cycle, then the sequence will have to be repeated.

## 5.5. ACOUSTIC ACTIVITY DETECT ANALOG (AAD A) OPERATION AND CONFIGURATION

Acoustic Activity Detect Analog (AAD A) compares the analog signal from the MEMS with the defined conditions configured by the user - threshold level and Low Pass Frequency cutoff. If the acoustic signal meets the conditions set (above the threshold and below the LPF cutoff) then the WAKE pin (pin4) will be set high and will stay high while the acoustic stimulus continues to meet those conditions. When the acoustic stimulus no longer meets the conditions the WAKE pin will automatically return to a LOW state. See Figure 21. The microphone consumes only 20μA when in AAD A mode.

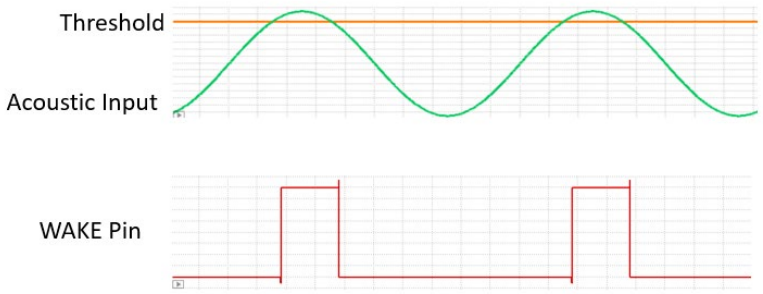


**Figure 21. AAD A Threshold level and WAKE pin activation**



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### 5.5.1. AAD A REGISTERS

| REG NAME | REG ADDR [BIT] | FUNCTION |
|---|---|---|
| AAD A_LPF[2:0] | Reg 0x35[2:0] | 3-bits to define the Low Pass Filter corner over a range of 1.2kHz to 4.4 kHz |
| AAD A_TH[3:0] | Reg 0x36[3:0] | 4-bits to define the Trigger Threshold. 16 levels available from 60 dB SPL to 97.5 dB SPL. |
| AAD A_EN[1] | Reg 0x29[3] | Analog Acoustic Activity Detect (AAD A) Enable. 0 = Disabled, 1 = Enabled. Default = 0 |

**Table 15. AAD A Registers**

On AAD A enabling, the microphone will acknowledge by pulsing the WAKE pin HIGH for about 12 us.

### 5.5.2. AAD A LPF VALUES

All levels, frequencies, and timing values in the AAD A and AAD D configuration sections are typical.

| AAD A_LPF (HEX) | FREQUENCY (kHz) |
|---|---|
| 0x1 | 4.4 |
| 0x2 | 2.0 |
| 0x3 | 1.9 |
| 0x4 | 1.8 |
| 0x5 | 1.6 |
| 0x6 | 1.3 |
| 0x7 | 1.1 |

**Table 16. AAD A LPF Values**

### 5.5.3. AAD A TH VALUES

| AAD A_TH [3:0] (HEX) | AAD A_TH (DEC) | THRESHOLD (dB SPL) |
|---|---|---|
| 0x0 | 0 | 60 |
| 0x1 | 1 | 62.5 |
| 0x2 | 2 | 65 |
| 0x3 | 3 | 67.5 |
| 0x4 | 4 | 70 |
| 0x5 | 5 | 72.5 |
| 0x6 | 6 | 75 |
| 0x7 | 7 | 77.5 |
| 0x8 | 8 | 80 |
| 0x9 | 9 | 82.5 |
| 0xA | 10 | 85 |
| 0xB | 11 | 87.5 |
| 0xC | 12 | 90 |
| 0xD | 13 | 92.5 |
| 0xE | 14 | 95 |
| 0xF | 15 | 97.5 |

**Table 17. AAD A TH Values**

### 5.5.4. AAD A EXAMPLE CONFIGURATION AND ACTIVATION SEQUENCE

AAD Analog can be activated with the following sequence of powerup conditions and register writes:

1. Apply Vdd, apply CLK > 50 kHz
2. Apply AAD Unlock write sequence:

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 1 | 0x5C | 0x00 |
| 2 | 0x3E | 0x00 |
| 3 | 0x6F | 0x00 |
| 4 | 0x3B | 0x00 |
| 5 | 0x4C | 0x00 |

3. Configure AAD A settings, AAD A_LPF = 0x1 (4.4kHz), AAD A_TH = 0x4 (70 dB SPL)

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 6 | 0x35 | 0x01 |
| 7 | 0x36 | 0x04 |

4. Enable AAD A

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 8 | 0x29 | 0x08 |

   The microphone will acknowledge the enable by pulsing the WAKE pin HIGH for about 12 us.

5. Activate AAD A by setting CLK to a frequency between 50 kHz and 200 kHz for 2 ms followed by setting CLK = OFF. The microphone will now set the WAKE pin HIGH in response to acoustic stimulus above 70 dB SPL and less than 4.4 kHz.

### 5.5.5. AAD A REGISTER MAP

| AAD Analog (AAD A) Register Map | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| **29h** | Reserved | | | | AAD A_EN | Reserved | AAD D2_EN | AAD D1_EN |
| **2Ah** | Reserved | | | Unused for AAD A | | | | |
| **2Bh** | Unused for AAD A | | | | | | | |
| **2Ch** | Unused for AAD A | | | | | | | |
| **2Dh** | Unused for AAD A | | | | | | | |
| **2Eh** | Unused for AAD A | | | | | | | |
| **2Fh** | Unused for AAD A | | | | | | | |
| **30h** | Unused for AAD A | | | | | | | |
| **31h** | Unused for AAD A | | | | | | | |
| **32h** | Unused for AAD A | | | | | | | |
| **33h** | Unused for AAD A | | | | | | | |
| **35h** | Reserved | | | | | AAD A_LPF[2:0] | | |
| **36h** | Reserved | | | | AAD A_TH[3:0] | | | |

**Table 18. AAD A Register Map**



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## 5.6. ACOUSTIC ACTIVITY DETECT DIGITAL (AAD D) OPERATION AND CONFIGURATION

AAD Digital provides a more advanced method of activity detection compared to AAD Analog. It has two modes of operation - AAD D1 and AAD D2, where D1 requires an external CLK and provides a I²S bitstream output, and D2 where no external CLK is required, but no I²S bitstream is produced. The activity detection capability operates in the same way for AAD D1 or AAD D2 so the following settings apply to both modes. Their configuration is still applied via one wire writes on the THSEL pin and the output is shown as activity on the WAKE pin.

### 5.6.1. AAD D VOICE BAND FILTER

To better target voice activity, the AAD Digital path includes a bandpass filter with a fixed bandwidth. The low- and high-frequency corners of this filter are tune to approximately 100 Hz and 500 Hz, respectively. This filter attenuates low-frequency, such as AC mains, and high-frequency noise to focus detection in on typical fundamental frequencies of speech.

### 5.6.2. AAD D REGISTERS

Both AAD D1 and AAD D2 share registers which are defined as shown in Table 19:

| REGISTER NAME | REG ADDR [BIT] | FUNCTION |
|---|---|---|
| **AADD_EN[1:0]** | Reg 0x29[1:0] | Digital Acoustic Activity Detect (AADD).<br>0x1 = AAD D1 Enable, 0x2 = AAD D2 Enable.<br>Default = 0x0 (AAD D1, D2 both disabled). |
| **AADD_ALGO_SEL[1:0]** | Reg0x2D[7:6] | Selects AAD Digital threshold algorithm.<br>0x0 = No Thresholds Enabled, 0x1 = Relative Enabled, 0x2 = Absolute Enabled.<br>Default = 0x3 (Absolute and Relative Enabled). |
| **AADD_FLOOR[12:0]** | Reg0x2A[4:0]<br>Reg0x2B[7:0] | 13-bits used to set the Relative Threshold for both AAD D1 and AAD D2 modes. The allowable range for these bits is 0x0F – 0x7BC. |
| **AADD_REL_PULSE_MIN[11:0]** | Reg0x2F[3:0]<br>Reg0x2E[7:0] | 12-bits used to set the minimum duration the acoustic signal must exceed before the Relative Threshold detection mode is activated. The allowable range for these bits is 0x000 to 0x12C |
| **AADD_ABS_PULSE_MIN[11:0]** | Reg0x2F[7:4]<br>Reg0x30[7:0] | 12-bits used to set the minimum duration the acoustic signal must exceed before the Absolute Threshold detection mode is activated. The allowable range for these bits is 0x000 to 0xDAC |
| **AADD_ABS_TH[12:0]** | Reg0x32[4:0]<br>Reg0x31[7:0] | 13-bits used to set the Absolute Threshold detection level. The allowable range for these bits is 0x0F – 0x7BC. |
| **AADD_REL_TH[7:0]** | Reg0x33[7:0] | Configures the gain for the AADD modes. See text for details. Gain range is limited to 3dB to 20dB or 0x24 to 0xFF |

**Table 19. AADD Registers**

On AAD D enabling, the microphone will acknowledge by pulsing the WAKE pin HIGH for about 12 us.

The functionality of the AADD mode registers is shown diagrammatically in Figure 22 below.



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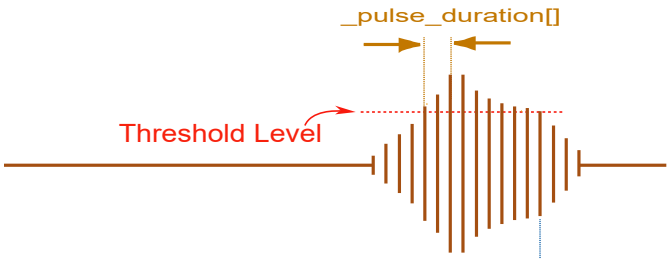


**Figure 22. AADD Parameter Visualization**

### 5.6.3. THRESHOLD ALGORITHMS

Once activated, the AAD D processing block waits for an acoustic signal in the voice band to exceed the defined conditions – threshold and minimum pulse duration. There are two threshold options: an absolute threshold (similar to AAD Analog, but with wider range and voice band filter), or relative threshold (a dynamic/adaptive threshold also with wide range and voice band filter). The absolute and relative threshold algorithms work in parallel and are described in more detail in the next section. Like AAD Analog, the AAD Digital block sets the WAKE pin high when stimulus exceeds the conditions, WAKE stays high while the stimulus remains at those levels and pulls WAKE low when the stimulus drops below the defined conditions. To enable one or both algorithms, the two-bit value ***AADD_ALGO_SEL[1:0]*** in register address 0x2D[7:6] is set. The relative algorithm is enabled by setting the lower of the two bits and the absolute algorithm is enabled with the upper bit. The default value of 0x3 enables both algorithms simultaneously.

### 5.6.4. ABSOLUTE THRESHOLD ALGORITHM

This is the simplest of the threshold settings and simply sets the threshold above which the AAD is triggered. AAD D is a more sophisticated version of the AAD A in that it incorporates parameters like a voice filter and configurable minimum pulse duration to help distinguish voice from background sound.

Setting the **AADD_ABS_TH** register defines the sound pressure level which will trigger the wake. It operates similar to AAD A, but with the ability to configure an additional voice filter and minimum pulse duration. It is an absolute value that, once the acoustic stimulus exceeds the defined threshold, the process of activating the WAKE pin is started. The absolute threshold is set by writing to the 13-bits in register ***AADD_ABS_TH[12:0]*** (reg addresses 0x32 and 0x31). The allowed range of values is 0x00F to 0x7BC.

### 5.6.5. ABSOLUTE THRESHOLD VALUES

| AADD_ABS_TH (HEX) | AADD_ABS_TH (DEC) | THRESHOLD (dB SPL) |
|---|---|---|
| F | 15 | 40 |
| 16 | 22 | 45 |
| 32 | 50 | 50 |
| 37 | 55 | 55 |
| 5F | 95 | 60 |
| A0 | 160 | 65 |
| 113 | 275 | 70 |
| 1E0 | 480 | 75 |
| 370 | 880 | 80 |
| 62C | 1580 | 85 |
| 7BC | 1980 | 87 |

Note: Values below 0xF or above 0x7BC are not supported or recommended.

**Table 20. Absolute Threshold Values**



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### 5.6.6. RELATIVE THRESHOLD ALGORITHM

The Relative Threshold mode operates in a way which allows the threshold to be dynamic, i.e. an instantaneous threshold, and is triggered if the signal exceeds the established SPL (running average background level) plus a configurable relative level, i.e. +6dB or +12dB. The configurable relative level also has an option of setting a floor below which this dynamic threshold will become static, and the instantaneous threshold level will be fixed at the floor level plus the relative level. This can be used to avoid false detections at lower SPLs.

In summary, the behavior of the threshold can be defined for the following scenarios:

- If the background noise level is less than the Floor -> The Instantaneous Threshold is fixed and is calculated from Floor + Relative Threshold
- If the background noise level is greater than the Floor -> The Instantaneous Threshold is dynamic and is calculated from background SPL + Relative Threshold

See Figure 23 for a graphical illustration.

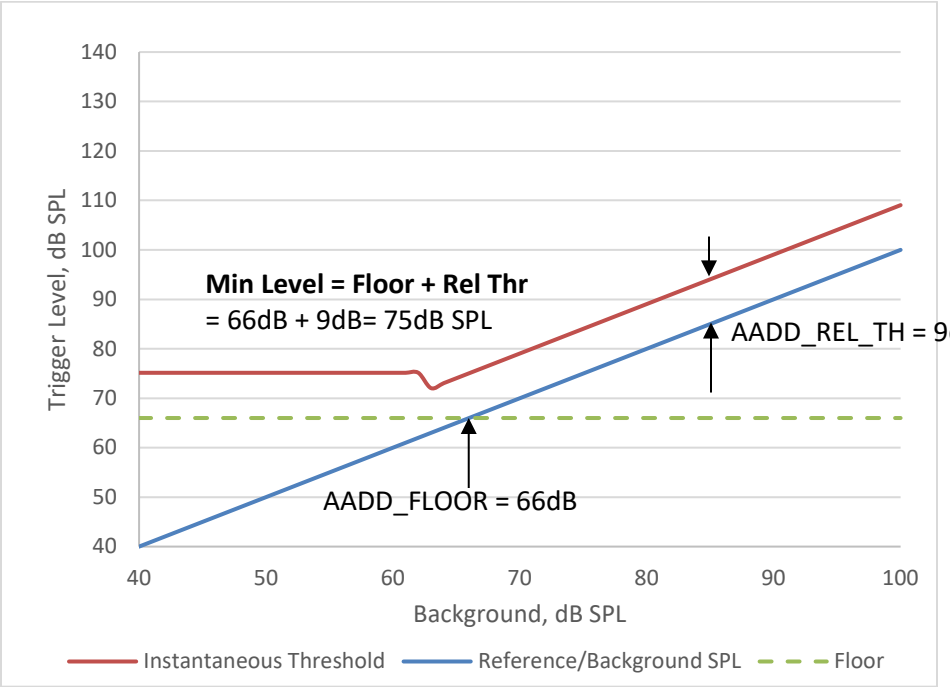


**Figure 23. Relative Threshold with floor indicated**



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### 5.6.7. RELATIVE THRESHOLD VALUES

| AADD_REL_TH (HEX) | AADD_REL_TH (DEC) | RELATIVE THRESHOLD (dB) |
|---|---|---|
| 24 | 36 | +3 |
| 36 | 50 | +6 |
| 48 | 72 | +9 |
| 64 | 100 | +12 |
| 8F | 143 | +15 |
| CA | 202 | +18 |
| FF | 255 | +20 |

**Table 21. Relative Threshold Values**

The floor level register ***AADD_FLOOR[12:0]***, in conjunction with the relative threshold register ***AADD_REL_TH[7:0]***, defines the required FLOOR level in relation to a background acoustic level after which the threshold tracks the background dB SPL as it increases and at a level above it defined by the **AADD_REL_TH** register. The allowed range for ***AADD_FLOOR[12:0]*** is 0x00F to 0x7BC. Values below 0x00F are not allowed. The allowed range for the **AADD_REL_TH** register is 0x24 to 0xFF.

For example, with ***AADD_FLOOR[12:0]*** = 0xFF (255d) the threshold level will be 69dB SPL.

### 5.6.8. FLOOR VALUES

| AADD_FLOOR [12:0] (HEX) | AADD_FLOOR [12:0] (DEC) | FLOOR LEVL (dB SPL) |
|---|---|---|
| F | 15 | 40 |
| 16 | 22 | 45 |
| 32 | 50 | 50 |
| 37 | 55 | 55 |
| 5F | 95 | 60 |
| A0 | 160 | 65 |
| 113 | 275 | 70 |
| 1E0 | 480 | 75 |
| 370 | 880 | 80 |
| 62C | 1580 | 85 |
| 7BC | 1980 | 87 |

Note: Values below 0xF or above 0x7BC are not supported or recommended.

**Table 22. Floor Values**

### 5.6.9. MINIMUM PULSE DURATION TIME

To prevent the acoustic activity detect circuitry triggering on every acoustic event that exceeds the defined threshold the system requires a minimum duration for the acoustic stimulus to be present before the AADD mode can be defined. This prevents the systems from activating on short duration acoustic impulses that might not be valid triggers. There are two pulse duration times that are configurable - one for Relative Threshold (**AADD_REL_PULSE_MIN[11:0]** at Reg0x2F[3:0] and Reg0x2E[7:0]) and the other for Absolute Threshold mode (**AADD_ABS_PULSE_MIN[11:0]** at Reg0x2F[7:4] and Reg0x30[7:0]).

The pulse minimum time for the relative threshold has a narrower configurable range compared to the option for the absolute threshold, due to the responsiveness of the relative threshold to the environment. It is not recommended to use a pulse minimum value above 0x12C for the AADD_REL_PULSE_MIN as this could result in unresponsive behavior for the relative algorithm.

These duration values scale with clock frequency. AAD-D2 mode uses a fixed internally derived 768 kHz clock and so these values are fixed for AAD-D2. In AAD-D1 mode, the internal clock is derived from the external clock provided and this means that, for this mode, the pulse duration values will vary depending on the clock frequency provided to the microphone. In this case, the values vary according to the following formula:

$$duration = \frac{register\ value * 72}{f_{clk}}$$

AADD_REL_PULSE_MIN and AADD_ABS_PULSE_MIN have approximately the same pulse times vs configuration values where their useable ranges overlap. A selection of values for each, assuming a clock frequency of 768 kHz is shown in Table 23 below:

### 5.6.10. MINIMUM PULSE DURATION TIME VALUES

| AADD_x_PULSE_MIN [11:0] (HEX) | AADD_x_PULSE_MIN [11:0] (DEC) | RELATIVE ALGORITHM MIN PULSE DURATION (ms) | ABSOLUTE ALGORITHM MIN PULSE DURATION (ms) |
|---|---|---|---|
| 0 | 0 | 0.7 | 1.1 |
| 64 | 100 | 10 | 10 |
| C8 | 200 | 19 | 19 |
| 12C | 300 | 29 | 29 |
| 1F4 | 500 | N/A | 48 |
| 3E8 | 1000 | N/A | 95 |
| 7D0 | 2000 | N/A | 188 |
| BB8 | 3000 | N/A | 282 |
| DAC | 3500 | N/A | 328 |

**Table 23. Minimum Pulse Duration**



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### 5.6.11. AAD D1 EXAMPLE CONFIGURATION AND ACTIVATION SEQUENCE

AAD Digital 1 can be activated with the following sequence of powerup conditions and register writes:

1. Apply Vdd, apply CLK > 50 kHz
2. Apply AAD Unlock write sequence:

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 1 | 0x5C | 0x00 |
| 2 | 0x3E | 0x00 |
| 3 | 0x6F | 0x00 |
| 4 | 0x3B | 0x00 |
| 5 | 0x4C | 0x00 |

3. Apply AAD D settings, ABS_TH = 0x113 (70dB SPL), FLOOR = 0x16 (45dB SPL), RE_TH = 0x24 (+3dB), REL_PULSE_MIN = 0x0, ABS_PULSE_MIN = 0

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 6 | 0x29 | 0x00 |
| 7 | 0x2A | 0x00 (FLOOR MSBs) |
| 8 | 0x2B | 0x16 (FLOOR LSBs) |
| 9 | 0x2C | 0x32 (Reserved; must be written for AAD D) |
| 10 | 0x2D | 0xC0 (ALGO_SEL) |
| 11 | 0x2E | 0x00 (REL_PULSE_MIN LSBs) |
| 12 | 0x2F | 0x00 (ABS_PULSE_MIN MSBs; REL_PULSE_MIN MSBs) |
| 13 | 0x30 | 0x00 (ABS_PULSE_MIN LSBs) |
| 14 | 0x31 | 0x13 (ABS_TH LSBs) |
| 15 | 0x32 | 0x41 (ABS_TH MSBs; bits[7:5] must be written to 0x2) |
| 16 | 0x33 | 0x24 (REL_TH) |

4. Enable AAD D1

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 17 | 0x29 | 0x01 |

   The microphone will acknowledge the enable by pulsing the WAKE pin HIGH for about 12 us.

5. Activate AAD D1 by setting CLK = 768 kHz. The microphone will now set the WAKE pin HIGH in response to acoustic stimulus in the voice band above the acoustic threshold.

### 5.6.12. AAD D2 EXAMPLE CONFIGURATION AND ACTIVATION SEQUENCE

AAD Digital 2 can be activated with the following sequence of powerup conditions and register writes:

1. Apply Vdd, apply CLK > 50 kHz
2. Apply AAD Unlock write sequence:

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 1 | 0x5C | 0x00 |
| 2 | 0x3E | 0x00 |
| 3 | 0x6F | 0x00 |
| 4 | 0x3B | 0x00 |
| 5 | 0x4C | 0x00 |

3. Apply AAD D settings, ABS_TH = 0x113 (70dB SPL), RE_TH = 0x24 (+3dB), FLOOR = 0x16 (45dB SPL), REL_PULSE_MIN = 0x0, ABS_PULSE_MIN = 0 (same as previous example configuration)

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 6 | 0x29 | 0x00 |
| 7 | 0x2A | 0x00 (FLOOR MSBs) |
| 8 | 0x2B | 0x16 (FLOOR LSBs) |
| 9 | 0x2C | 0x32 (Reserved; must be written for AAD D) |
| 10 | 0x2D | 0xC0 (ALGO_SEL) |
| 11 | 0x2E | 0x00 (REL_PULSE_MIN LSBs) |
| 12 | 0x2F | 0x00 (ABS_PULSE_MIN MSBs; REL_PULSE_MIN MSBs) |
| 13 | 0x30 | 0x00 (ABS_PULSE_MIN LSBs) |
| 14 | 0x31 | 0x13 (ABS_TH LSBs) |
| 15 | 0x32 | 0x41 (ABS_TH MSBs; bits[7:5] must be written to 0x2) |
| 16 | 0x33 | 0x24 (REL_TH) |

4. Enable AAD D2

| WRITE # | REGISTER ADDRESS (HEX) | REGISTER DATA (HEX) |
|---|---|---|
| 17 | 0x29 | 0x02 |

   The microphone will acknowledge the enable by pulsing the WAKE pin HIGH for about 12 us.

5. Activate AAD D2 by setting CLK to a frequency between 50 kHz and 200 kHz for 2 ms followed by setting CLK = OFF. The microphone will now set the WAKE pin HIGH in response to acoustic stimulus in the voice band above the acoustic threshold.

### 5.6.13. AAD D REGISTER MAP

| AAD Digital (AADD) Register Map | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| **29h** | Reserved | | | | AAD A_EN | Reserved | AAD D2_EN | AAD D1_EN |
| **2Ah** | Reserved | | | AADD_FLOOR[12:8] | | | | |
| **2Bh** | AADD_FLOOR[7:0] | | | | | | | |
| **2Ch** | Reserved | | | | | | | |
| **2Dh** | AADD_ALGO_SEL[1:0] | | Reserved | | | | | |
| **2Eh** | AADD_REL_PULSE_MIN[7:0] | | | | | | | |
| **2Fh** | AADD_ABS_PULSE_MIN[11:8] | | | | AADD_REL_PULSE_MIN[11:8] | | | |
| **30h** | AADD_ABS_PULSE_MIN[7:0] | | | | | | | |
| **31h** | AADD_ABS_THR[7:0] | | | | | | | |
| **32h** | Reserved | | | AADD_ABS_THR[12:8] | | | | |
| **33h** | AADD_REL_TH[7:0] | | | | | | | |
| **35h** | Reserved | | | | | Unused for AADD | | |
| **36h** | Reserved | | | | Unused for AADD | | | |

**Table 24. AADD Register Map**

## 5.7. AAD REGISTER RESET

The AAD configuration registers are reset by either of the following events.

- A full power cycle of the microphone
- Entering sleep mode, described below, with AAD disabled (addr 0x29[3:0] = 0x0).

In either case, the device returns to its default state when a clock greater than 24 kHz is provided.

# 6. THEORY OF OPERATION

## 6.1. POWER MANAGEMENT

The T5848 has three power states: High Quality Mode, Low Power Mode, and Sleep Mode.

### 6.1.1. STARTUP AND NORMAL OPERATION

Typical start-up time of the T5848 is less than 10 ms. The $I^2S$ data from the microphone is valid to be used as soon as the data is being output. The part is in normal operation (High Quality and Low Power modes) when SCK and WS are active.

### 6.1.2. SLEEP MODE

The microphone enters standby mode when the frequency of SCK falls below about 200 kHz. It is recommended to enter standby mode by stopping both the SCK and WS clock signals and pulling those signals to ground to avoid drawing current through the WS pin's internal pull-down resistor. The timing for exiting standby mode is the same as normal startup.

It is not recommended to supply active clocks (WS and SCK) to the T5848 while there is no power supplied to VDD. Doing this continuously turns on ESD protection diodes, which may affect long-term reliability of the microphone.

## 6.2. SYNCHRONIZING MICROPHONES

Stereo T5848 microphones are synchronized by the WS signal, so audio captured from two microphones sharing the same clock will be in sync. The two microphones will synchronously sample the acoustic signals at the beginning of the $I^2S$ frame (WS falling edge).

## 6.3. I²S DATA INTERFACE

The slave serial data port's format is I²S, two's complement. There must be 64 SCK cycles in each stereo WS frame when operating in High Quality Mode and 48 SCK cycles per frame in Low Power Mode. The LR control pin determines whether the T5848 outputs data in the left or right channel. When set to the left channel, the data will be output following WS's falling edge and when set to output on the right channel, data will be output following WS's rising edge.

For a stereo application, the SD pins of the left and right T5848 microphones should be tied together as shown in Figure 24.

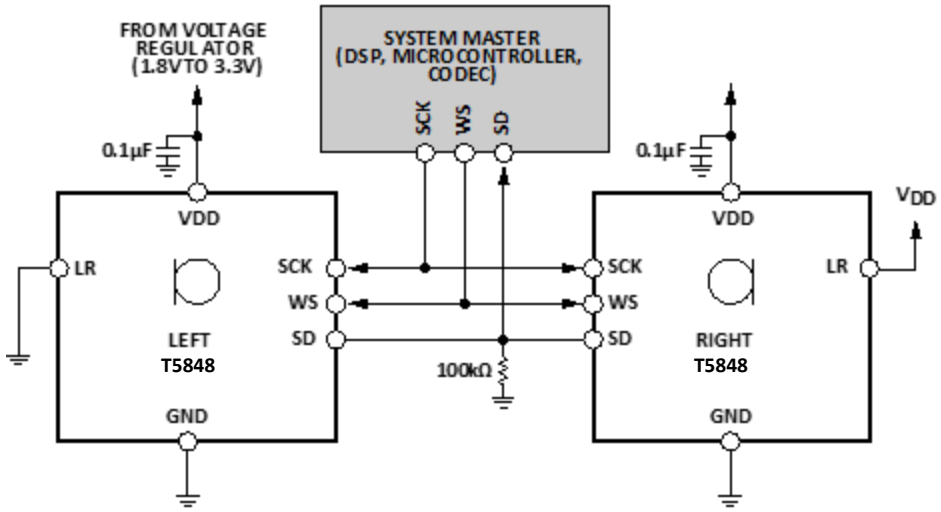


**Figure 24. System Block Diagram**

### 6.3.1. DATA OUTPUT MODE

The output data pin (SD) is tristated when it is not actively driving I²S output data. SD immediately tristates after the LSB is output so that another microphone can drive the common data line.

The SD trace should have a pull-down resistor to discharge the line during the time that all microphones on the bus have tristated their outputs. A 100 kΩ resistor is sufficient for this, as shown in Figure 24. If the SD line needs to be discharged faster than a 100 kΩ resistor can, a smaller resistor, such as 10 kΩ, can be used.

### 6.3.2. DATA WORD LENGTH

When the microphone is operated in High Quality Mode, the output data word length is 24 bits per channel. In Low Power Mode, the output data word length is 16 bits per channel.

### 6.3.3. DATA WORD FORMAT

The default data format is I²S (two's complement), MSB-first. In this format, the MSB of each word is delayed by one SCK cycle from the start of each half-frame.

### 6.3.4. HIGH QUALITY MODE DATA OUTPUT FORMAT

When operating in High Quality Mode, the output data word length is 24 bits/channel. In this mode, the microphone data has a precision of 20 bits. The unused 4 lowest bits are tied to ground.

The format of a stereo I²S data stream in HQM is shown in Figure 25. Figure 26 and Figure 27 show the formats of a mono microphone data stream for left and right microphones, respectively.

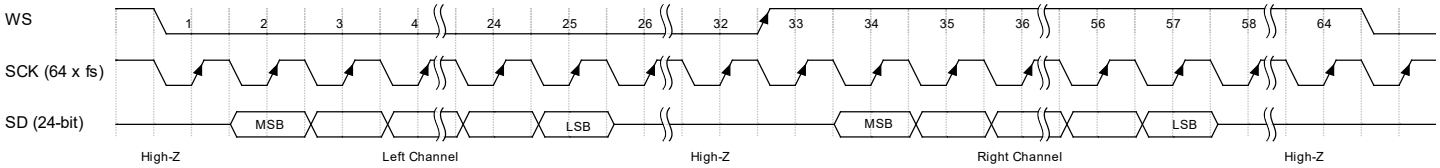


**Figure 25. High Quality Mode Stereo Output I²S Format**

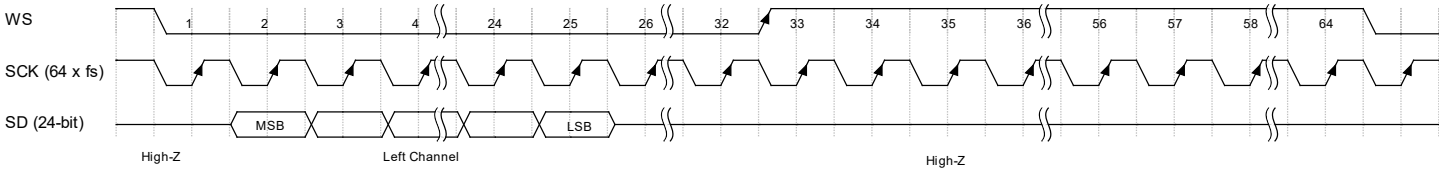


**Figure 26. High Quality Mode Stereo Left Channel (LR = 0)**

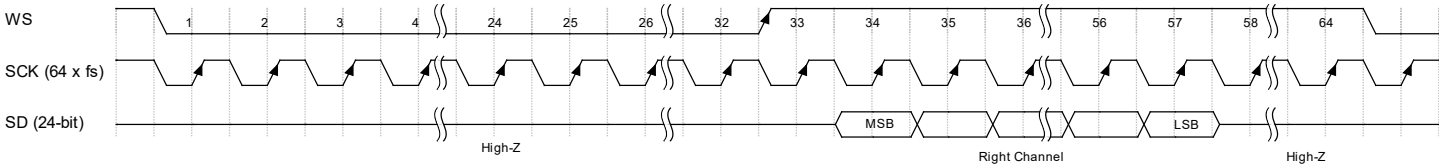


**Figure 27. High Quality Mode Stereo Right Channel (LR = 1)**



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### 6.3.5. LOW POWER MODE DATA OUTPUT FORMAT

In Low Power Mode, the output data word length is 16 bits/channel.

The format of a stereo I²S data stream in LPM is shown in Figure 28. Figure 29 and Figure 30 show the formats of a mono microphone data stream for left and right microphones, respectively.

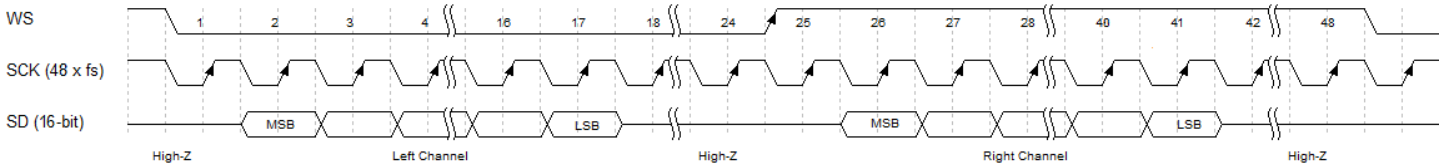


**Figure 28. Low Power Mode Stereo Output I²S Format**

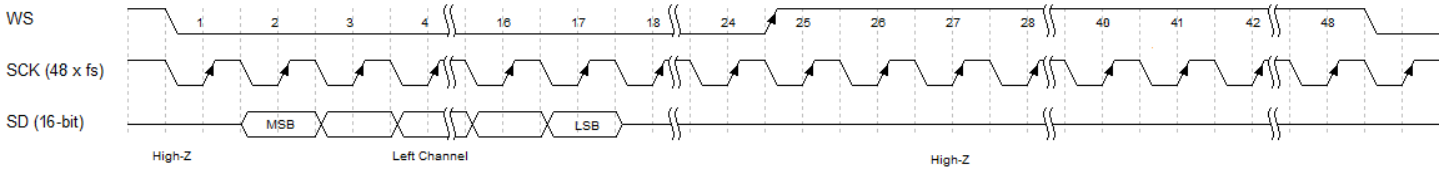


**Figure 29. Low Power Mode Stereo Left Channel (LR = 0)**

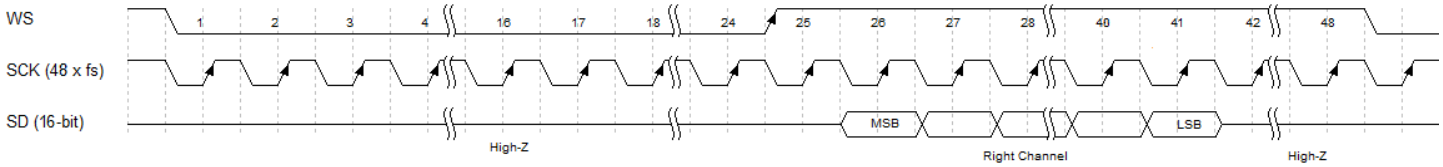


**Figure 30. Low Power Mode Stereo Right Channel (LR = 1)**



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## 6.4. DIGITAL MICROPHONE SENSITIVITY

The sensitivity of a digital output microphone is specified in units of dB FS (decibels relative to a full-scale digital output). A 0 dB FS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 31). This measurement convention means that signals with a different crest factor may have an RMS level higher than 0 dB FS. For example, a full-scale square wave has an RMS level of 3 dB FS.

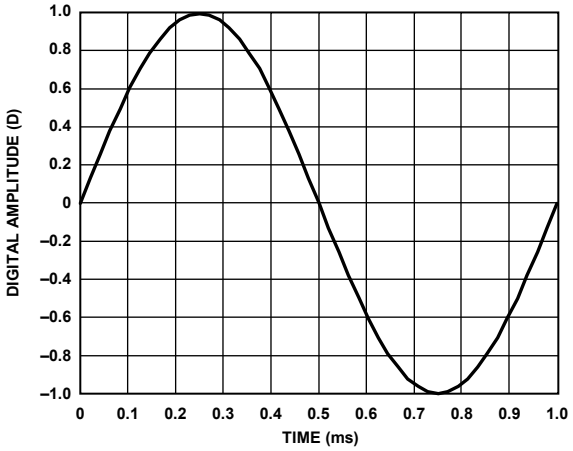


**Figure 31. 1 kHz, 0 dB FS Sine Wave**

The definition of a 0 dB FS signal must be understood when measuring the sensitivity of the T5848. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the T5848 in Low Power Mode results in an output signal with a −26 dB FS level. This means that the output digital word peaks at −26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −29 dB FS; however, this is not the case because of the definition of a 0 dB FS sine wave.

There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the RMS level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 31). In this case, a −26 dB FS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

## 6.5. DIGITAL FILTER CHARACTERISTICS

The T5848 has an internal digital bandpass filter. A high-pass filter eliminates unwanted low frequency signals. A low-pass decimation filter scales the pass band with the sampling frequency and performs required out-of-band noise reduction.

### 6.5.1. HIGH-PASS FILTER

The T5848 incorporates a high-pass filter to remove DC and low frequency components. This high pass filter has a −3 dB corner frequency of 27 Hz and does not scale with the sampling rate.

### 6.5.2. LOW-PASS DECIMATION FILTER

The analog-to-digital converter in the T5848 is a single-bit, high order, sigma-delta (Σ-Δ) running at a high oversampling ratio. The noise shaping of the converter pushes the majority of the noise well above the audio band and gives the microphone a wide dynamic range. However, it does require a good quality low-pass decimation filter to eliminate the high frequency noise.



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The pass band of the filter extends to 0.318 × $f_S$ and, in that band, has only ±0.3 dB of ripple. The stop-band attenuation of the filter is >60 dB.

### 6.5.3. HIGH QUALITY MODE FILTER BANDWIDTH

When the microphone is operated in High Quality Mode, the data is decimated by 64x resulting in $f_S = f_{clk} / 64$. This means that a 3.072 MHz clock results in a sample rate of 48 kHz and a high frequency corner of 15 kHz.

### 6.5.4. LOW POWER MODE FILTER BANDWIDTH

Low power mode uses a decimation rate of 48x resulting in $f_S = f_{clk} / 48$. For example, a 768 kHz clock results in a sample rate of 16 kHz and a high frequency corner of 5 kHz.

# 7. APPLICATIONS INFORMATION

## 7.1. LOW POWER MODE

Low Power Mode (LPM) enables the T5848 to be used in an AlwaysOn listening mode for keyword spotting and ambient sound analysis. The T5848 will enter LPM when the frequency of SCK is between 600 and 800 kHz. In this mode, the microphone consumes only 120 µA while retaining high electro-acoustic performance.

When one microphone is in LPM for AlwaysOn listening, a second microphone sharing the same data line may be powered down. In this case, where one microphone is powered up and another is powered down by disabling the VDD supply or in sleep mode by reducing the frequency of a separate clock source, the disabled microphone does not present a load to the signal on the LPM microphone's DATA pin.

## 7.2. ENTERING AND EXITING SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 200 kHz. In this mode, the microphone data output is in a high impedance state. The current consumption in sleep mode is 9 µA with a SCK active, 1uA with SCK OFF.

To exit sleep mode, a clock with a frequency in the range of 600 kHz to 800 kHz, for Low Power Mode, or 2 MHz to 3.7 MHz, for High Quality Mode, must be provided. The microphone wakes up from sleep mode and begins to output data 6 ms after the clock becomes active. The wake-up time indicates the time from when the clock is enabled to when the T5848 outputs data within 0.5 dB of its settled sensitivity.

## 7.3. SD OUTPUT DRIVE STRENGTH

The SD data output pin must drive a load that includes the PCB trace and the tri-stated inputs of the other T5848 SD pins connected to that same trace. The tri-stated load capacitance of the T5848 SD pin is about 6 pF. The T5848 has been designed to drive a load of 85 pF.

## 7.4. POWER SUPPLY DECOUPLING

For best performance and to avoid potential parasitic artifacts, placing a 0.1 µF ceramic type X7R or better capacitor between Pin 5 (VDD) and ground is strongly recommended. The capacitor should be placed as close to Pin 3 as possible.

The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the ground planes should be made on the far side of the capacitor, as shown in Figure 32.

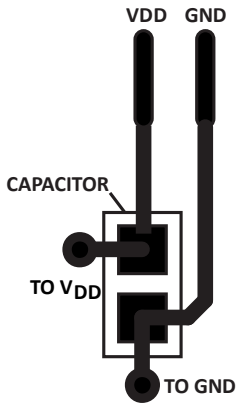


**Figure 32. Recommended Power Supply Bypass Capacitor Layout**



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# 8. SUPPORTING DOCUMENTS

For additional information, see the following documents.

## 8.1. APPLICATION NOTES – GENERAL

AN-100, *MEMS Microphone Handling and Assembly Guide*
AN-1003, *Recommendations for Mounting and Connecting the TDK, Bottom-Ported MEMS Microphones*
AN-1112, *Microphone Specifications Explained*
AN-1124, *Recommendations for Sealing TDK Bottom-Port MEMS Microphones from Dust and Liquid Ingress*
AN-1140, *Microphone Array Beamforming*
AN-000298, *T583x MEMS Microphone Acoustic Activity Detect User Guide*
AN-000376, *T5848 Flex EVB User Guide*

# 9. PCB DESIGN AND LAND PATTERN LAYOUT

The recommended PCB land pattern for the T5848 is a 1:1 ratio of the solder pads on the microphone package, as shown in Figure 33. Avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 34.

The response of the T5848 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.375 mm in diameter). A 0.5 mm to 1 mm diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.

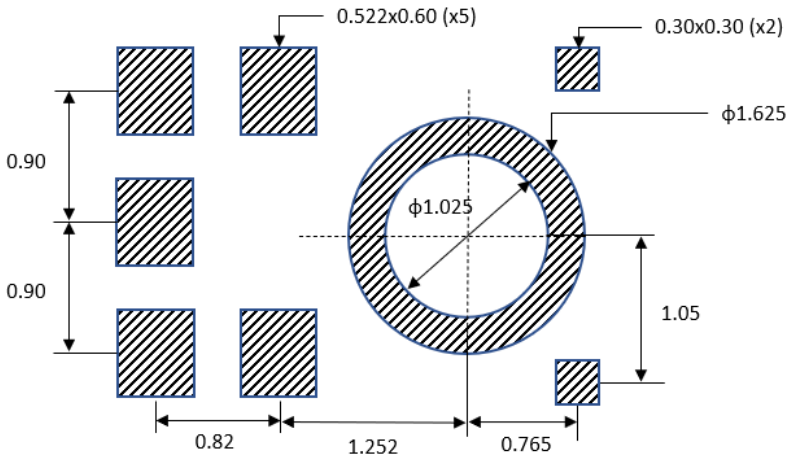


**Figure 33. Recommended PCB Land Pattern Layout**

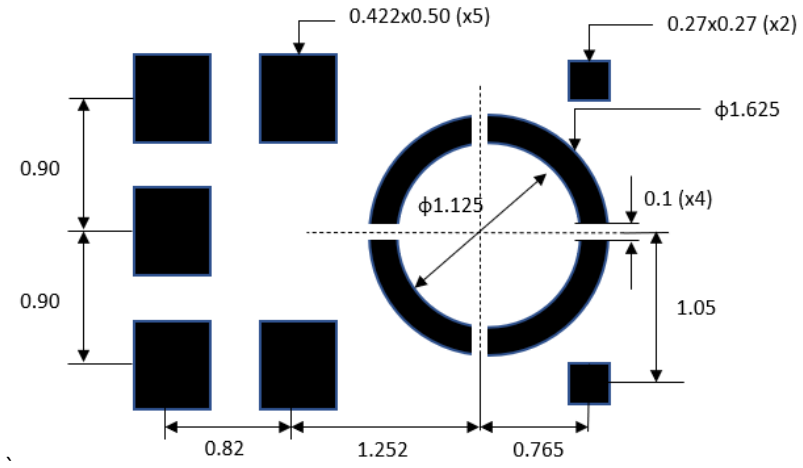


**Figure 34. Suggested Solder Paste Stencil Pattern Layout**

## 9.1. PCB MATERIAL AND THICKNESS

The performance of the T5848 is not affected by PCB thickness. The T5848 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.



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# 10. HANDLING INSTRUCTIONS

## 10.1. PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone.
  Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

## 10.2. REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 9.

## 10.3. BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

## 11. OUTLINE DIMENSIONS

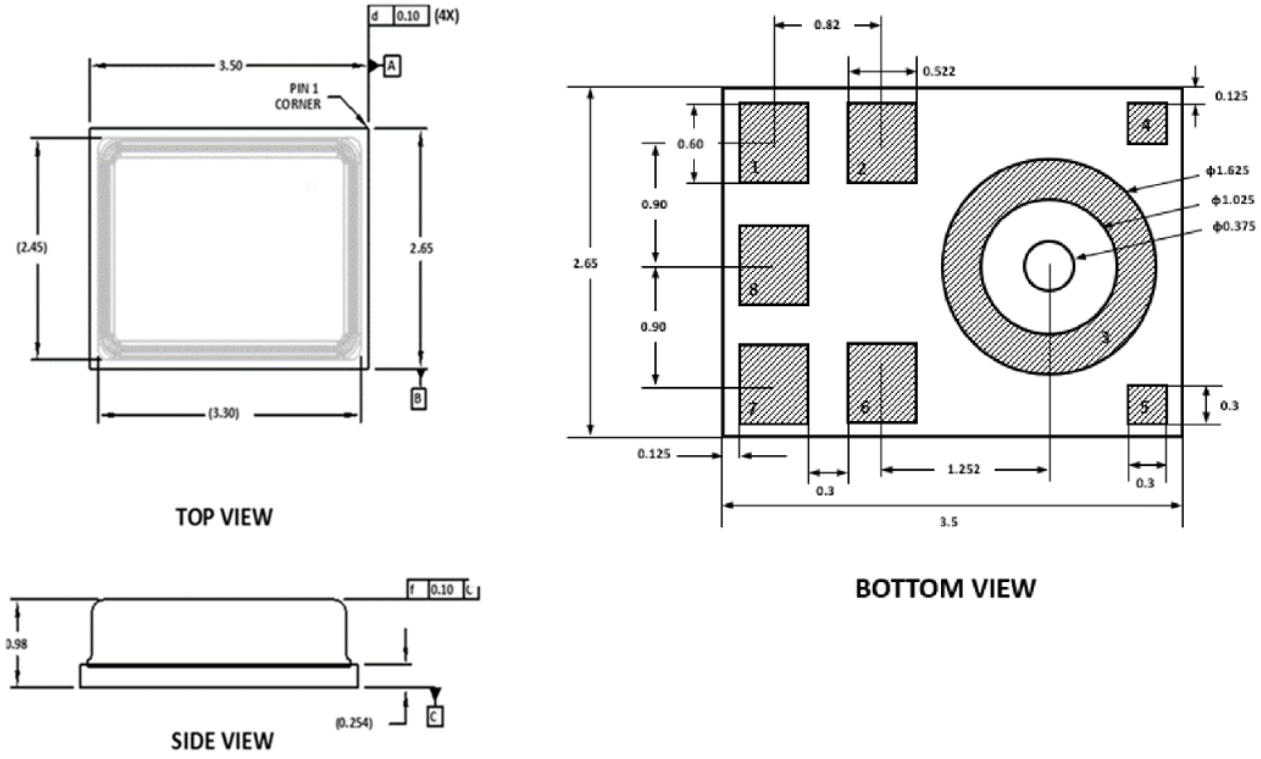


**Figure 35. 8-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]**
**3.5 mm × 2.65 mm × 0.98 mm Body**
**Dimensions shown in millimeters**
**Dimension tolerance is ±0.15 mm unless otherwise specified**

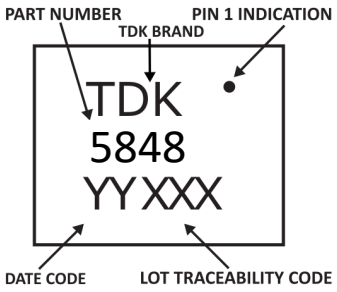


**Figure 36. Package Marking Specification (Top View)**



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# 12. RELIABILITY SPECIFICATIONS

| Test | Standard | Conditions |
|---|---|---|
| Early Life Failure Rate (ELFR) | JEDEC JESD22-A108 | $T_j \geq 125°C$, VDD max, 48 hrs. |
| Temperature Humidity Bias (THB) | JEDEC JESD22-A101 | Biased, 85°C, 85% RH, 1000 hrs. Preceded with JESD22-A113 MSL 1 Preconditioning |
| High Temperature Operating Life (HTOL) | JEDEC JESD22-A108 | $T_j \geq 125°C$, VDD max, 1000 hrs. |
| High Temperature Storage life (HTS) | JEDEC JESD22-A103 | Un-biased bake: Condition B, $T_a \geq 150$ (-0/+10) °C |
| Temperature Cycling (TC) | JEDEC JESD22 A104 | -40 to +125°C, Soak Mode 2: 5 min, Preceded with JESD22-A113 MSL 1 preconditioning. |
| ESD Human-Body Model (ESD-HBM) | ANSI/ESDA/JEDEC JS-001-2014 | 1.5 kV, 2.0 kV, All pins, 1 zap per polarity. |
| ESD Charged Device Model (ESD-CDM) | JESD22-C101 | 250 V, 500 V, Std. Sample, 1 zap per polarity. |
| Latch-up (LU) | JEDEC JESD-78 | $I_{inj}$ = ± 100 mA; $V_{os}$ = 1.5*Vdd max at 85°C, Class II. |
| Vibration (VIB) | MIL-STD-883K-CHG3, Method 2007.3, Condition B | 20 Hz-2 kHz, ≥4 min/cycle, 4 cycles, 50 g peak accel. |
| Random Drop (RD) | AEC-Q100, Test G5 | 18 free-fall drops from 1.2 m on concrete surface. |
| Mechanical Shock Test (MS) | IEC 60068-2-27, Condition E. | 10,000 g, 0.1 ms pulse, ±X, ±Y, ±Z – 5 shock pulses, 6 directions |

**Note:** Microphone sensitivity variations shall not exceed 3 dB over the lifetime of the device.

**Table 25. Reliability Specifications**

# 13. ORDERING GUIDE

| PART | TEMP RANGE | PACKAGE | QUANTITY | PACKAGING |
|---|---|---|---|---|
| MMICT5848-00-012 | –40°C to +85°C | 5-Terminal LGA_CAV | 10,000 | 13” Tape and Reel |
| EV_T5848-FX2 | - | Flex Evaluation Board | - | |

# 14. REVISION HISTORY

| REVISION DATE | REVISION | DESCRIPTION |
|---|---|---|
| 3/18/2024 | 1.0 | Initial Release |

## 15. COMPLIANCE DECLARATION DISCLAIMER

TDK believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. TDK subcontracts manufacturing, and the information contained herein is based on data received from vendors and suppliers, which has not been validated by TDK.