IAM-20680HV

High Performance Automotive 6-Axis MotionTracking Device

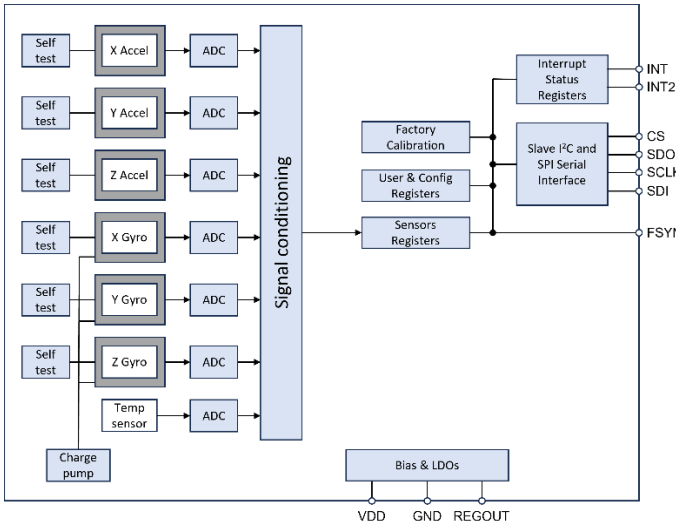
GENERAL DESCRIPTION

The IAM-20680HV is a 6-axis MotionTracking device for Automotive non-safety applications that combines a 3-axis gyroscope and a 3-axis accelerometer in a thin 3x3x0.75mm^3 (16-pin LGA) package. IAM-20680HV, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The gyroscope has a programmable full-scale range of ±125dps, ±250dps, ±500dps and ±1000dps. The accelerometer has a user-programmable full-scale range of ±2g, ±4g, ±8g and ±16g. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and two programmable interrupts. The device features I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

BLOCK DIAGRAM



APPLICATIONS

IAM-20680HV address a wide range of Automotive applications, including but not limited to:

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detection
- Location for Vehicle to Vehicle and Infrastructure
- View Camera Stabilization and Vision Systems
- Head-up display (HUD) and augmented reality HUD
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

ORDERING INFORMATION

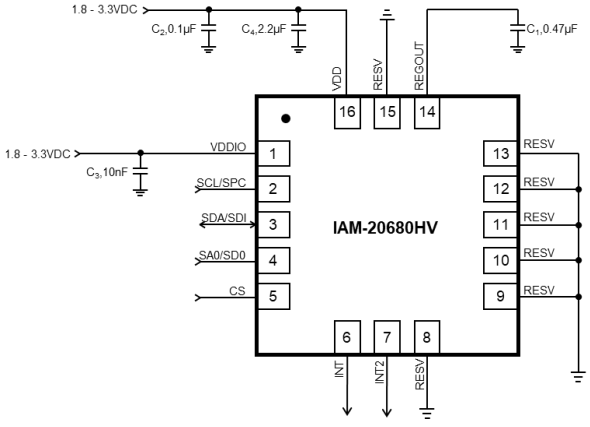
PART†	AXES	TEMP RANGE**	PACKAGE	MSL*
IAM-20680HV	X, Y, Z	-40°C to +125°C	16-Pin LGA	3

†Denotes RoHS and Green-compliant package
* Moisture sensitivity level of the package
** Datasheet parameters guaranteed up to 105°C

FEATURES

- Digital-output X-, Y- and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±125dps, ±250dps, ±500dps and ±1000dps, integrated 16-bit ADCs.
- Digital-output X-, Y- and Z-axis accelerometer with a user-programmable full-scale range of ±2g, ±4g, ±8g and ±16g and integrated 16-bit ADCs.
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor.
- Embedded Self-test.
- Two interrupt lines.
- Wake-on-Motion interrupt for low-power operation of applications processor.
- Reliability testing performed according to AEC–Q100: PPAP and qualification report available upon request.

TYPICAL OPERATING CIRCUIT



TDK-InvenSense, Inc. reserves the right to change specifications and information herein without notice unless the product is in mass production and the datasheet has been designated by TDK-InvenSense in writing as subject to a specified Product / Process Change Notification Method regulation.

InvenSense, Inc.
1745 Technology Drive, San Jose, CA 95110 U.S.A
+1(408) 988–7339
www.invensense.com

Document Number: DS-000612
Revision: 1.0
Rev. Date: 02/26/2025

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing description, specifications, and design related information on the IAM-20680HV Automotive MotionTracking device. The device is housed in a thin 3x3x0.75 mm^3 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The IAM-20680HV is a 6-axis MotionTracking device for Automotive non-safety applications, that combines a 3-axis gyroscope and a 3-axis accelerometer in a thin 3x3x0.75 mm^3 (16-pin LGA) package. IAM-20680HV, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The gyroscope has a programmable full-scale range of ±125 dps, ±250 dps, ±500 dps and ±1000 dps. The accelerometer has a user-programmable full-scale range of ±2g, ±4g, ±8g and ±16g. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using either I^{2}C at 400 kHz or SPI at 8 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK-InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75 mm^3 (16-pin LGA), to provide a very small yet high-performance. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detections
- Accurate Location for Vehicle to Vehicle and Infrastructure
- View Camera Stabilization and Vision Systems
- Head-up display (HUD) and augmented reality HUD
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the IAM-20680HV includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±125 dps, ±250 dps, ±500 dps and ±1000 dps and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in IAM-20680HV includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* and integrated 16-bit ADCs
- Two user-programmable interrupts
- Per-axis Wake-on-Motion (WoM) interrupt for low-power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The IAM-20680HV includes the following additional features:

- Thinnest LGA package for automotive applications: 3x3x0.75 mm^3 (16-pin LGA)
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- 10,000*g* shock tolerant
- 400 kHz Fast Mode I^2C for communicating with all registers
- 8 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, Full Scale = 1000dps, Low-Noise Mode enabled unless otherwise noted.

All Zero-rate output, sensitivity, and noise specifications include board soldering effects, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Full-Scale Range	FS_SEL=0		±125		dps	3
	FS_SEL=1		±250		dps	3
	FS_SEL=2		±500		dps	3
	FS_SEL=3		±1000		dps	3
Gyroscope ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		262		LSB/(dps)	3
	FS_SEL=1		131		LSB/(dps)	3
	FS_SEL=2		65.5		LSB/(dps)	3
	FS_SEL=3		32.8		LSB/(dps)	3
Sensitivity Scale Factor Tolerance	All axes, 25°C		±1.5		%	1,2,5
Sensitivity Scale Factor Variation over Temperature	All axes, -40°C to +105°C, initial		±1.8		%	1,2,5
Nonlinearity	Best fit straight line, 25°C		±0.1		%	1,5
Cross-Axis Sensitivity	25°C		±1.0		%	1,5
ZRO Tolerance	All axes combined, 25°C		±1.0		dps	1,2,5
ZRO Variation Over Temperature	All axes combined, -40°C to +105°C		±1.2		dps	1,2,5
Rate Noise Spectral Density	25°C, initial, Noise BW = 306 Hz, VDD = VDDIO = 1.8V		0.005		dps/√Hz	1,4,5
Gyroscope Start Up Time	From Sleep mode, 25°C		35		ms	1,5
Output Data Rate		4		8000	Hz	3

Table 1. Gyroscope Specifications

Notes:

1. Based on characterization or validation data on a limited number of parts.
2. Tested in production at component level. Over temperature tests are performed at 25°C, 105°C, and/or -40°C.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.
5. Typical specifications are not guaranteed.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, Full Scale = 8*g*, Low-Noise Mode enabled unless otherwise noted.

All Zero-g output, sensitivity, and noise specifications include board soldering effects, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Full-Scale Range	AFS_SEL=0		±2		g	3
	AFS_SEL=1		±4		g	3
	AFS_SEL=2		±8		g	3
	AFS_SEL=3		±16		g	3
ADC Word Length			16		bits	3
Sensitivity Scale Factor	AFS_SEL=0		16,384		LSB/g	3
	AFS_SEL=1		8,192		LSB/g	3
	AFS_SEL=2		4,096		LSB/g	3
	AFS_SEL=3		2,048		LSB/g	3
Sensitivity Scale Factor Tolerance	All axes, 25°C		±0.5		%	1,2,5
Sensitivity Scale Factor Variation Over Temperature	All axes, -40°C to +105°C, initial		±0.8		%	1,2,5
Nonlinearity	Best Fit Straight Line for 2g, 25°C		±0.05		%	1,5
Cross-Axis Sensitivity	25°C		±1		%	1,5
Zero-G Level Tolerance	All axes combined, 25°C		±60		mg	1,2,5
Zero-G Level Variation Over Temperature	All axes combined, -40°C to +105°C		±60		mg	1,2,5
Power Spectral Density	Low-noise mode, +25°C, initial, Noise BW = 235 Hz, VDD = VDDIO = 1.8V		135		µg/√Hz	1,4,5
Accelerometer Start-up Time	From Sleep mode, 25°C			20	ms	1
Output Data Rate		4		4000	Hz	3

Table 2. Accelerometer Specifications

Notes:

1. Based on characterization or validation data on a limited number of parts.
2. Tested in production at component level. Over temperature tests are performed at 25°C, 105°C, and/or -40°C.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.
5. Typ specifications are not guaranteed.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, Low-Noise Mode enabled unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
VDD		1.71	1.8	3.6	V	3 (max), 4 (min)
VDDIO		1.71	1.8	3.6	V	3 (max), 4 (min)
Supply current	6-axis Gyroscope + Accelerometer, -40°C to +105°C		3	3.75	mA	1
	3-axis Gyroscope		2.6		mA	1
	3-axis Accelerometer, 4 kHz ODR		390		µA	1
Full-Chip Sleep Mode current			6		µA	5
Specified Temperature Range	Performance parameters are guaranteed	-40		105	°C	1,2
Operating Temperature Range	Device can operate without reliability impact but performances are not guaranteed between 105°C and 125°C	-40		125	°C	1,2,3

Table 3. D.C. Electrical Characteristics

Notes:

1. Based on characterization or validation data on a limited number of parts.
2. Based on qualification.
3. Functionality in the operating temperature range is proven by HTOL executed at 125°C, 1000h.
4. Guaranteed by design
5. Tested in production

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
Room Temperature Offset	25°C		0		°C	2
Sensitivity	Untrimmed		326.8		LSB/°C	2
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
	From sleep			5	ms	1
I^2C ADDRESS	SA0 = 0 SA0 = 1		1101000 1101001			2
DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	1
C_I, Input Capacitance			< 10		pF	1
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	1
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink current			0.1	V	1
Output Leakage Current	OPEN=1		100		nA	1
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	1
I^2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO+0.5V	V	1
V_{hys}, Hysteresis			0.1*VDDIO		V	1
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	1
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	1
Output Leakage Current			100		nA	1
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	1
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3 SMPLRT_DIV=0		32		kHz	2
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6 or gyro inactive; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6 or gyro inactive	-10		+10	%	1
	CLK_SEL=1,2,3,4,5 and gyro active	-1		+1	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Based on validation data on a limited number of parts.
2. Guaranteed by design.

3.3.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	1
	High Speed Characterization		1	8	MHz	1,2
SPI Modes			Modes 0 and 3			
I²C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 5. Other Electrical Specifications

Notes:

1. Based on validation data on a limited number of parts.
2. SPI clock duty cycle between 45% and 55% should be used for 8-MHz operation.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING (I²C FAST-MODE)						
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 6. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage, mounted on evaluation board or in sockets.

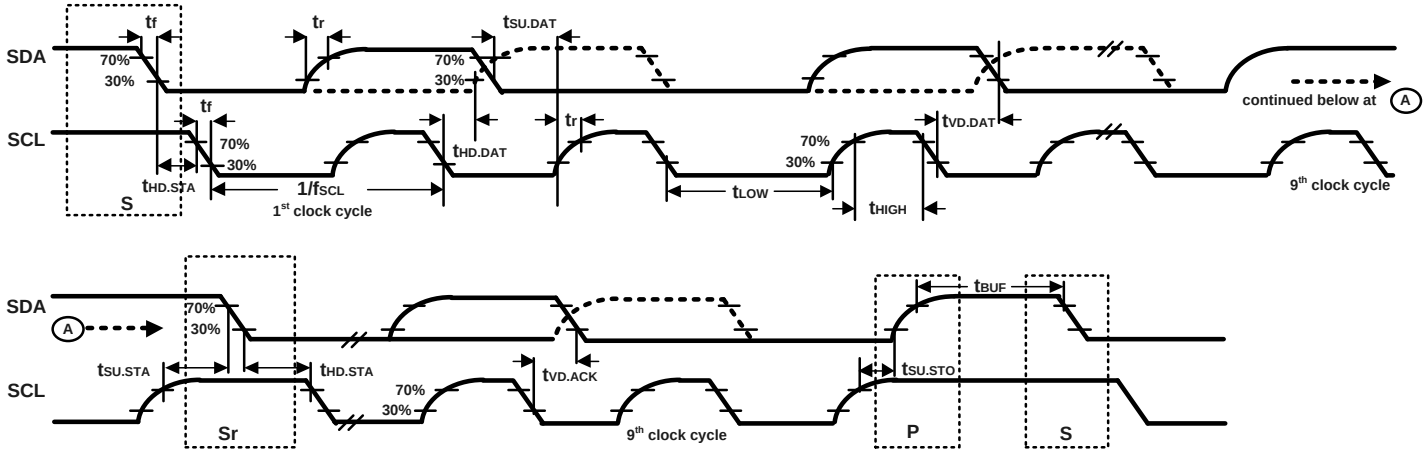


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SPC Clock Frequency				8	MHz	1
t_{LOW}, SPC Low Period		56			ns	1
t_{HIGH}, SPC High Period		56			ns	1
$t_{SU.CS}$, CS Setup Time		2			ns	1
$t_{HD.CS}$, CS Hold Time		63			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			40	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	6			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1
t_{Fall}, SCLK Fall Time				6.5	ns	2
t_{Rise}, SCLK Rise Time				6.5	ns	2

Table 7. SPI Timing Characteristics (8 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage, mounted on evaluation board or in sockets.
2. Based on other parameter values.

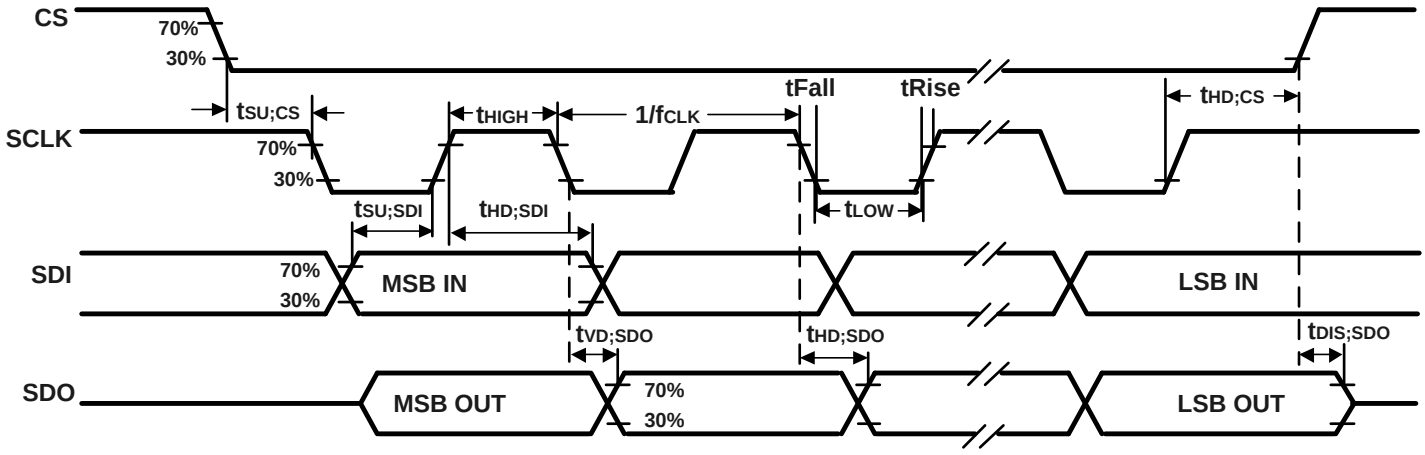


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING	NOTES
Supply Voltage, VDD	-0.5V to 4V	
Supply Voltage, VDDIO	-0.5V to 4V	
REGOUT	-0.5V to 2V	
Input Voltage Level (SA0, FSYNC, SCL, SDA)	-0.5V to VDDIO + 0.5V	
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2ms	
Specified Temperature Range	-40°C to 105°C	1
Operating Temperature Range	-40°C to 125°C	2
Storage Temperature Range	-40°C to 125°C	
Electrostatic Discharge (ESD) Protection	2 kV (HBM) 750V (CDM corner pins) 500V (CDM all other pins)	
Latch-up	JEDEC Class II (2),125°C ±100 mA	
Ultrasonic excitation (cleaning/welding/…)	Not allowed	

Table 8. Absolute Maximum Ratings

Notes:

1. Datasheet limits are guaranteed.
2. Datasheet limits are NOT guaranteed beyond Specified Temperature range but the component can operate without damage.

3.7 THERMAL INFORMATION

THERMAL METRIC	DESCRIPTION	VALUE
θ_{JA}	Junction-to-ambient thermal resistance	84.58 °C/W
ψ_{JT}	Junction-to-top characterization parameter	7 °C/W

Table 9. Thermal Information

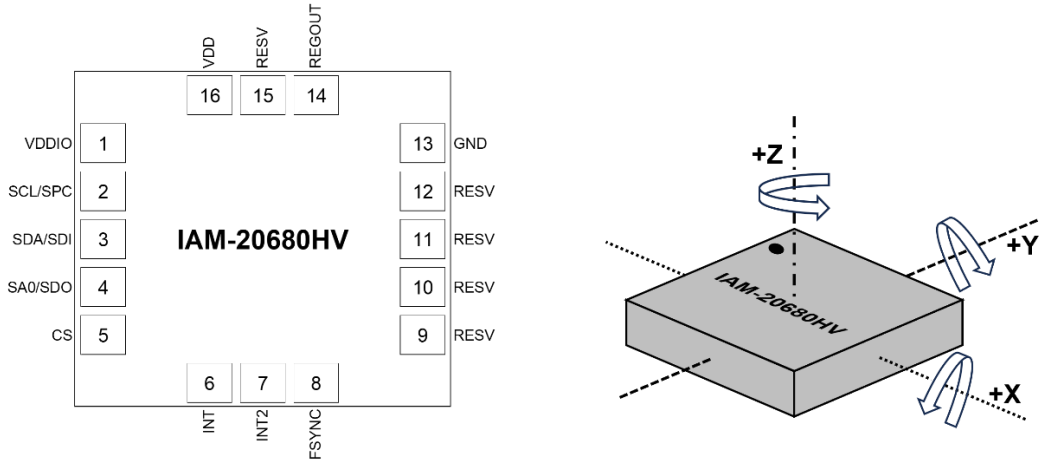
4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage
2	SCL/SPC	I^2C serial clock (SCL); SPI serial clock (SPC)
3	SDA/SDI	I^2C serial data (SDA); SPI serial data input (SDI)
4	SA0/SDO	I^2C slave address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I^2C mode)
6	INT	Interrupt digital output (push-pull or open-drain)
7	INT2	Second Interrupt digital output (push-pull or open-drain)
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused
9	RESV	Reserved. Connect to GND
10	RESV	Reserved. Connect to GND
11	RESV	Reserved. Connect to GND
12	RESV	Reserved. Connect to GND
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND
16	VDD	Power Supply

Table 10. Signal Descriptions

Note: VDD, VDDIO, SCL/SPC and CS pins must be correctly managed at power-up to guarantee proper IAM-20680HV start-up. Please refer to sections 4.17.1 and 4.17.2 for detailed power-up instructions.



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and Thickness

Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for IAM-20680HV 3.0x3.0x0.75mm³ LGA

4.2 TYPICAL OPERATING CIRCUIT

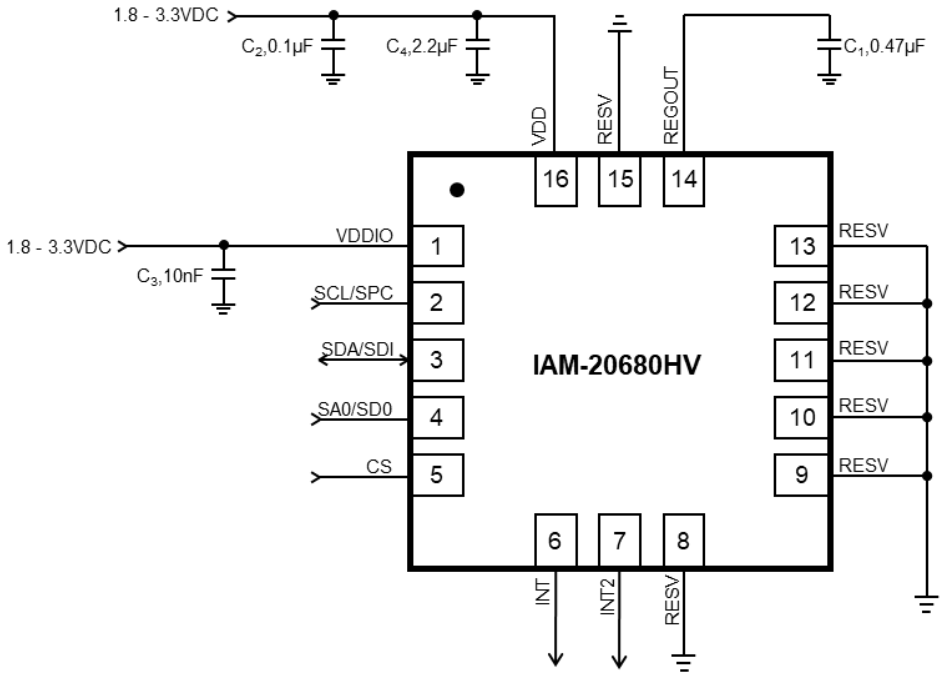


Figure 4. IAM-20680HV LGA Application Schematic

Note: I^2C lines are open drain and pullup resistors (e.g. 10 kΩ) are required.

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	X7R, 0.47 µF ±10%	1
VDD Bypass Capacitors	C2	X7R, 0.1 µF ±10%	1
	C4	X7R, 2.2 µF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10 nF ±10%	1

Table 11. Bill of Materials

4.4 BLOCK DIAGRAM

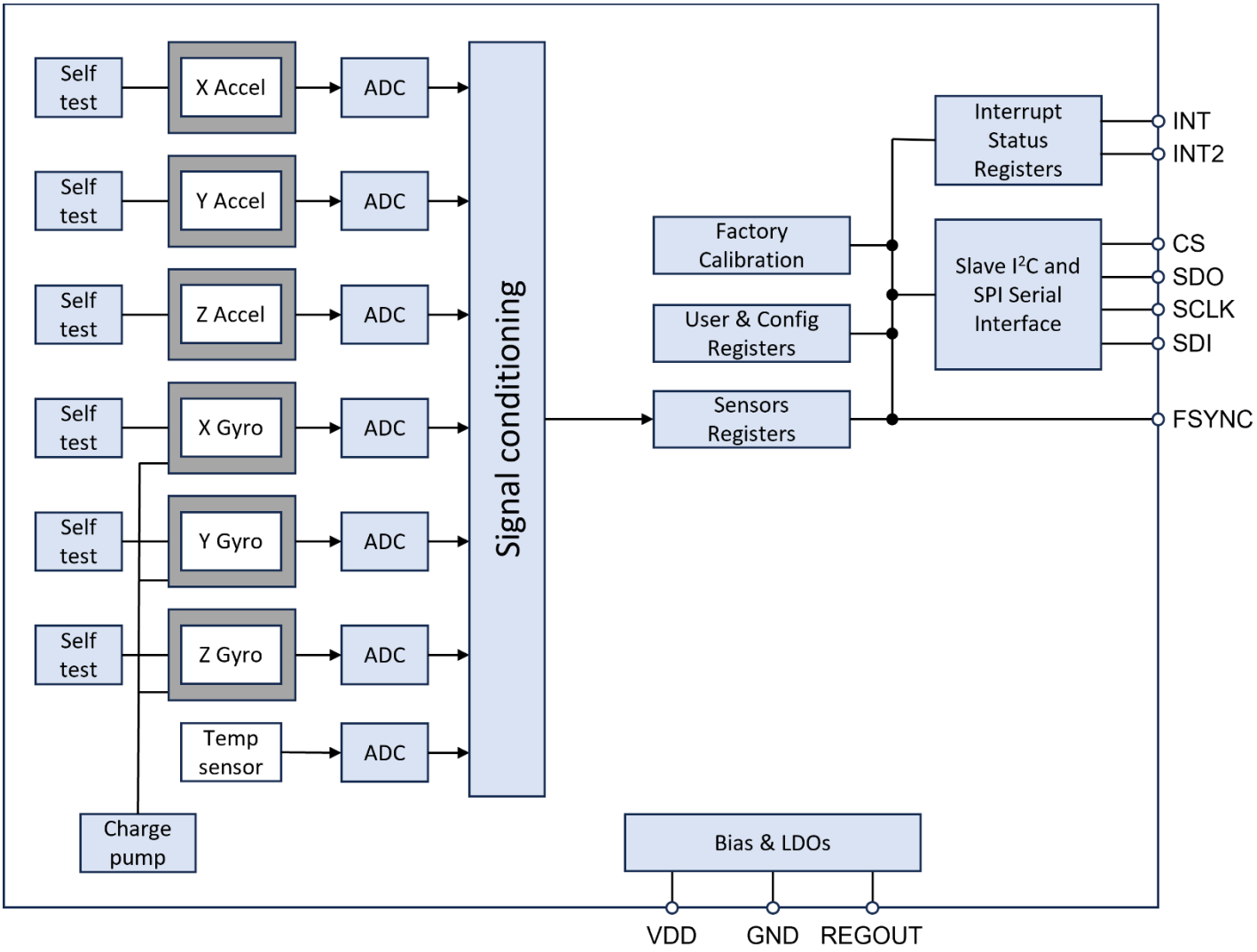


Figure 5. IAM-20680HV Block Diagram

4.5 OVERVIEW

The IAM-20680HV is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- Two independent Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20680HV consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±125, ±250, ±500 or ±1000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20680HV's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The IAM-20680HV's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.8 I²C AND SPI SERIAL COMMUNICATIONS INTERFACES

The IAM-20680HV communicates to a system processor using either a SPI or an I²C serial interface. The IAM-20680HV always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 4 (SA0).

4.8.1 IAM-20680HV Solution Using I²C Interface

In Figure 6, the system processor is an I²C master to the IAM-20680HV.

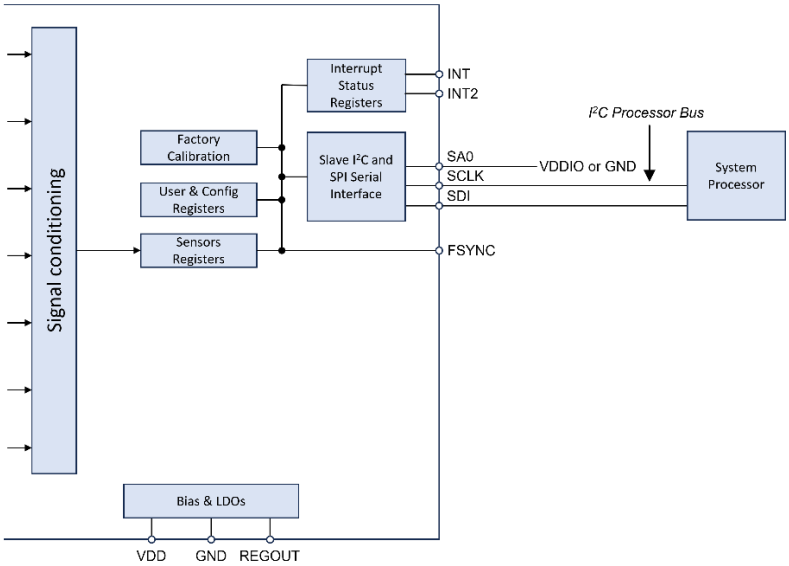


Figure 6. IAM-20680HV Solution Using I²C Interface

4.8.2 IAM-20680HV Solution Using SPI Interface

In Figure 7, the system processor is an SPI master to the IAM-20680HV. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

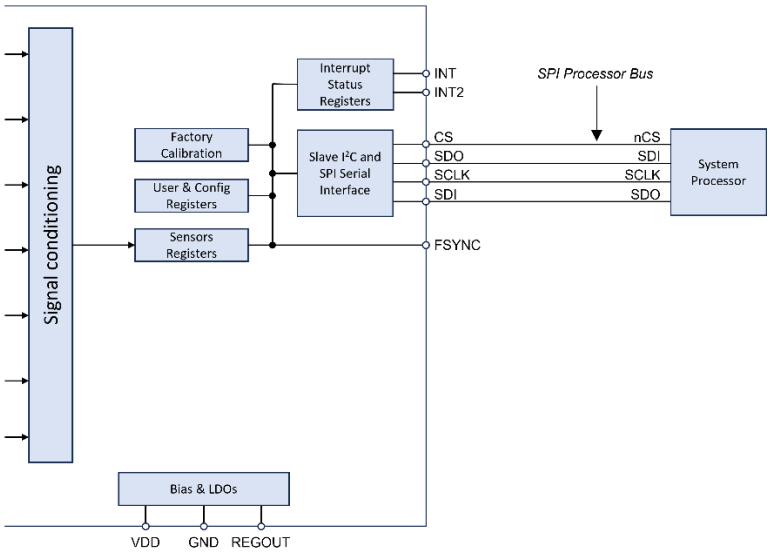


Figure 7. IAM-20680HV Solution Using SPI Interface

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers (registers 27 and 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 CLOCKING

The IAM-20680HV has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are new data available to be read from Data registers and wake on motion. The interrupt status can be read from the Interrupt Status register.

4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the IAM-20680HV die temperature. The readings from the ADC can be read from the Sensor Data registers.

4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IAM-20680HV. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.16 STANDARD POWER MODES

Table 12 lists the user-accessible power modes for IAM-20680HV.

MODE	NAME	GYRO	ACCEL
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Wake-on-Motion (WoM) Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Noise Mode	On	Off
6	6-Axis Low-Noise Mode	On	On

Table 12. Standard Power Modes for IAM-20680HV

Notes:

1. Power consumption for individual modes can be found in section 3.3.1.

4.17 SENSOR INITIALIZATION AND BASIC CONFIGURATION

The basic configuration of the IAM-20680HV includes the following steps:

- Power-up sequence
- Sensor initialization and clock source selection
- Digital interface access test
- Output data rate (i.e. sampling frequency) selection
- Full scale range selection
- Filter frequency selection
- Power mode selection

4.17.1 Power-up sequence

When applying VDD, the power voltage ramp is detected and a power-on-reset sequence is triggered inside the component. During this phase the device starts operating and internal logic levels are defined. For proper component initialization the power-up should be performed with both CS and SCL/SPC low, ensuring that CS and SCL pins are not in an undetermined state during the VDD ramp. If starting in I^2C mode (CS at logic high), power-up should be performed with SCL/SPC low. Power-up with SCL/SPC high is not a supported case and must be avoided.

It is worth noting that if the I/O pins (e.g. CS, SCL/SPC) are between V_{IL} and V_{IH} when the power-on-reset sequence is triggered, their value is undetermined and the internal logic levels may not be properly defined. It should also be noted that V_{IL} and V_{IH} are related to VDDIO and their value changes at power-up according to the applied VDDIO voltage ramp.

Power-up sequences that do not respect the conditions above may not lead to proper digital interface initialization. In this case a preliminary soft reset operation (PWR_MGMT_1 register set 0x81) must be performed to reset the digital interface, as soon as both VDD and VDDIO are stable at their final voltage. Since the digital interface may not be properly initialized, the device may not provide the acknowledge signal if the I^2C protocol is used.

4.17.2 Sensor Initialization and Clock Source Selection

When power-up sequence is completed (as per section 4.17.1), a soft reset is required to initialize the sensor and let the IAM-20680HV select the best clock source. The soft reset must be performed by setting the register PWR_MGMT_1 (address 0x6B) to 0x81 (see section 9.26), prior to registers initialization.

Soft reset must be performed as first operation after the power-up sequence to ensure the proper component registers setting. Correct WHO_AM_I value is ensured only after the soft reset has been completed.

4.17.3 Digital interface access test

When soft reset is completed, make sure the component registers access can be done as expected. WHO_AM_I (address 0x75) register can be used for this purpose to verify the identity of the device.

4.17.4 Output Data Rate Selection

To set the output data rate (ODR) to the desired frequency, select the sample rate divider by setting the register SMPLRT_DIV (address 0x19) to the desired value (see section 9.9). For instance, to set the output data rate to 100 Hz, write 0x09 into SMPLRT_DIV.

4.17.5 Full-Scale Range Selection

To set the full-scale range (FSR) of the accelerometer, set the register ACCEL_CONFIG (address 0x1C) to the desired value (see section 9.12). For instance, to set the FSR of the accelerometer to 2g, write 0x00 into ACCEL_CONFIG.

To set the FSR of the gyroscope, set the register GYRO_CONFIG (address 0x1B) to the desired value (see section 9.11). For instance, to set the FSR of the gyroscope to 250 dps, write 0x00 into GYRO_CONFIG.

4.17.6 Filter Selection

To set the corner frequency of the digital low-pass filter (DLPF) of the accelerometer, set the register ACCEL_CONFIG2 (address 0x1D) to the desired value (see section 9.13). For instance, to set the corner frequency of the DLPF of the accelerometer to 10.2 Hz, write 0x05 into ACCEL_CONFIG2.

To set the corner frequency of the DLPF of the gyroscope, set the register CONFIG (address 0x1A) to the desired value (see section 9.10). For instance, to set the corner frequency of the DLPF of the gyroscope to 10 Hz, write 0x05 into CONFIG.

4.17.7 Power mode selection

To set desired power modes for IAM-20680HV (see section 4.16).

5 PROGRAMMABLE INTERRUPTS

The IAM-20680HV has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

INTERRUPT NAME	MODULE
Motion Detection	Motion
Data Ready	Sensor Registers

Table 13. Table of Interrupt Sources

5.1 WAKE-ON-MOTION INTERRUPT

The IAM-20680HV provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt to raise an interrupt when motion is detected on any accelerometer axis.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = b111

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_X/Y/Z_INT_EN = b1 to enable motion interrupt on any axis

Once triggered, WOM interrupt is generated on INT pin (if INT2_EN bit is set to 0) or on INT2 pin (if INT2_EN is set to 1).

Step 4: Set Motion Threshold

- Set the motion threshold in ACCEL_WOM_X/Y/Z_THR register (0x20, 0x21, 0x22)

Step 5: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = 1 to enable the Wake-on-Motion detection logic
- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_MODE = 1 to make the detection insensitive to the acceleration DC-component
- In ACCEL_INTEL_CTRL register (0x69) ensure that bit 0 is set to 0.

Step 6: Set Accelerometer WoM ODR Selection

- In LP_MODE_CFG register (0x1E) set ACCEL_WOM_ODR_CTRL[3:0] according to Table 19

Step 7: Enable Cycle Mode (Accelerometer WoM Mode)

- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1
- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 1

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the IAM-20680HV can be accessed using either I²C at 400 kHz or SPI at 8 MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage.
4	SA0 / SDO	I²C Slave Address LSB (SA0); SPI serial data output (SDO)
2	SCL / SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

Table 14. Serial Interface

Note: To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in section 3.3.2.

For further information regarding the I2C_IF_DIS bit, please refer to sections 8 and 9 of this document.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IAM-20680HV always operates as a slave device when communicating to the system processor, which acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the IAM-20680HV is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin SA0. This allows two IAM-20680HVs to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

6.2.1 IC Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see Figure 8).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

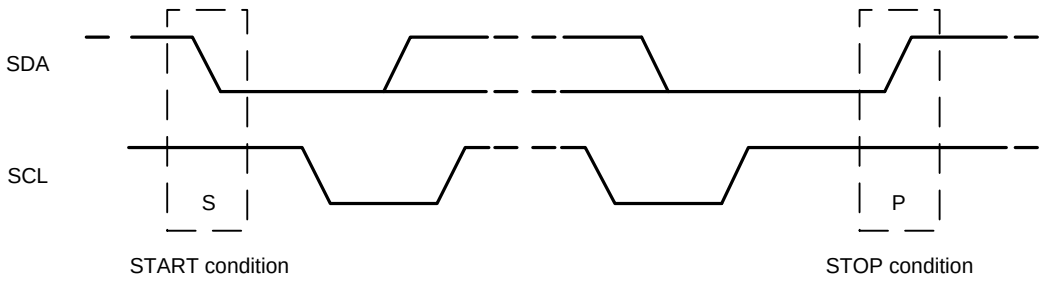


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to Figure 9).

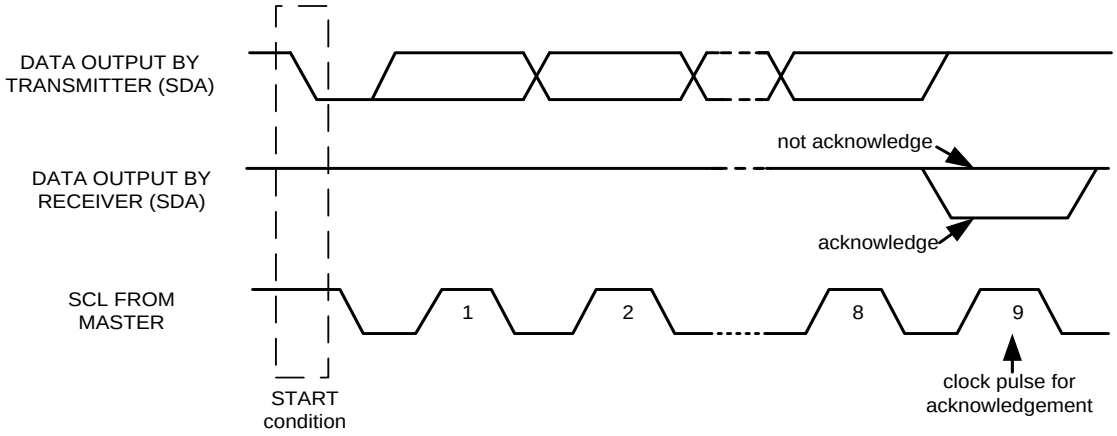


Figure 9. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

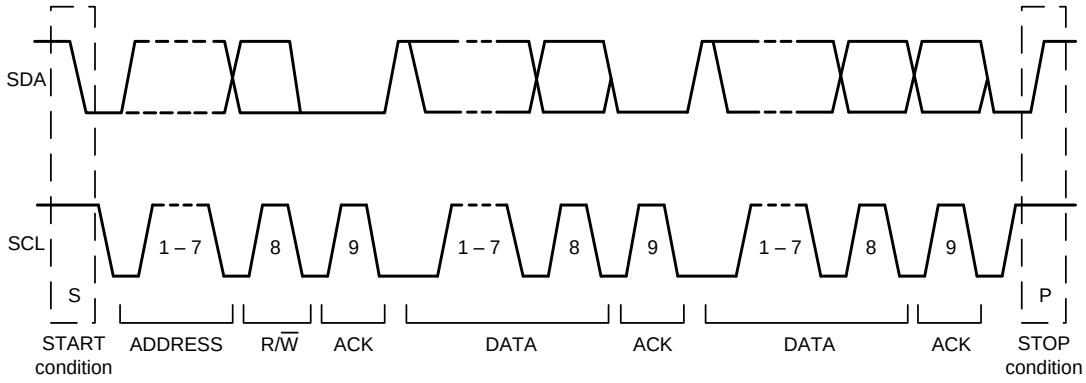


Figure 10. Complete I²C Data Transfer

To write the internal IAM-20680HV registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the IAM-20680HV acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IAM-20680HV acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IAM-20680HV automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal IAM-20680HV registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IAM-20680HV, the master transmits a start signal followed by the slave address and read bit. As a result, the IAM-20680HV sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.2.2 I^2C Terms

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	IAM-20680HV internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 15. I^2C Terms

6.3 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The IAM-20680HV always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SPC), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data are delivered MSB first and LSB last
2. Data are latched on the rising edge of SPC
3. Data should be transitioned on the falling edge of SPC
4. The maximum frequency of SPC is 8 MHz

5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data are two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

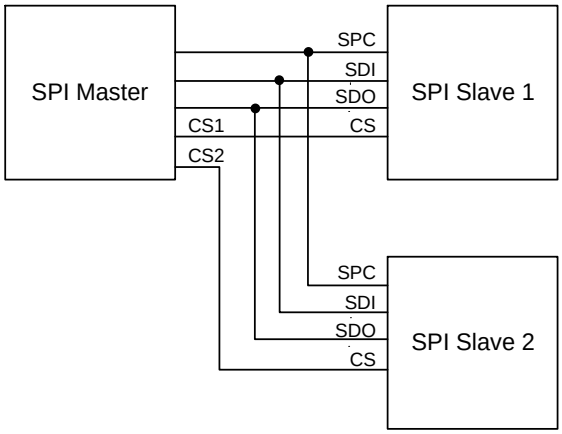


Figure 11. Typical SPI Master/Slave Configuration

7 SERIAL INTERFACE CONSIDERATIONS

7.1 IAM-20680HV SUPPORTED INTERFACES

The IAM-20680HV supports I^2C communications on its serial interface.

The IAM-20680HV's I/O logic levels are set to be VDDIO.

Figure 12 depicts a sample circuit of IAM-20680HV. It shows the relevant logic levels and voltage connections.

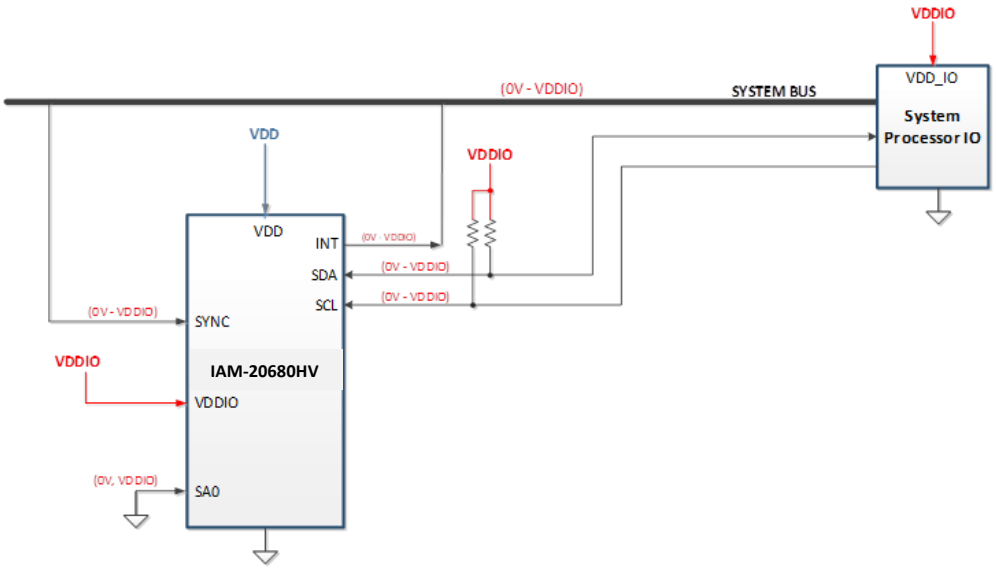


Figure 12. I/O Levels and Connections

8 REGISTER MAP

The following table lists the register map for the IAM-20680HV.

Addr (Hex)	Addr (Dec)	Register Name	Serial I/F	Accessible (writable) in Sleep Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	SELF_TEST_X_GYRO	R/W	N	XG_ST_DATA[7:0]							
1	1	SELF_TEST_Y_GYRO	R/W	N	YG_ST_DATA[7:0]							
2	2	SELF_TEST_Z_GYRO	R/W	N	ZG_ST_DATA[7:0]							
0D	13	SELF_TEST_X_ACCEL	R/W	N	XA_ST_DATA[7:0]							
0E	14	SELF_TEST_Y_ACCEL	R/W	N	YA_ST_DATA[7:0]							
0F	15	SELF_TEST_Z_ACCEL	R/W	N	ZA_ST_DATA[7:0]							
13	19	XG_OFFS_USRH	R/W	N	X_OFFS_USR [15:8]							
14	20	XG_OFFS_USRL	R/W	N	X_OFFS_USR [7:0]							
15	21	YG_OFFS_USRH	R/W	N	Y_OFFS_USR [15:8]							
16	22	YG_OFFS_USRL	R/W	N	Y_OFFS_USR [7:0]							
17	23	ZG_OFFS_USRH	R/W	N	Z_OFFS_USR [15:8]							
18	24	ZG_OFFS_USRL	R/W	N	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	R/W	N	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	N	-		-		EXT_SYNC_SET[2:0]		DLPF_CFG[2:0]	
1B	27	GYRO_CONFIG	R/W	N	XG_ST	YG_ST	ZG_ST		FS_SEL [1:0]		-	FCHOICE_B[1:0]
1C	28	ACCEL_CONFIG	R/W	N	XA_ST	YA_ST	ZA_ST	ACCEL_FS_SEL[1:0]		-	-	-
1D	29	ACCEL_CONFIG 2	R/W	N	-		-	DEC2_CFG[1:0]		ACCEL_FCHOICE_B		A_DLPF_CFG[2:0]
1E	30	LP_MODE_CFG	R/W	N	GYRO_CYCLE			G_AVGCFG[2:0]			ACCEL_WOM_ODR_CTRL [3:0]	
20	32	ACCEL WOM_X_THR	R/W	N	WOM_X_THRESHOLD[7:0]							
21	33	ACCEL WOM_Y_THR	R/W	N	WOM_Y_THRESHOLD[7:0]							
22	34	ACCEL WOM_Z_THR	R/W	N	WOM_Z_THRESHOLD[7:0]							
36	54	FSYNC_INT	R/C	N	FSYNC_INT	-	-	-	-	-	-	-
37	55	INT_PIN_CFG	R/W	Y	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	FSYNC_INT_LEVEL	FSYNC_INT_MODE_EN	-	INT2_EN
38	56	INT_ENABLE	R/W	Y	WOM_X_INT_EN	WOM_Y_INT_EN	WOM_Z_INT_EN	-	-	GDRIVE_INT_EN	-	DATA_RDY_INT_EN
3A	58	INT_STATUS	R/C	N	WOM_X_INT	WOM_Y_INT	WOM_Z_INT	-	-	GDRIVE_INT	-	DATA_RDY_INT
3B	59	ACCEL_XOUT_H	R	N	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	R	N	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	R	N	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	R	N	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	R	N	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	R	N	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	R	N	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	N	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	R	N	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	N	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	N	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	N	GYRO_YOUT[7:0]							

Addr (Hex)	Addr (Dec)	Register Name	Serial I/F	Accessible (writable) in Sleep Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
47	71	GYRO_ZOUT_H	R	N	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	R	N	GYRO_ZOUT[7:0]							
68	104	SIGNAL_PATH_RESET	R/W	N	-	-	-	-	-	-	ACCEL_RST	TEMP_RST
69	105	ACCEL_INTEL_CTRL	R/W	N	ACCEL_INTEL_EN	ACCEL_INTEL_MODE	-	-	-	-	-	-
6A	106	USER_CTRL	R/W	N	-	-	-	I2C_IF_DIS	-	-	-	SIG_COND_RST
6B	107	PWR_MGMT_1	R/W	Y	DEVICE_RESET	SLEEP	ACCEL_CYCLE		GYRO_STANDBY	TEMP_DIS		CLKSEL[2:0]
6C	108	PWR_MGMT_2	R/W	Y	-	-	STBY_XA	STBY_YA	STBY_ZA	STBY_XG	STBY_YG	STBY_ZG
75	117	WHO_AM_I	R	N	WHOAMI[7:0]							
77	119	XA_OFFSET_H	R/W	N	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	R/W	N	XA_OFFS [6:0]				-			
7A	122	YA_OFFSET_H	R/W	N	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	R/W	N	YA_OFFS [6:0]				-			
7D	125	ZA_OFFSET_H	R/W	N	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	R/W	N	ZA_OFFS [6:0]				-			

Table 16. Register Map

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below:

- Self-test registers 0, 1, 2, 13, 14, 15 contain pre-programmed values
- Register 107, PWR_MGMT_1 = 0x01
- Register 117, WHO_AM_I: (default value is reported in section 9.28)
- Registers 119, 120, 122, 123, 125, 126 contain pre-programmed offset cancellation values

9 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the IAM-20680HV.

Note: The device will come up in 6-Axis Low-Noise Mode upon power-up.

9.1 REGISTERS 0 TO 2 – GYROSCOPE SELF-TEST REGISTERS

Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO

Type: READ/WRITE

Register Address: 00, 01, 02 (Decimal); 00, 01, 02 (Hex)

REGISTER	BIT	NAME	FUNCTION
SELF_TEST_X_GYRO	[7:0]	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_GYRO	[7:0]	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_GYRO	[7:0]	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620 / 2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round(\frac{\log(ST\_FAC / (2620 / 2^{FS}))}{\log(1.01)}) + 1$$

9.2 REGISTERS 13 TO 15 – ACCELEROMETER SELF-TEST REGISTERS

Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL

Type: READ/WRITE

Register Address: 13, 14, 15 (Decimal); 0D, 0E, 0F (Hex)

REGISTER	BITS	NAME	FUNCTION
SELF_TEST_X_ACCEL	[7:0]	XA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_ACCEL	[7:0]	YA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_ACCEL	[7:0]	ZA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620 / 2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round(\frac{\log(ST\_FAC / (2620 / 2^{FS}))}{\log(1.01)}) + 1$$

9.3 REGISTER 19 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 19 (Decimal); 13 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.4 REGISTER 20 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 20 (Decimal); 14 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.5 REGISTER 21 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 21 (Decimal); 15 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.6 REGISTER 22 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 22 (Decimal); 16 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.7 REGISTER 23 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 23 (Decimal); 17 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.8 REGISTER 24 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 24 (Decimal); 18 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.9 REGISTER 25 – SAMPLE RATE DIVIDER

Register Name: SMPLRT_DIV

Register Type: READ/WRITE

Register Address: 25 (Decimal); 19 (Hex)

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate. **Note**: This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7). This is the update rate of the sensor register: SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV) Where INTERNAL_SAMPLE_RATE = 1 kHz

9.10 REGISTER 26 – CONFIGURATION

Register Name: CONFIG

Register Type: READ/WRITE

Register Address: 26 (Decimal); 1A (Hex)

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>[7]</td><td>-</td><td>Always set to 0</td></tr>
<tr><td>[6]</td><td>-</td><td>Reserved</td></tr>
<tr><td>[5:3]</td><td>EXT_SYNC_SET[2:0]</td><td>Enables the FSYNC pin data to be sampled.
<table>
<tr><th>EXT_SYNC_SET</th><th>FSYNC bit location</th></tr>
<tr><td>0</td><td>function disabled</td></tr>
<tr><td>1</td><td>TEMP_OUT_L[0]</td></tr>
<tr><td>2</td><td>GYRO_XOUT_L[0]</td></tr>
<tr><td>3</td><td>GYRO_YOUT_L[0]</td></tr>
<tr><td>4</td><td>GYRO_ZOUT_L[0]</td></tr>
<tr><td>5</td><td>ACCEL_XOUT_L[0]</td></tr>
<tr><td>6</td><td>ACCEL_YOUT_L[0]</td></tr>
<tr><td>7</td><td>ACCEL_ZOUT_L[0]</td></tr>
</table>
FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.</td></tr>
<tr><td>[2:0]</td><td>DLPF_CFG[2:0]</td><td>For the DLPF to be used, FCHOICE_B[1:0] is 2'b00.
See Table 17.</td></tr>
</table>

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in Table 17.

FCHOICE_B		DLPF_CFG	Gyroscope			Temperature Sensor
<1>	<0>		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)	3-dB BW (Hz)
X	1	X	8173	8595.1	32	4000
1	0	X	3281	3451.0	32	4000
0	0	0	250	306.6	8	4000
0	0	1	176	177.0	1	188
0	0	2	92	108.6	1	98
0	0	3	41	59.0	1	42
0	0	4	20	30.5	1	20
0	0	5	10	15.6	1	10
0	0	6	5	8.0	1	5
0	0	7	3281	3451.0	8	4000

Table 17. Gyroscope and Temperature Sensor Data Rates and Bandwidths (Low-Noise Mode)

9.11 REGISTER 27 – GYROSCOPE CONFIGURATION

Register Name: GYRO_CONFIG

Register Type: READ/WRITE

Register Address: 27 (Decimal); 1B (Hex)

BIT	NAME	FUNCTION
[7]	XG_ST	X Gyro self-test
[6]	YG_ST	Y Gyro self-test
[5]	ZG_ST	Z Gyro self-test
[4:3]	FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±125 dps 01= ±250 dps 10 = ±500 dps 11 = ±1000 dps
[2]	-	Reserved
[1:0]	FCHOICE_B[1:0]	Used to bypass DLPF as shown in Table 17 above.

9.12 REGISTER 28 – ACCELEROMETER CONFIGURATION

Register Name: ACCEL_CONFIG

Register Type: READ/WRITE

Register Address: 28 (Decimal); 1C (Hex)

BIT	NAME	FUNCTION
[7]	XA_ST	X Accel self-test
[6]	YA_ST	Y Accel self-test
[5]	ZA_ST	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	-	Reserved

9.13 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

Register Name: ACCEL_CONFIG2

Register Type: READ/WRITE

Register Address: 29 (Decimal); 1D (Hex)

BIT	NAME	FUNCTION
[7:6]	-	-
[5:4]	DEC2_CFG[1:0]	Averaging filter settings for WoM Accelerometer Mode: 0 = Average 4 samples 1 = Average 8 samples 2 = Average 16 samples 3 = Average 32 samples
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in the table below.
[2:0]	A_DLPF_CFG	Accelerometer low pass filter setting as shown in Table 18.

ACCEL_FCHOICE_B	A_DLPF_CFG	Accelerometer		
		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)
1	X	1046.0	1100.0	4
0	0	218.1	235.0	1
0	1	218.1	235.0	1
0	2	99.0	121.3	1
0	3	44.8	61.5	1
0	4	21.2	31.0	1
0	5	10.2	15.5	1
0	6	5.1	7.8	1
0	7	420.0	441.6	1

Table 18. Accelerometer Data Rates and Bandwidths (Low-Noise Mode)

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the Low-Noise mode in this manner (Hz): 3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K.

The Table 19 lists the accelerometer filter bandwidths and noise available in the WoM mode of operation. In the WoM mode of operation, the accelerometer is duty-cycled.

To operate in accelerometer WoM mode, gyroscope must be off and ACCEL_CYCLE must be set to ‘1’ in PWR_MGMT_1 (address 0x6B).

ACCEL_FCHOICE_B		1	0	0	0	0
A_DLPF_CFG		x	7	7	7	7
DEC2_CFG		x	0	1	2	3
Averages		1x	4x	8x	16x	32x
Ton (ms)		1.084	1.84	2.84	4.84	8.84
Noise BW (Hz)		1100.0	441.6	235.4	121.3	61.5
Noise (mg rms) TYP [1] Based on 250 µg/√Hz		8.3	5.3	3.8	2.8	2.0
ACCEL_WOM_ODR_CTRL	ODR (Hz)	Current Consumption (µA) TYP [1]				
4	3.9	8.4	9.4	10.8	13.6	19.2
5	7.8	9.8	11.9	14.7	20.3	31.4
6	15.6	12.8	17.0	22.5	33.7	55.9
7	31.3	18.7	27.1	38.2	60.4	104.9
8	62.5	30.4	47.2	69.4	113.9	202.8
9	125.0	57.4	87.5	132.0	220.9	N/A
10	250.0	100.9	168.1	257.0	N/A	
11	500.0	194.9	329.3	N/A		

Table 19. Example Configurations for Accelerometer WoM Mode

Notes:
1. Not tested in production, not guaranteed

9.14 REGISTER 30 – LOW POWER MODE CONFIGURATION

Register Name: LP_MODE_CFG

Register Type: READ/WRITE

Register Address: 30 (Decimal); 1E (Hex)

BIT	NAME	FUNCTION
[7]	GYRO_CYCLE [1]	When set to ‘1’ gyroscope or 6-axis are duty-cycled. Default setting is ‘0’
[6:4]	G_AVGCFG[2:0]	Gyroscope averaging filter settings when GYRO_CYCLE is set to ‘1’. Default setting is ‘000’
[3:0]	ACCEL_WOM_ODR_CTRL[3:0]	Accelerometer WoM Mode ODR configuration. ACCEL_WOM_ODR_CTRL is effective only when GYRO is off and ACCEL_CYCLE is set to ‘1’: 0 to 3 = RESERVED 4 = 3.9 Hz 5 = 7.8 Hz 6 = 15.6 Hz 7 = 31.3 Hz 8 = 62.5 Hz 9 = 125 Hz 10 = 250 Hz 11 = 500 Hz 12 to 15 = RESERVED

Notes:
1. Not tested in production, not guaranteed

To reduce gyroscope or 6-axis power consumption, GYRO_CYCLE should be set to ‘1'. When GYRO_CYCLE is set to '1' gyroscope is duty-cycled and performance are reduced compared to Low-Noise mode. When GYRO_CYCLE is set to '1' gyroscope filter configuration is determined by G_AVGCFG[2:0] that sets the averaging filter configuration, gyroscope filter is not dependent on DLPF_CFG[2:0]. Table 20 shows some example configurations when GYRO_CYCLE is set to '1'.

FCHOICE_B		0	0	0	0	0	0	0	0
G_AVGCFG		0	1	2	3	4	5	6	7
Averages		1x	2x	4x	8x	16x	32x	64x	128x
Ton (ms)		1.73	2.23	3.23	5.23	9.23	17.23	33.23	65.23
Noise BW (Hz)		650.8	407.1	224.2	117.4	60.2	30.6	15.6	8.0
Noise (dps rms) TYP [1] Based on 0.008 dps/√Hz		0.20	0.16	0.12	0.09	0.06	0.04	0.03	0.02
SMPLRT_DIV	ODR (Hz)	Current Consumption (mA) TYP [1]							
255	3.9	1.3	1.3	1.3	1.3	1.4	1.4	1.5	1.8
99	10.0	1.3	1.3	1.4	1.4	1.5	1.6	1.9	2.5
64	15.4	1.4	1.4	1.4	1.5	1.6	1.8	2.2	N/A
32	30.3	1.4	1.4	1.5	1.6	1.8	2.2	N/A	
19	50.0	1.5	1.5	1.6	1.8	2.1	2.8		
9	100.0	1.6	1.7	1.9	2.2	3.0	N/A		
7	125.0	1.7	1.8	2.0	2.5	N/A			
4	200.0	1.9	2.1	2.5	N/A				
3	250.0	2.1	2.3	2.7					
2	333.3	2.3	2.6	N/A					
1	500.0	2.9	N/A						

Table 20. Example Configurations for Gyroscope when GYRO_CYCLE = 1

Notes:

1. Not tested in production, not guaranteed

9.15 REGISTER 32 TO 34 – WAKE-ON MOTION THRESHOLDS (ACCELEROMETER)

Register Name: ACCEL_WOM_X_THR

Register Type: READ/WRITE

Register Address: 32 (Decimal); 20 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_X_THRESHOLD[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for x-axis accelerometer. Wake on motion threshold resolution is 4 mg/LSB regardless the selected full scale.

Register Name: ACCEL_WOM_Y_THR

Register Type: READ/WRITE

Register Address: 33 (Decimal); 21 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_Y_THRESHOLD[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for y-axis accelerometer. Wake on motion threshold resolution is 4 mg/LSB regardless the selected full scale.

Register Name: ACCEL_WOM_Z_THR

Register Type: READ/WRITE

Register Address: 34 (Decimal); 22 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_Z_THRESHOLD[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for z-axis accelerometer. Wake on motion threshold resolution is 4 mg/LSB regardless the selected full scale.

9.16 REGISTER 54 – FSYNC INTERRUPT STATUS

Register Name: FSYNC_INT

Register Type: READ to CLEAR

Register Address: 54 (Decimal); 36 (Hex)

BIT	NAME	FUNCTION
[7]	FSYNC_INT	This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read.

9.17 REGISTER 55 – INT/INT2 PIN / BYPASS ENABLE CONFIGURATION

Register Name: INT_PIN_CFG

Register Type: READ/WRITE

Register Address: 55 (Decimal); 37 (Hex)

BIT	NAME	FUNCTION
[7]	INT_LEVEL	1 – The logic level for INT/INT2 pin is active low. 0 – The logic level for INT/INT2 pin is active high.
[6]	INT_OPEN	1 – INT/INT2 pin is configured as open drain. 0 – INT/INT2 pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT/INT2 pin level held until interrupt status is cleared. 0 – INT/INT2 pin indicates interrupt pulse's width is 50 µs.
[4]	INT_RD_CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
[3]	FSYNC_INT_LEVEL	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by *FSYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.
[1]	-	Reserved.
[0]	-INT2_EN	When INT2_EN = 0, all of the interrupts appear on the INT pin, and INT2 interrupt pin is unused. When INT2_EN = 1, all interrupts except for data ready appear on the INT2 pin, and data ready interrupt appears on the INT interrupt pin.

9.18 REGISTER 56 – INTERRUPT ENABLE

Register Name: INT_ENABLE

Register Type: READ/WRITE

Register Address: 56 (Decimal); 38 (Hex)

BIT	NAME	FUNCTION
[7]	WOM_X_INT_EN	1 – Enable WoM interrupt on X accelerometer. 0 – Disable WoM interrupt on X accelerometer.
[6]	WOM_Y_INT_EN	1 – Enable WoM interrupt on Y accelerometer. 0 – Disable WoM interrupt on Y accelerometer.
[5]	WOM_Z_INT_EN	1 – Enable WoM interrupt on Z accelerometer. 0 – Disable WoM interrupt on Z accelerometer.
[4:3]	-	Reserved.
[2]	GDRIVE_INT_EN	Gyroscope Drive System Ready interrupt enable.
[1]	-	Reserved.
[0]	DATA_RDY_INT_EN	Data ready interrupt enable.

Data ready interrupt is always generated on INT pin. All the other interrupts signals are generated on INT pin if INT2_EN bit is set to 0 or on INT2 pin if INT2_EN bit is set to 1.

9.19 REGISTER 58 – INTERRUPT STATUS

Register Name: INT_STATUS

Register Type: READ to CLEAR

Register Address: 58 (Decimal); 3A (Hex)

BIT	NAME	FUNCTION
[7]	WOM_X_INT	Accelerometer X, WoM interrupt status. Cleared on Read. 1 – WOM detected
[6]	WOM_Y_INT	Accelerometer Y, WoM interrupt status. Cleared on Read. 1 – WOM detected
[5]	WOM_Z_INT	Accelerometer Z, WoM interrupt status. Cleared on Read. 1 – WOM detected
[4:3]	-	Reserved.
[2]	GDRIVE_INT	Gyroscope Drive System Ready interrupt
[1]	-	Reserved.
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

9.20 REGISTERS 59 TO 64 – ACCELEROMETER MEASUREMENTS

Register Name: ACCEL_XOUT_H

Register Type: READ only

Register Address: 59 (Decimal); 3B (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_H[15:8]	High byte of accelerometer x-axis data.

Register Name: ACCEL_XOUT_L

Register Type: READ only

Register Address: 60 (Decimal); 3C (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_L[7:0]	Low byte of accelerometer x-axis data.

Register Name: ACCEL_YOUT_H

Register Type: READ only

Register Address: 61 (Decimal); 3D (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_H[15:8]	High byte of accelerometer y-axis data.

Register Name: ACCEL_YOUT_L

Register Type: READ only

Register Address: 62 (Decimal); 3E (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_L[7:0]	Low byte of accelerometer y-axis data.

Register Name: ACCEL_ZOUT_H

Register Type: READ only

Register Address: 63 (Decimal); 3F (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_H[15:8]	High byte of accelerometer z-axis data.

Register Name: ACCEL_ZOUT_L

Register Type: READ only

Register Address: 64 (Decimal); 40 (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_L[7:0]	Low byte of accelerometer z-axis data.

9.21 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

Register Name: TEMP_OUT_H

Register Type: READ only

Register Address: 65 (Decimal); 41 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[15:8]	High byte of the temperature sensor output.

Register Name: TEMP_OUT_L

Register Type: READ only

Register Address: 66 (Decimal); 42 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[7:0]	Low byte of the temperature sensor output TEMP [°C] = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25°C

9.22 REGISTERS 67 TO 72 – GYROSCOPE MEASUREMENTS

Register Name: GYRO_XOUT_H

Register Type: READ only

Register Address: 67 (Decimal); 43 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[15:8]	High byte of the X-Axis gyroscope output.

Register Name: GYRO_XOUT_L

Register Type: READ only

Register Address: 68 (Decimal); 44 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[7:0]	Low byte of the X-Axis gyroscope output. **GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps)

Register Name: GYRO_YOUT_H

Register Type: READ only

Register Address: 69 (Decimal); 45 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[15:8]	High byte of the Y-Axis gyroscope output.

Register Name: GYRO_YOUT_L

Register Type: READ only

Register Address: 70 (Decimal); 46 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[7:0]	Low byte of the Y-Axis gyroscope output. **GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps)

Register Name: GYRO_ZOUT_H

Register Type: READ only

Register Address: 71 (Decimal); 47 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[15:8]	High byte of the Z-Axis gyroscope output.

Register Name: GYRO_ZOUT_L

Register Type: READ only

Register Address: 72 (Decimal); 48 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[7:0]	Low byte of the Z-Axis gyroscope output. **GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps)

9.23 REGISTER 104 – SIGNAL PATH RESET

Register Name: SIGNAL_PATH_RESET

Register Type: READ/WRITE

Register Address: 104 (Decimal); 68 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved.
[1]	ACCEL_RST	Reset accel digital signal path. **Note**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. **Note**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

9.24 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

Register Name: ACCEL_INTEL_CTRL

Register Type: READ/WRITE

Register Address: 105 (Decimal); 69 (Hex)

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic.
[6]	ACCEL_INTEL_MODE	0 – Compares the current sample to the first sample taken when entering in WoM mode. 1 – Compare the current sample with the previous sample.
[5:1]	-	Reserved.
[0]	-	Reserved, must be set to 0 when WoM is activated. Please refer to section 5.1

9.25 REGISTER 106 – USER CONTROL

Register Name: USER_CTRL

Register Type: READ/WRITE

Register Address: 106 (Decimal); 6A (Hex)

BIT	NAME	FUNCTION
[7:5]	-	Reserved.
[4]	I2C_IF_DIS	1 – Disable I^2C Slave module and put the serial interface in SPI mode only.
[3:1]	-	Reserved.
[0]	SIG_COND_RST	1 – Reset all gyro digital signal path, accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

9.26 REGISTER 107 – POWER MANAGEMENT 1

Register Name: PWR_MGMT_1

Register Type: READ/WRITE

Register Address: 107 (Decimal); 6B (Hex)

BIT	NAME	FUNCTION
[7]	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done.
[6]	SLEEP	When set to 1, the chip is set to sleep mode. Default setting is 0.
[5]	ACCEL_CYCLE	When set to 1, and SLEEP and STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample. **Note**: When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	GYRO_STANDBY	When set, the gyro drive and PLL circuitry are enabled, but the sense paths are disabled. This is a power mode that allows quick enabling of the gyros.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.

BIT	NAME	FUNCTION
[2:0]	CLKSEL[2:0]	Code / Clock Source 0 – Internal 20 MHz oscillator. 1 – Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 2 – Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 3 – Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 4 – Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 5 – Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 – Internal 20 MHz oscillator. 7 – Stops the clock and keeps timing generator in reset.

Note: The default value of CLKSEL[2:0] is 001.

9.27 REGISTER 108 – POWER MANAGEMENT 2

Register Name: PWR_MGMT_2

Register Type: READ/WRITE

Register Address: 108 (Decimal); 6C (Hex)

BIT	NAME	FUNCTION
[7:6]	-	Reserved.
[5]	STBY_XA	1 – X accelerometer is disabled. 0 – X accelerometer is on.
[4]	STBY_YA	1 – Y accelerometer is disabled. 0 – Y accelerometer is on.
[3]	STBY_ZA	1 – Z accelerometer is disabled. 0 – Z accelerometer is on.
[2]	STBY_XG	1 – X gyro is disabled. 0 – X gyro is on.
[1]	STBY_YG	1 – Y gyro is disabled. 0 – Y gyro is on.
[0]	STBY_ZG	1 – Z gyro is disabled. 0 – Z gyro is on.

9.28 REGISTER 117 – WHO AM I

Register Name: WHO_AM_I

Register Type: READ only

Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	WHOAMI	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0xFE. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the IAM-20680HV is 0x68 or 0x69 depending upon the value driven on AD0 pin.

9.29 REGISTERS 119, 120, 122, 123, 125, 126 ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H

Register Type: READ/WRITE

Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the X accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: XA_OFFSET_L

Register Type: READ/WRITE

Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the X accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved. This bit is set during factory calibration and the value must be kept unchanged.

Register Name: YA_OFFSET_H

Register Type: READ/WRITE

Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the Y accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: YA_OFFSET_L

Register Type: READ/WRITE

Register Address: 123 (Decimal); 7B (Hex)

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the Y accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved. This bit is set during factory calibration and the value must be kept unchanged.

Register Name: ZA_OFFSET_H

Register Type: READ/WRITE

Register Address: 125 (Decimal); 7D (Hex)

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the Z accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: ZA_OFFSET_L

Register Type: READ/WRITE

Register Address: 126 (Decimal); 7E (Hex)

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the Z accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved. This bit is set during factory calibration and the value must be kept unchanged.

10 ASSEMBLY

This section provides general guidelines for assembling TDK-InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

10.1 ORIENTATION OF AXES

Figure 13 below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

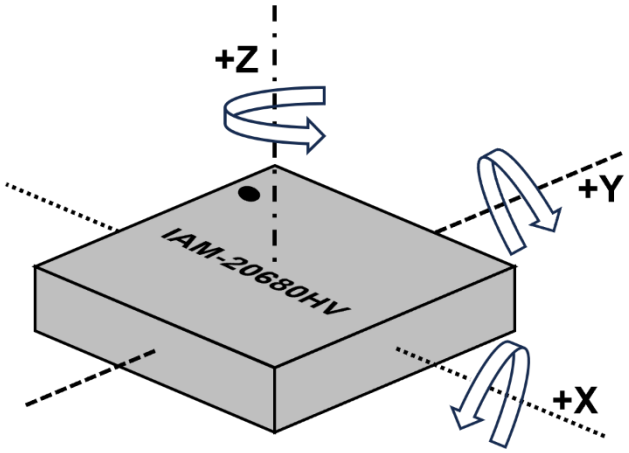


Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

10.2 PACKAGE DIMENSIONS

16 Lead LGA 3x3x0.75 mm^3 NiAu pad finish.

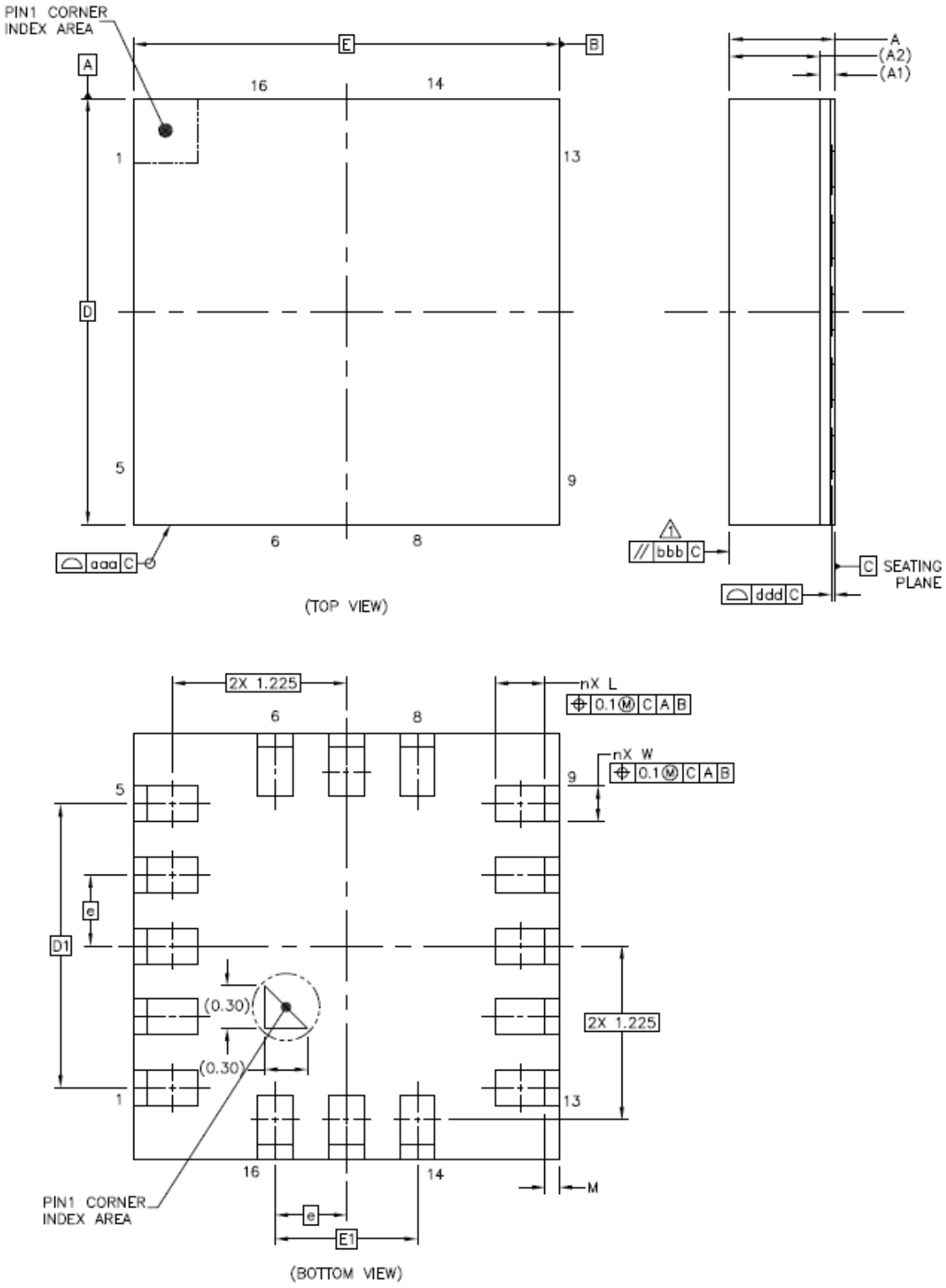


Figure 14. Package Dimensions

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.7	0.75	0.8
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.63	REF
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.3	0.35	0.4
Lead Pitch	e		0.5	BSC
Lead Count	n		16	
Edge Ball Center to Center	D1		2	BSC
	E1		1	BSC
Body Center to Contact Ball	SD		---	BSC
	SE		---	BSC
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Lead Edge to Package Edge	M	0.05	0.1	0.15

Table 21. Package Dimensions

11 PART NUMBER PACKAGE MARKING

The part number package marking for IAM-20680HV devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
IAM-20680HV	IA268HV

Table 22. Part Number Package Marking

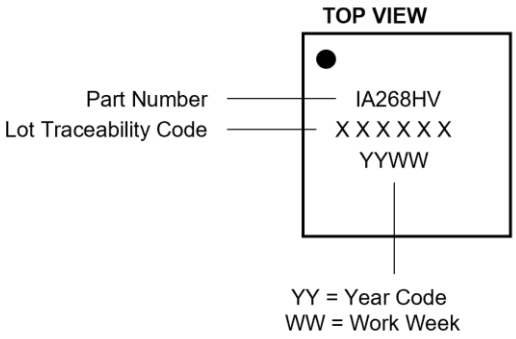


Figure 15. Part Number Package Marking

Samples with Part Number Package Marking “IA268HV E” are engineering samples and may have deviations in respect to the specifications and functions reported in the datasheet. Engineering samples are not production-intent parts.

12 REFERENCE

Please refer to “IMU PCB Design and MEMS Assembly Guidelines for ICM/IAM/IIM-4xxxx, 2xxxx and MPU-6xxx Products” (AN-000393) for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

13 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
02/26/2025	1.0	Initial revision

This information furnished by InvenSense or its affiliates (“TDK InvenSense”) is believed to be accurate and reliable. However, no responsibility is assumed by TDK InvenSense for its use, or for any infringements of patents or other rights of third parties that may result from its use. Specifications are subject to change without notice. TDK InvenSense reserves the right to make changes to this product, including its circuits and software, in order to improve its design and/or performance, without prior notice. TDK InvenSense makes no warranties, neither expressed nor implied, regarding the information and specifications contained in this document. TDK InvenSense assumes no responsibility for any claims or damages arising from information contained in this document, or from the use of products and services detailed therein. This includes, but is not limited to, claims or damages based on the infringement of patents, copyrights, mask work and/or other intellectual property rights.

Certain intellectual property owned by InvenSense and described in this document is patent protected. No license is granted by implication or otherwise under any patent or patent rights of InvenSense. This publication supersedes and replaces all information previously supplied. Trademarks that are registered trademarks are the property of their respective companies. TDK InvenSense sensors should not be used or sold in the development, storage, production or utilization of any conventional or mass-destructive weapons or for any other weapons or life threatening applications, as well as in any other life critical applications such as medical equipment, transportation, aerospace and nuclear instruments, undersea equipment, power plant equipment, disaster prevention and crime prevention equipment.

©2024 InvenSense. All rights reserved. InvenSense, SmartMotion, SmartIndustrial, SmartSonic, SmartAutomotive, SmartRobotics, SmartSound, SmartPressure, MotionProcessing, MotionProcessor, UltraPrint, MotionTracking, CHIRP Microsystems, SmartBug, SonicLink, Digital Motion Processor, AAR, and the InvenSense logo are registered trademarks of InvenSense, Inc. The TDK logo is a trademark of TDK Corporation. Other company and product names may be trademarks of the respective companies with which they are associated.

©2024 InvenSense. All rights reserved.