IAM-20680xx - WoM User Guide

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1 PURPOSE AND SCOPE

An application of TDK-InvenSense motion sensors is motion detection for low power operation of applications processor. The products of the IAM-20680xx 6-Axes family have a programmable interrupt system which can generate an interrupt signal on the INT pin (or on INT2 pin, where available). One of the interrupts provides motion detection capability, Wake-on-Motion (WoM).
This document will explain the details on how to use WoM with IAM-20680xx and supplement to the WoM functions to provide the base understanding that customers need.

2 WHY USING WAKE-ON-MOTION

WoM detects motion when accelerometer data exceeds a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
For example, a possible Automotive application (*theft-attempt detection*) is represented in Figure 1. When the car is parked, host processor generally wants to enter standby mode to save power consumption. In case of a theft attempt, car might be lifted, thus inducing an acceleration on any of the IMU axes. As a wake-event, if an acceleration is detected compared to any time frame, then IMU asserts interruption signal from INT pin as an event. By receiving the signal, HOST can be enabled and then can read IMU information or other processing can be implemented.

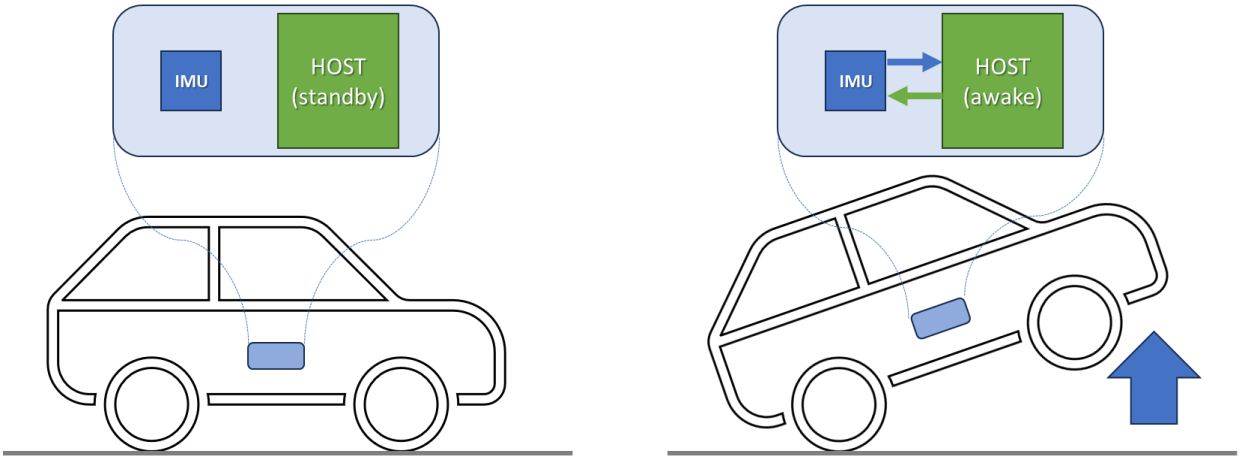

Figure 1. WOM mode for anti-theft application

2.1. DETECTION AXES AND AVAILABLE INTERRUPT PINS

Depending on the Motion Sensor product in use, WoM interrupt can be generated by detecting motion on different axes:

- ***any-axis WoM***: interrupt is generated when motion is detected on any axis, with the same trigger threshold on all axes.
- ***per-axis WoM***: interrupt is generated by motion detected on a specific axis, with a dedicated threshold.

Once WoM event is detected (in either of the two ways above), the interrupt signal can be generated on different pin, according to the configurability of the specific device.

Device	Any-axis WoM	Per-axis WoM	INT pin available for WoM interrupt
IAM-20381HT	Y	N	INT or INT2
IAM-20680HT	Y	N	INT or INT2
IAM-20680HP	Y	N	INT
IAM-20680HV	N	Y	INT or INT2

Table 1. WoM strategy per device

3 WAKE-ON-MOTION ENABLE SEQUENCE

This section describes the necessary steps to enable WOM functionality in IAM-20x80xx products. For details concerning the typical application schematic and necessary components, please refer to the product datasheet.

3.1. ANY-AXIS MODE

Step 1: Initialize all configurations

- In PWR_MGMT_1 register (0x6B) set DEVICE_RESET = 1 (the bit will reset to 0 automatically)

Step 2: Ensure that Accelerometers, Gyroscopes and WOM function are disabled

- In PWR_MGMT_1 register (0x6B):
  - set ACCEL_CYCLE = 0
- In PWR_MGMT_2 register (0x6C):
  - set STBY_XA = STBY_YA = STBY_ZA = 1
  - set STBY_XG = STBY_YG = STBY_ZG = 1 (where available)

Step 3: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D):
  - set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = b111
  - set DEC2_CFG according to the desired averaging factor (refer to datasheet for DEC2_CFG values)

Step 4: Enable Motion Interrupt

- In INT_ENABLE register (0x38):
  - WOM_INT_EN[2:0] = b111 to enable motion interrupt

Step 5: Set Motion Threshold

- In ACCEL_WOM_THR register (0x1F) set the desired motion threshold

Step 6: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69):
  - set ACCEL_INTEL_EN = 1 to enable the Wake-on-Motion detection logic
  - choose ACCEL_INTEL_MODE = 0 or 1 to select the detection mode. (see sections 4.3.1, 4.3.2)
  - ensure bit 0 is set to 0

Step 7: Set Accelerometer WoM ODR Selection

- In LP_MODE_CFG register (0x1E) set ACCEL_WOM_ODR_CTRL[3:0] (refer to datasheet for ACCEL_WOM_ODR_CTRL values)

Step 8: Enable Accelerometers and WoM Mode

- In PWR_MGMT_2 register (0x6C):
  - STBY_XA = STBY_YA = STBY_ZA = 0
  - STBY_XG = STBY_YG = STBY_ZG = 1 (where available)
- In PWR_MGMT_1 register (0x6B):
  - ACCEL_CYCLE = 1

3.2. PER-AXIS MODE

Step 1: Initialize all configurations

- In PWR_MGMT_1 register (0x6B) set DEVICE_RESET = 1 (the bit will reset to 0 automatically)

Step 2: Ensure that Accelerometers, Gyroscopes and WOM function are disabled

- In PWR_MGMT_1 register (0x6B):
  - set ACCEL_CYCLE = 0
- In PWR_MGMT_2 register (0x6C):
  - set STBY_XA = STBY_YA = STBY_ZA = 1
  - set STBY_XG = STBY_YG = STBY_ZG = 1 (where available)

Step 3: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D):
  - set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = b111
  - set DEC2_CFG according to the desired averaging factor (refer to datasheet for DEC2_CFG values)

Step 4: Enable Motion Interrupt on the desired axes

- In INT_ENABLE register (0x38):
  - WOM_X_INT_EN motion detection on X axis - select enable or disable as required
  - WOM_Y_INT_EN motion detection on Y axis - select enable or disable as required
  - WOM_Z_INT_EN motion detection on Z axis - select enable or disable as required

Step 5: Set Motion Threshold on each axis

- In ACCEL WOM_X_THR register (0x20): set motion threshold for X axis
- In ACCEL WOM_Y_THR register (0x21): set motion threshold for Y axis
- In ACCEL WOM_Z_THR register (0x22): set motion threshold for Z axis

Step 6: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69):
  - set ACCEL_INTEL_EN = 1 to enable the Wake-on-Motion detection logic
  - choose ACCEL_INTEL_MODE = 0 or 1 to select the detection mode. (see sections 4.3.1, 4.3.2)
  - ensure bit 0 is set to 0

Step 7: Set Accelerometer WoM ODR Selection

- In LP_MODE_CFG register (0x1E) set ACCEL_WOM_ODR_CTRL[3:0] (refer to datasheet for ACCEL_WOM_ODR_CTRL values)

Step 8: Enable Accelerometers and WoM Mode

- In PWR_MGMT_2 register (0x6C):
  - STBY_XA = STBY_YA = STBY_ZA = 0
  - STBY_XG = STBY_YG = STBY_ZG = 1 (where available)
- In PWR_MGMT_1 register (0x6B):
  - ACCEL_CYCLE = 1

4 WAKE-ON-MOTION CONFIGURATION DETAILS

In this section, configuration signals are listed, and key parameters are described in detail.

4.1. SIGNALS SUMMARY

Several registers are involved in the Wake-on-Motion functionality configuration; their presence in the different product's register map, matches with the WoM detection strategy available on the specific product (ref. to section 2.1).

WoM det. strategy	Signal name	Addr	Bits	Description
Both	ACCEL_WOM_ODR_CTRL	0x1E	3:0	Accelerometer WoM Mode ODR configuration
	ACCEL_INTEL_EN	0x69	7	WoM functionality Enabling bit
	ACCEL_INTEL_MODE	0x69	6	WoM triggering mode (absolute / relative)
Any-axis	WOM_THR	0x1F	7:0	General acceleration threshold value(1)
	WOM_INT_EN	0x38	7:5	Set to 111: Enable WoM interrupt on accelerometer
	WOM_INT	0x3A	7:5	WoM interrupt status (clear on read)
Per-axis	WOM_X_THR	0x20	7:0	X-axis acceleration threshold value(1)
	WOM_Y_THR	0x21	7:0	Y-axis acceleration threshold value(1)
	WOM_Z_THR	0x22	7:0	Z-axis acceleration threshold value(1)
	WOM_X_INT_EN	0x38	7	Enable WoM interrupt on accelerometer X-axis
	WOM_Y_INT_EN	0x38	6	Enable WoM interrupt on accelerometer Y-axis
	WOM_Z_INT_EN	0x38	5	Enable WoM interrupt on accelerometer Z-axis
	WOM_X_INT	0x3A	7	WoM interrupt status (clear on read) on X-axis
	WOM_Y_INT	0x3A	6	WoM interrupt status (clear on read) on Y-axis
	WOM_Z_INT	0x3A	5	WoM interrupt status (clear on read) on Z-axis

Table 2. WoM configuration registers summary

NOTES:

(1) Resolution for threshold setting registers is **1lsb = 4mg**, regardless of the selected full-scale

4.2. WOM FLAG BITS DETAIL

The Wake-on-Motion status register information is updated on bit [7:5] at address 0x3A (INT_STATUS), both for "any-axis" and "per-axis" detection.

If WoM enable bits at address 0x38 (INT_ENABLE) are set to 1, and then a Wake-on-Motion event is detected, INT pin asserts high or low depending on address 0x37 (INT_PIN_CFG) configuration (see section 5 for details).

In "any-axis" detection mode, once Wake-on-Motion event is occurred, WOM_INT[2:0] in address 0x37 (INT_STATUS) indicates b'010 regardless which axis have detected WoM event.See below summary table to help understanding the behavior.

Also, the status register can be flagged even if the WOM_INT_EN[2:0] bit is NOT enabled (= b'000). That means the device is capable to detect and report WoM events without INT pin signal flag.

Motion on axis:	Any-Axis Mode			Per-Axis Mode		
	0x3A[7]	0x3A[6]	0x3A[5]	0x3A[7]	0x3A[6]	0x3A[5]
	WOM_INT	*WOM_INT*	*WOM_INT*	*WOM_X_INT*	*WOM_Y_INT*	*WOM_Z_INT*
X	0	**1**	0	**1**	0	0
Y	0	**1**	0	0	**1**	0
Z	0	**1**	0	0	0	**1**
X+Y	0	**1**	0	**1**	**1**	0
X+Z	0	**1**	0	**1**	0	**1**
Y+Z	0	**1**	0	0	**1**	**1**
X+Y+Z	0	**1**	0	**1**	**1**	**1**

Table 3. WOM_INT signal behavior

4.3. WOM TRIGGERING MODE SETTING BY ACCEL_INTEL_MODE

Wake-On-Motion interrupt is generated when, on any of the three axes (or, on a specific axis), the difference between measured acceleration and a reference value exceeds the threshold specified in the configuration phase. User can select between two detection modes, based on the reference value considered:

- ***Mode 0: Absolute acceleration mode*** (measured acceleration value is compared to the value sampled at the activation of WOM functionality)
- ***Mode 1: Relative acceleration mode*** (measured acceleration value sampled at instant *t* is compared to the value sampled at *t-1*)

4.3.1. Mode 0: Absolute acceleration mode

Activated by setting ACCEL_INTEL_MODE[6] = 0, in this mode the device compares the current sample to the first sample taken when entering in WoM by ACCEL_INTEL_EN = 1.
Figure 2 represents the initialization of WoM threshold in Mode 0. To re-initialize the reference accelerometer value to be compared with the current sample, it is required to repeat the enabling sequence described in section 3.

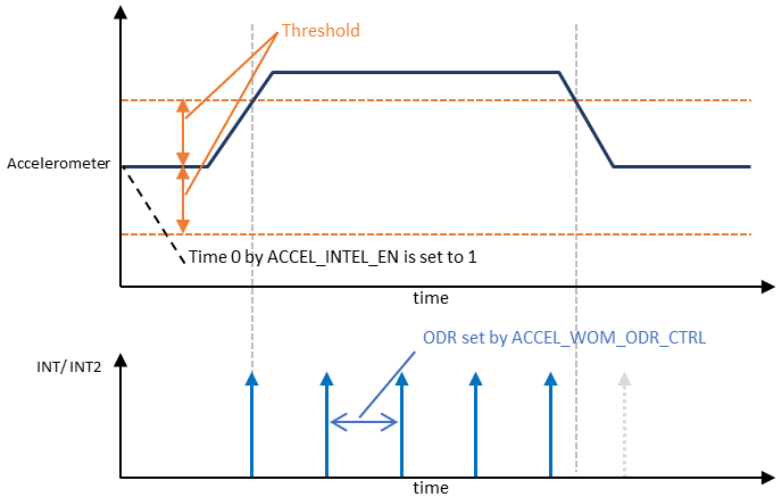

Figure 2. WoM absolute mode - threshold initialization

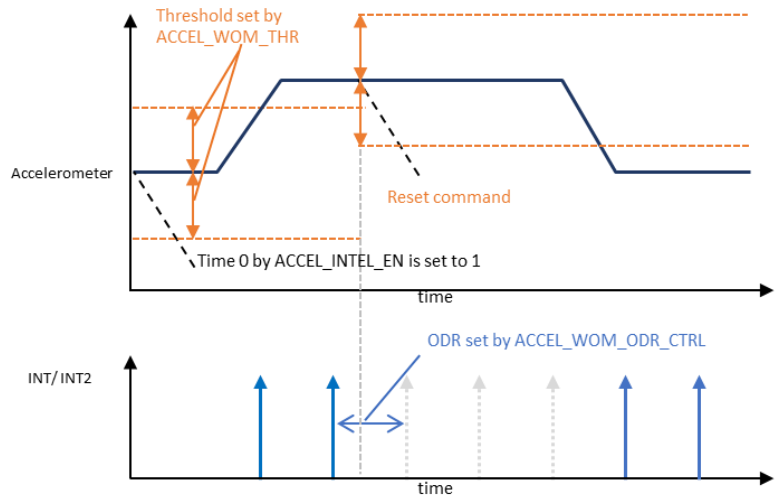

Figure 3. WoM absolute mode - threshold re-initialization

4.3.2. Mode 1: Relative acceleration mode

Activated by setting ACCEL_INTEL_MODE[6] = 1, in this mode the device compares each sample with the previous one and detects WoM if the difference is higher than the threshold.

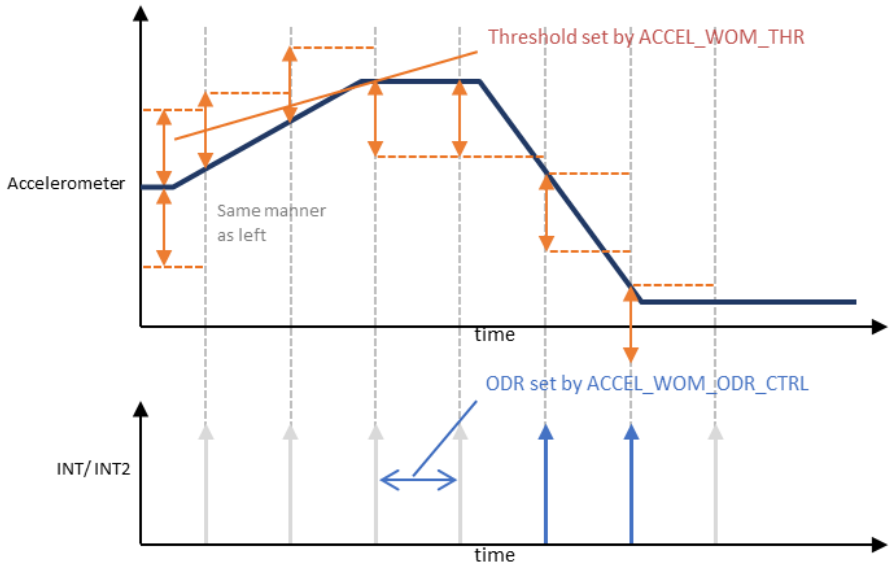

Figure 4. WoM relative mode

5 INTERRUPT PINS CONFIGURATION

WoM interrupt, as well as other interrupt sources provided by the IAM-20x80xx devices, are available for external MCU to detect on specific pins; namely INT (on all the devices on the family) and INT2 (on all the products but IAM-20680HP). Next table summarizes the configuration signals for the INT/INT2 pins.

Signal name	Address	Bit	Description
INT_LEVEL	0x37	7	1 – The logic level for INT/INT2 pin is active low. 0 – The logic level for INT/INT2 pin is active high.
INT_OPEN	0x37	6	1 – INT/INT2 pin is configured as open drain. 0 – INT/INT2 pin is configured as push-pull.
LATCH_INT_EN	0x37	5	1 – INT/INT2 pin level held until interrupt status is cleared. 0 – INT/INT2 pin indicates interrupt pulse's width is 50 µs.
INT_RD_CLEAR	0x37	4	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
INT2_EN	0x37	0	When INT2_EN = 0, all the interrupts appear on the INT pin, and INT2 interrupt pin is unused. When INT2_EN = 1, all interrupts except for data ready appear on the INT2 pin, and data ready interrupt appears on the INT interrupt pin.

Table 4. Interrupt pin configuration register

5.1. INT PIN STATUS LATCH

By setting LATCH_INT_EN = 1, the device's INT pin status can be latched to avoid passing over the signal in case of periodical INT monitoring from HOST. Then, INT pin status can be cleared by register read command, and read clear condition is programmable by INT_RD_CLEAR bit in register INT_PIN_CFG (0x37).
Key conditions at INT_PIN_CFG(0x37) in example below:
Bit 7 (INT_LEVEL) = 0 (The logic level for INT/INT2 pin is active high.)
Bit 6 (INT_OPEN) = 0 (INT/INT2 pin is configured as push-pull.)
Bit 5 (LATCH_INT_EN) = 1 (INT/INT2 pin level held until interrupt status is cleared.)

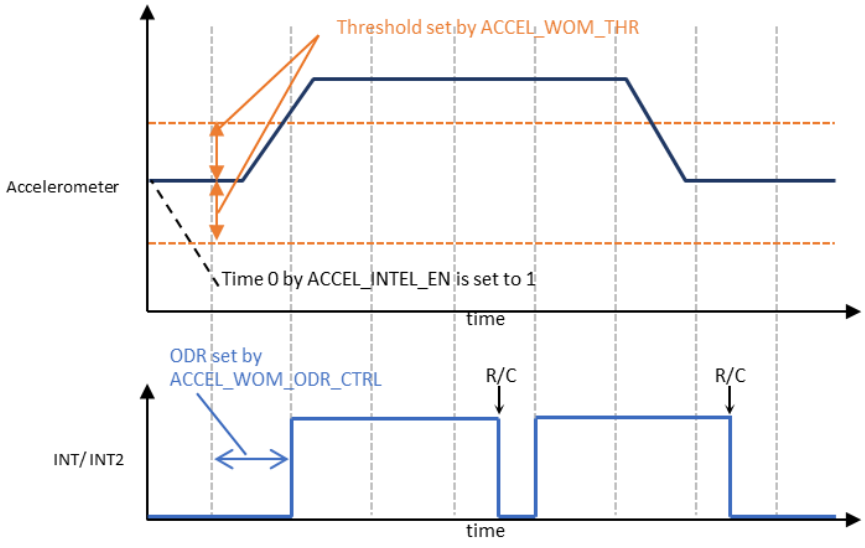

Figure 5. INT/INT2 pin behavior

5.2. STATUS REGISTER UPDATE

The serial interface allows detailed interrupt status information to be read from the Status register (0x3A: INT_STATUS) any time regardless of the INT pin status. If any interrupt event occurs, the status register is flagged immediately, and the interrupt status can be read. Also, the status register bit information is cleared once INT_STATUS is read regardless the INT_RD_CLEAR bit condition.
If the INT_RD_CLEAR bit is set to b'1, any register read command affects INT_STATUS register to be cleared. (See details in datasheet about INT_RD_CLEAR bit. Below table is a summary of read clear.

Read at	**INT_RD_CLEAR = 0**		**INT_RD_CLEAR = 1**	
	INT_STATUS	***Other registers***	***INT_STATUS***	***Other registers***
INT pin status	Cleared	Keep condition	Cleared	Cleared
INT_STATUS register	Cleared	Keep condition	Cleared	Cleared

Table 5. INT_RD_CLEAR bit effect detail

In case of INT_RD_CLEAR = 1, if HOST is aware that the INT signal is generated by only WoM event from an INT_ENABLE register setting standpoint, the HOST can directly read sensor values to clear the INT pin status when the HOST receive the INT signal.
On the other hand, in case of INT_RD_CLEAR bit is set to b'0, it is required to read INT_STATUS register to clear the INT pin status. Otherwise, next INT flagged timing could be not updated due to INT pin flag is maintained.

6 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/27/2023	1.0	Initial release
02/19/2025	2.0	Per-axis WoM functionality added Document general review

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