ICM-56686 Datasheet

High Precision 6-Axis MEMS MotionTracking™ Device

ICM-56686 HIGHLIGHTS

The ICM-56686 is a 6-axis MEMS MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer. It has a configurable host interface that supports I3C℠, I²C and SPI serial communication, features up to 4Kbyte FIFO and 2 programmable interrupts with ultra-low-power wake-on-motion support to minimize system power consumption.

ICM-56686 supports highly accurate external clock input, that helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation.

The device supports 20-bits motion sensor data (accelerometer data is 19-bits or 20-bits depending on bandwidth setting) format support in both sense registers and FIFO. Optionally, 16-bits data format is also supported.

Other industry-leading features include InvenSense on-chip APEX Motion Processing engine for gesture recognition, activity classification, and pedometer, along with programmable digital filters, and an embedded temperature sensor.

The device supports a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.08V to 3.6V.

ICM-56686 FEATURES

- User selectable Gyro Full-scale range (dps): ±15.625/31.25/62.5/125/250/500/1000/2000/4000
- User selectable Accelerometer Full-scale range (g): ± 2/4/8/16/32
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions:
  - Pedometer, Tilt Detection, Raise to Wake/Sleep, Tap Detection, Wake on Motion, Free-Fall Detection, Significant Motion Detection, Low-G Detection, High-G Detection, No-Motion Detection, Shake Detection, Flat Detection, Bring to See
- Host interface: 12.9 MHz I3C℠, 1 MHz I²C Slave, 24 MHz SPI

APPLICATIONS

- AR/VR Head Mounted Devices*
- Smartphones
- Wearables
- IoT Applications

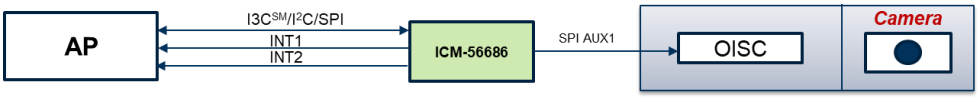
* Please contact TDK InvenSense for special considerations for use of this product in AR/VR head mounted device applications and dedicated accessories.

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-56686†	−40°C to +85°C	2.5x3mm 14-Pin LGA

†Denotes RoHS and Green-Compliant Package

BLOCK DIAGRAM



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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a preliminary product specification, providing a description, specifications, and design related information on the ICM-56686 MotionTracking device. The device is housed in a small 2.5x3x0.81 mm 14-pin LGA package.

Specifications and features described in the document are preliminary and subject to update.

1.2 PRODUCT OVERVIEW

The ICM-56686 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.81 mm (14-pin LGA) package. The ICM-56686 contains up to 4kByte FIFO (user can configure FIFO_DEPTH for default FIFO size 2kByte, and can extend it up to 4kByte by disabling APEX functions; see FIFO_DEPTH register field settings in the register map section) that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-56686, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports nine programmable full-scale range settings from ±15.625dps to ±4000dps, and the accelerometer supports five programmable full-scale range settings from ±2g to ±32g.

ICM-56686 also supports external clock input for highly accurate 20kHz to 40kHz clock, that helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation.

The device supports 20-bits motion sensor data (accelerometer data is 19-bits or 20-bits depending on bandwidth setting) format support in both sense registers and FIFO. Optionally, 16-bits data format is also supported. Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate VDDIO operating range of 1.08 V to 3.6 V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.9MHz (data rates up to 12.9Mbps in SDR mode, 25.8Mbps in DDR mode), the I^{2}C slave interface supports speeds up to 1 MHz, and the SPI interface supports speeds up to 24 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.81 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- AR/VR Head Mounted Devices*
- Smartphones
- Wearables
- IoT Applications

* Please contact TDK InvenSense for special considerations for use of this product in AR/VR head mounted device applications and dedicated accessories

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-56686 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, ±2000 and ±4000 degrees/sec
- Low Noise (LN) power mode support
- Digitally-programmable low-pass filters
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-56686 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g*, ±8*g*, ±16*g* and ±32*g*
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

ICM-56686 includes the following motion features, also known as APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen)

- Pedometer: Tracks Step Count, also issues Step Detect interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds a programmable angle for more than a programmable time.
- Raise to Wake/Sleep: Gesture detection for raise to wake and sleep events to disable or enable a device screen. Interrupt is issued when either of these two events are detected.
- Single Tap / Double Tap / Triple Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Significant Motion Detection: Detects significant motion based on accelerometer data.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.
- No-Motion Detection: State detection of No motion. Detects the static phase of a device and gives high level information about its tilt angle and its “majority face up.”
- Shake Detection: Gesture detection when user shakes a device.
- Flat Detection: Issues interrupt when the angle between device orientation and a programmable reference axis changes by at least a programmable angle for more than a programmable time.
- Bring to See: Gesture detection for wrist wearable device when user brings up the device screen to visible position.

User defined motion algorithms can be implemented as EDMP software depending on device capacity constraints.

2.4 ADDITIONAL FEATURES

ICM-56686 includes the following additional features:

- External clock input supports highly accurate clock input from 20kHz to 40kHz, helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation
- Up to 4kByte FIFO (user can configure FIFO_DEPTH for default FIFO size 2kByte, and can extend it up to 4kByte by disabling APEX functions; see FIFO_DEPTH register field settings in the register map section)
- EDMP Enhanced Digital Motion Processor for implementing motion algorithms
- 20-bits data format support in FIFO for high-data resolution
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- Host Interface: 12.9MHz I3C^{SM} (data rates up to 12.9Mbps in SDR mode, 25.8Mbps in DDR mode); 1 MHz I^{2}C slave host interface; 24 MHz SPI slave host interface
- AUX SPI interface for OIS controller

- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.81 mm (14-pin LGA)
- 20,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level; RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	AP_GYRO_FS_SEL =0; AUX1_GYRO_FS_SEL =0		±4000		º/s	3, 9
	AP_GYRO_FS_SEL =1; AUX1_GYRO_FS_SEL =1		±2000		º/s	3, 9
	AP_GYRO_FS_SEL =2; AUX1_GYRO_FS_SEL =2		±1000		º/s	3, 9
	AP_GYRO_FS_SEL =3; AUX1_GYRO_FS_SEL =3		±500		º/s	3, 9
	AP_GYRO_FS_SEL =4; AUX1_GYRO_FS_SEL =4		±250		º/s	3, 9
	AP_GYRO_FS_SEL =5; AUX1_GYRO_FS_SEL =5		±125		º/s	3, 9
	AP_GYRO_FS_SEL =6; AUX1_GYRO_FS_SEL =6		±62.5		º/s	3, 9
	AP_GYRO_FS_SEL =7; AUX1_GYRO_FS_SEL =7		±31.25		º/s	3, 9
	AP_GYRO_FS_SEL =8; AUX1_GYRO_FS_SEL =8		±15.625		º/s	3, 9
Gyroscope ADC Word Length	Output in two's complement format		16 or 20		bits	3
Sensitivity Scale Factor	AP_GYRO_FS_SEL =0; AUX1_GYRO_FS_SEL =0		8.2		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =1; AUX1_GYRO_FS_SEL =1		16.4		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =2; AUX1_GYRO_FS_SEL =2		32.8		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =3; AUX1_GYRO_FS_SEL =3		65.5		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =4; AUX1_GYRO_FS_SEL =4		131		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =5; AUX1_GYRO_FS_SEL =5		262		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =6; AUX1_GYRO_FS_SEL =6		524.3		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =7; AUX1_GYRO_FS_SEL =7		1048.6		LSB/(º/s)	3, 9
	AP_GYRO_FS_SEL =8; AUX1_GYRO_FS_SEL =8		2097.2		LSB/(º/s)	3, 9
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C		±0.2		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C, board-level		±0.01		%/ºC	1, 8
Full-Scale Nonlinearity	Best fit straight line; board-level, 25°C		±0.05		%FS	1, 8
Cross-Axis Sensitivity	Board-level		±0.2		%	1, 8
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Component-level, 25°C		±0.3		º/s	2
ZRO Change vs. Temperature	-40°C to +85°C, board-level		±0.005		º/s/ºC	1, 8
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz, 25°C; FSR < ±4000dps; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.0029		º/s /√Hz	1, 4
	@ 10 Hz, 25°C; FSR ±4000dps; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.0045		º/s /√Hz	1, 4
	@ 10 Hz, 25°C; FSR ±4000dps; 20-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.0025		º/s /√Hz	1, 4
Total RMS Noise	Bandwidth = 100 Hz; 25°C; FSR < ±4000dps; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.029		º/s-rms	4, 5
	Bandwidth = 100 Hz; 25°C; FSR ±4000dps; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.045		º/s-rms	4, 5
	Bandwidth = 100 Hz; 25°C; FSR ±4000dps; 20-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.025		º/s-rms	4, 5
Gyroscope Mechanical Frequencies			29.3		kHz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		35		ms	1, 6
Output Data Rate	Low Noise Mode (LNM)	12.5		6400	Hz	3, 7
	Low Power Mode (LPM)	1.5625		400	Hz	3, 7

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Rate Noise Spectral Density.
6. Measurement conditions: Gyroscope ODR = 6400Hz; Register field GYRO_UI_LPFBW_SEL set to 000 (low pass filter bypassed.
7. AUX1 output is fixed at 6.4kHz ODR LNM.
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs. Board-level MIN/MAX or MAX specs are based on 3σ calculation from limited 3-lots characterization data, using TDK-InvenSense test boards, not applicable to all production units.
9. Values shown are for 16-bits output. For 20-bits output, full-scale range is fixed at ±4000dps (131 LSB/dps).

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	AP_ACCEL_FS_SEL = 0; AUX1_ACCEL_FS_SEL = 0		±32		*g*	3, 9
	AP_ACCEL_FS_SEL = 1; AUX1_ACCEL_FS_SEL = 1		±16		*g*	3, 9
	AP_ACCEL_FS_SEL = 2; AUX1_ACCEL_FS_SEL = 2		±8		*g*	3, 9
	AP_ACCEL_FS_SEL = 3; AUX1_ACCEL_FS_SEL = 3		±4		*g*	3, 9
	AP_ACCEL_FS_SEL = 4; AUX1_ACCEL_FS_SEL = 4		±2		*g*	3, 9
ADC Word Length	Output in two's complement format		16 or 20		bits	3
Sensitivity Scale Factor	AP_ACCEL_FS_SEL = 0; AUX1_ACCEL_FS_SEL = 0		1,024		LSB/*g*	3, 9
	AP_ACCEL_FS_SEL = 1; AUX1_ACCEL_FS_SEL = 1		2,048		LSB/*g*	3, 9
	AP_ACCEL_FS_SEL = 2; AUX1_ACCEL_FS_SEL = 2		4,096		LSB/*g*	3, 9
	AP_ACCEL_FS_SEL = 3; AUX1_ACCEL_FS_SEL = 3		8,192		LSB/*g*	3, 9
	AP_ACCEL_FS_SEL = 4; AUX1_ACCEL_FS_SEL = 4		16,384		LSB/*g*	3, 9
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C		±0.2		%	2
Sensitivity Change vs. Temperature	0°C to +85°C, board-level		±0.01		%/ºC	1, 8
Full-Scale Nonlinearity	Best fit straight line, ±2g; board-level, 25°C		±0.01		%FS	1, 8
Cross-Axis Sensitivity	Board-level		±0.2		%	1, 8
ZERO-G OUTPUT						
Initial Tolerance	Component-level, 25°C		±10		m*g*	2
Zero-G Level Change vs. Temperature	0°C to +85°C, board-level		±0.15		m*g*/ºC	1, 8
OTHER PARAMETERS						
Noise Spectral Density	@ 10 Hz; 25°C; Up to ±8g FSR; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		55		µ*g*/√Hz	1, 4
	@ 10 Hz; 25°C; ±16g FSR; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		70		µ*g*/√Hz	1, 4
	@ 10 Hz; 25°C; ±32g FSR; 16-bits or 20-bits data; 800Hz ODR; LPF BW = 98.86Hz		100		µ*g*/√Hz	1, 4
RMS Noise	Bandwidth = 100 Hz; 25°C; Up to ±8g FSR; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.55		mg-rms	4, 5
	Bandwidth = 100 Hz; 25°C; ±16g FSR; 16-bits data; 800Hz ODR; LPF BW = 98.86Hz		0.7		mg-rms	4, 5
	Bandwidth = 100 Hz; 25°C; ±32g FSR; 16-bits or 20-bits data; 800Hz ODR; LPF BW = 98.86Hz		1.0		mg-rms	4, 5
Accelerometer Startup Time	From sleep mode to valid data		10		ms	1, 6
Output Data Rate	Low Noise Mode (LNM)	12.5		6400	12.5	3, 7
	Low Power Mode (LPM)	1.5625		400	1.5625	3, 7

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Noise Spectral Density.
6. Measurement conditions: Accelerometer ODR = 6400Hz; Register field ACCEL_UI_LPFBW_SEL set to 000 (low pass filter bypassed).
7. AUX1 output is fixed at 6.4kHz ODR LNM.
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs. Board-level MIN/MAX or MAX specs are based on 3σ calculation from limited 3-lots characterization data, using TDK-InvenSense test boards, not applicable to all production units.
9. Values shown are for 16-bits output. For 20-bits output, full-scale range is fixed at ±32g (16,384 LSB/g).

3.3 ELECTRICAL SPECIFICATIONS

D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.08*	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer (6400Hz ODR)		1.6		mA	2
	3-Axis Accelerometer (6400Hz ODR)		0.27		mA	2
	3-Axis Gyroscope (6400Hz ODR)		1.4		mA	2
Low-Power Mode	6-Axis Gyroscope + Accelerometer (50Hz ODR; Gyro 5x AVG; Accel 8x AVG)		0.45		mA	2
	6-Axis Gyroscope + Accelerometer (100Hz ODR; Gyro 5x AVG; Accel 8x AVG)		0.625		mA	2
	3-Axis Accelerometer (50Hz ODR; 8x AVG)		0.09		mA	2
	3-Axis Gyroscope (50Hz ODR; 5x AVG)		0.43		mA	2
	3-Axis Accelerometer (100Hz ODR; 8x AVG)		0.11		mA	2
	3-Axis Gyroscope (100Hz ODR; 5x AVG)		0.59		mA	2
Full-Chip Sleep Mode	At 25ºC		7.5		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

* Important Note: When using I3C^{SM} interface the minimum VDDIO value is 1.1V.

A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Valid power-on RESET Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		1	ms	1
Power Supply Noise	V_{DD}=1.8V or 3.6V, up to 1MHz		10	50	mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output	Output in two's complement format		0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	1.5625		3200	Hz	2, 4
Room Temperature Offset	25°C	-5		5	°C	3
Settling Time				0.242	sec	2
Sensitivity	Trimmed		128		LSB/°C	1
Sensitivity for FIFO data	Trimmed		2		LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			5	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	1
V_{IL}, Low Level Input Voltage		-0.5V		0.3*VDDIO	V	
C_I, Input Capacitance			<10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int0_tpulse_duration= 0 , 1 (100µs, 8µs) int1_tpulse_duration= 0 , 1 (100µs, 8µs)		100 or 8	100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Gyro inactive; 25°C	-1.25		+1.25	%	1
	Gyro active; 25°C	-1.25		+1.25	%	1
Frequency Variation over Temperature	Gyro inactive; -40°C to +85°C			±3	%	1
	Gyro active; -40ºC to +85ºC			±1	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Based on design. Not tested in production.
2. Guaranteed by design.
3. Production tested.
4. Temperature sensor ODR is the higher value between gyroscope and accelerometer ODR.

3.4 I²C SLAVE TIMING CHARACTERIZATION

Typical Operating Circuit of section 4, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.5			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.5			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.5			µs	1
C_b, Capacitive Load for each Bus Line				550	pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

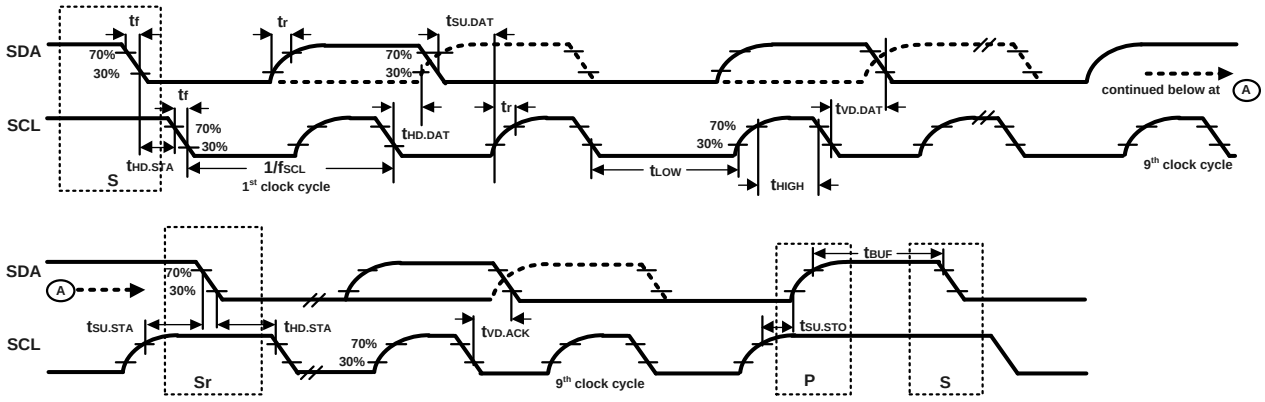

Figure 1. I²C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	VDDIO < 1.71V		VDDIO ≥ 1.71V			
		MIN	MAX	MIN	MAX	UNITS	NOTES
SPI TIMING							
f_{SPC}, SCLK Clock Frequency	Default		20		24	MHz	1
t_{LOW}, SCLK Low Period		23.5		17		ns	1
t_{HIGH}, SCLK High Period		22.5		17		ns	1
$t_{SU.CS}$, CS Setup Time		17		17		ns	1
$t_{HD.CS}$, CS Hold Time		5		5		ns	1
$t_{SU.SDI}$, SDI Setup Time		13		13		ns	1
$t_{HD.SDI}$, SDI Hold Time		8		8		ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF		18.5		18.5	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	3.5		3.5		ns	1
$t_{DIS.SDO}$, SDO Output Disable Time			28		28	ns	1

Table 6. 4-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

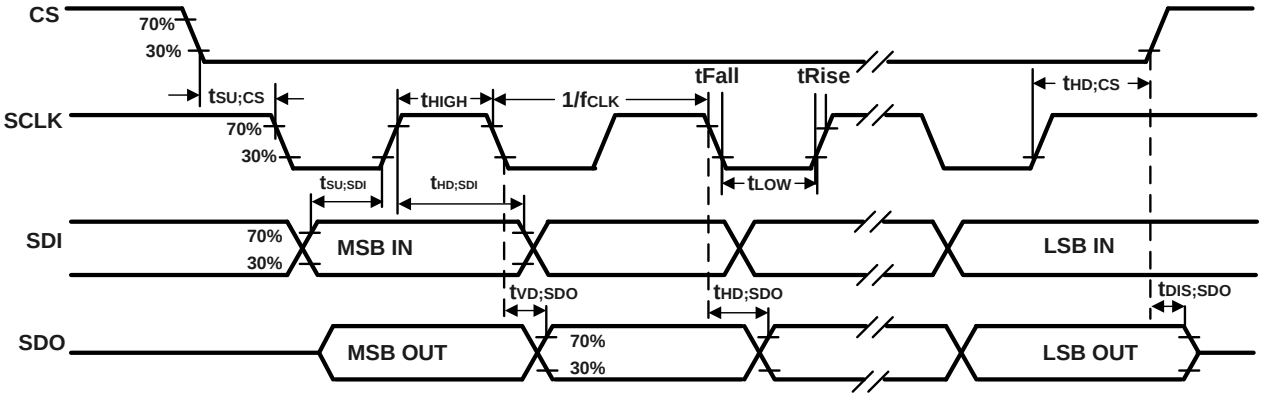

Figure 2. 4-Wire SPI Bus Timing Diagram

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3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	VDDIO < 1.71V		VDDIO ≥ 1.71V			
		MIN	MAX	MIN	MAX	UNITS	NOTES
SPI TIMING							
f_{SPC}, SCLK Clock Frequency	Default		20		24	MHz	1
t_{LOW}, SCLK Low Period		23.5		17		ns	1
t_{HIGH}, SCLK High Period		22.5		17		ns	1
$t_{SU.CS}$, CS Setup Time		17		17		ns	1
$t_{HD.CS}$, CS Hold Time		5		5		ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		13		13		ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8		8		ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF		18.5		18.5	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	3.5		3.5		ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time			28		28	ns	1

Table 7. 3-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

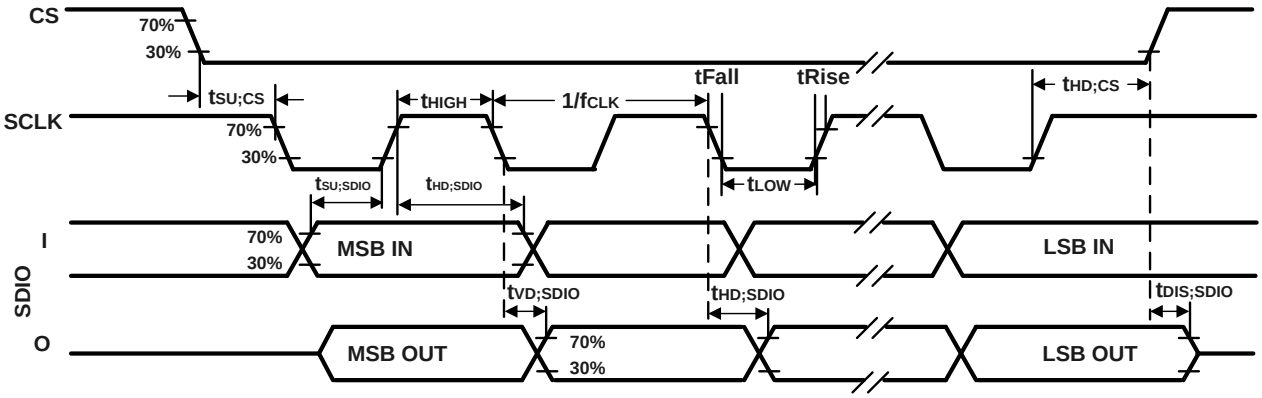

Figure 3. 3-Wire SPI Bus Timing Diagram

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3.7 RTC (CLKIN) TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
RTC (CLKIN) TIMING						
F_{RTC}, RTC Clock Frequency	Default	20	32	40	kHz	
$t_{HIGHRTC}$, RTC Clock High Period		1			µs	
$t_{RiseRTC}$, RTC Clock Rise Time		5		500	ns	
$t_{FallRTC}$, RTC Clock Fall Time		5		500	ns	

Table 8. RTC Timing Characteristics

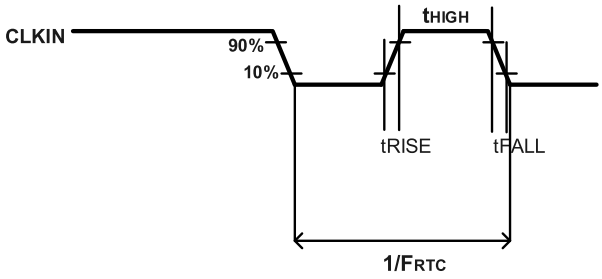

Figure 4. RTC Timing Diagram

External Clock Input Effect on ODR

ODR values supported by the device scale with external clock frequency, if external clock input is used. The ODR values shown in the datasheet are supported with external clock input frequency of 32kHz. For any other external clock input frequency, these ODR values will scale by a factor of (External clock value in kHz / 32). For example, if an external clock frequency of 32.768kHz is used, instead of ODR value of 500Hz, it will be 500 * (32.768 / 32) = 512Hz.

3.8 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (FSYNC, SCL, SDA)	-0.5 V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500 V (CDM)
Latch-up	JEDEC Class II (2), 125°C ±100 mA

Table 9. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Single Interface Mode	Dual Interface OIS Mode
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB
2	RESV / AUX1_SDIO / AUX1_SDI	RESV: No Connect or Connect to VDDIO or Connect to GND	AUX1_SDIO: AUX1 SPI serial data IO (3-wire mode); AUX1_SDI: AUX1 SPI serial data input (4-wire mode)
3	RESV AUX1_SCLK	RESV: No Connect or Connect to VDDIO or Connect to GND	AUX1_SCLK: AUX1 SPI serial clock
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All interrupts mapped to pin 4	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All interrupts mapped to pin 4
5	VDDIO	VDDIO: IO power supply voltage	VDDIO: IO power supply voltage
6	GND	GND: Power supply ground	GND: Power supply ground
7	RESV	RESV: No Connect or Connect to VDDIO or Connect to GND	RESV: No Connect or Connect to VDDIO or Connect to GND
8	VDD	VDD: Power supply voltage	VDD: Power supply voltage
9	INT2 / FSYNC / CLKIN	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; CLKIN: External clock input; If pin not used, can be No Connect or Connect to VDDIO	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; CLKIN: External clock input; If pin not used, can be No Connect or Connect to VDDIO
10	RESV / AUX1_CS	RESV: No Connect or Connect to VDDIO or Connect to GND	AUX1_CS: AUX1 SPI chip select
11	RESV / AUX1_SDO	RESV: No Connect or Connect to VDDIO or Connect to GND	AUX1_SDO: AUX1 SPI serial data output (4-wire mode); No Connect if pin not used
12	AP_CS	AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface	AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)

Table 10. ICM-56686 Signal Descriptions

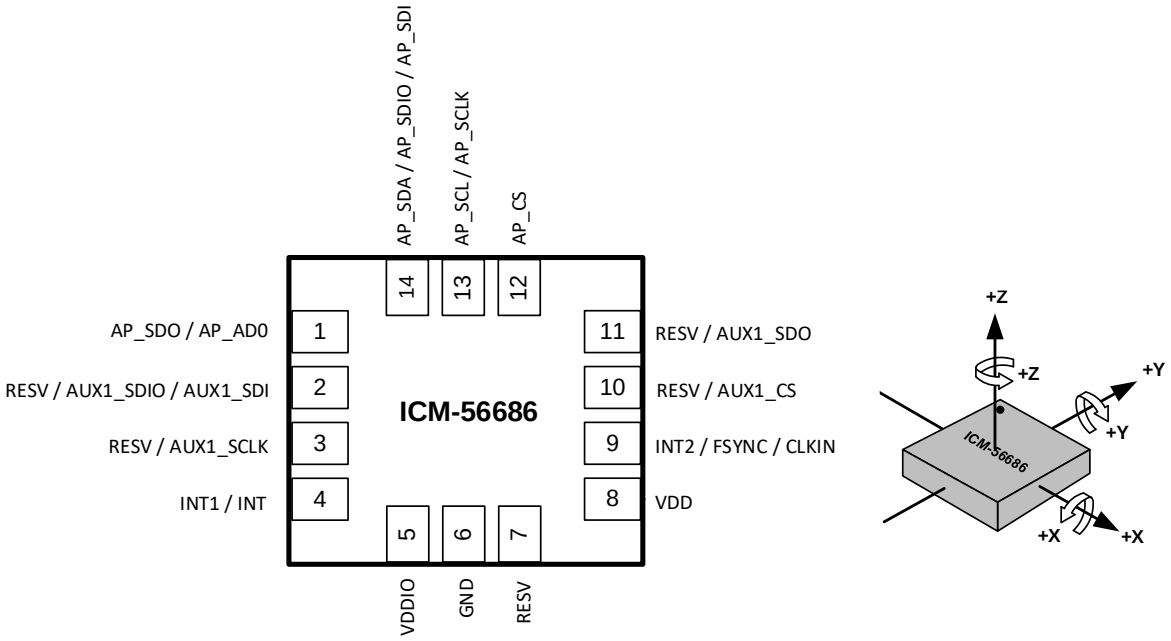

Figure 5. Pin Out Diagram for ICM-56686 2.5x3.0x0.81 mm LGA

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4.2 TYPICAL OPERATING CIRCUIT (SINGLE INTERFACE MODE)

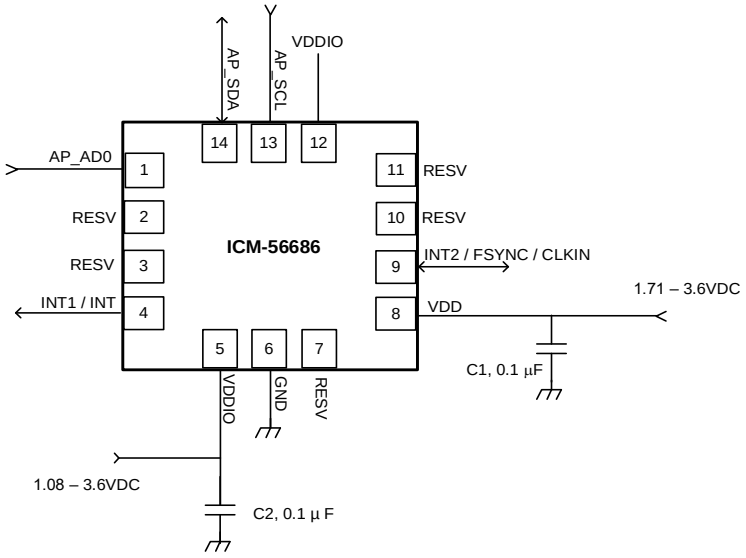

Figure 6. ICM-56686 Application Schematic Single Interface Mode (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

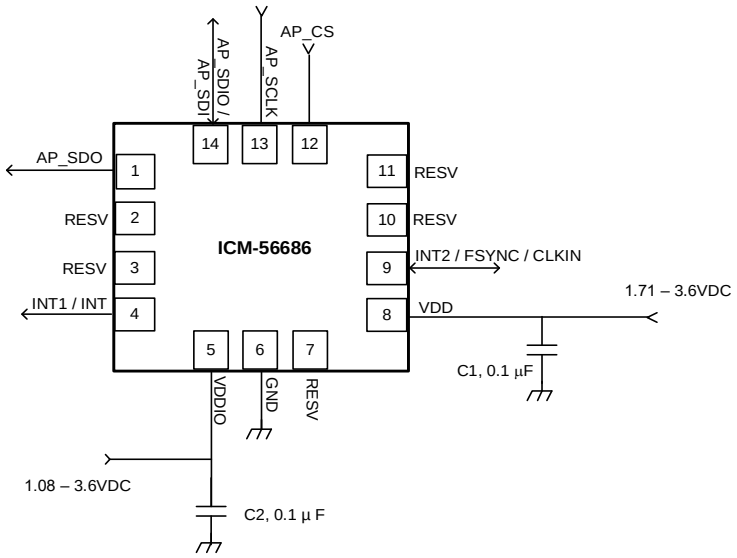

Figure 7. ICM-56686 Application Schematic Single Interface Mode (SPI Interface to Host)

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4.3 TYPICAL OPERATING CIRCUIT (DUAL INTERFACE OIS MODE)

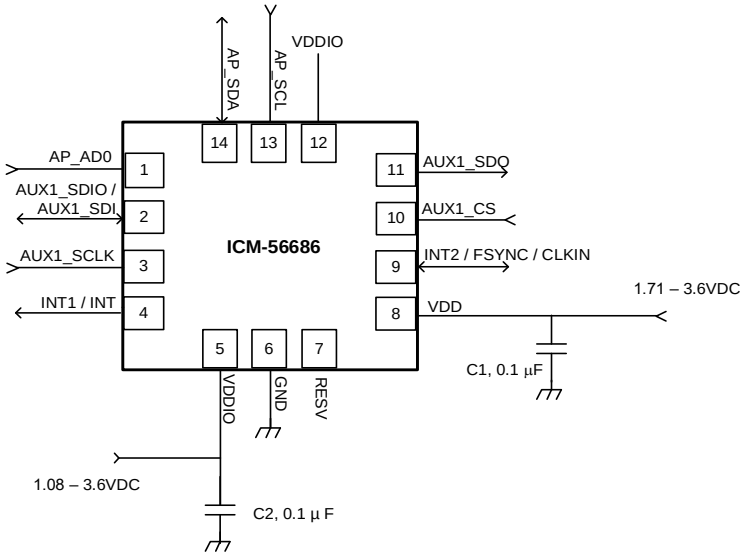

Figure 8. ICM-56686 Application Schematic Dual Interface OIS Mode (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

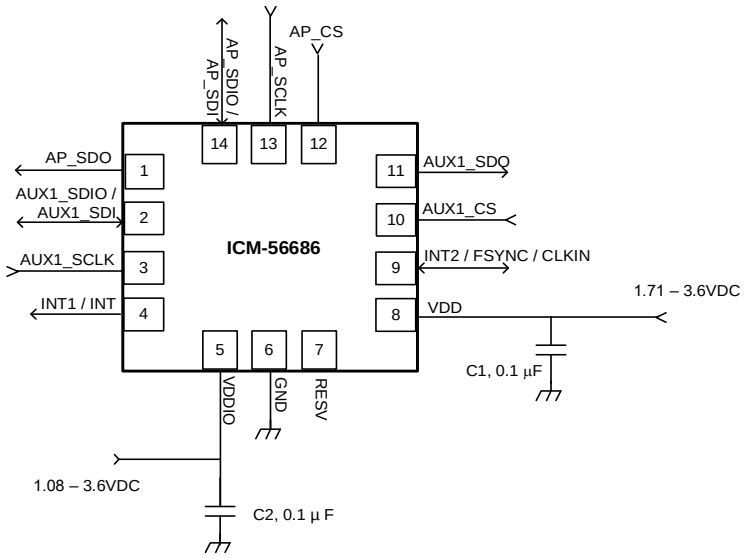

Figure 9. ICM-56686 Application Schematic Dual Interface OIS Mode (SPI Interface to Host)

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4.4 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitors	C1	X7R, 0.1µF ±10%	1
VDDIO Bypass Capacitor	C2	X7R, 0.1µF ±10%	1

Table 11. Bill of Materials

4.5 SYSTEM BLOCK DIAGRAM

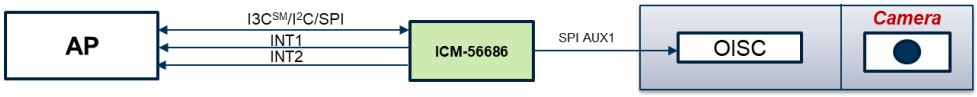

Figure 10. ICM-56686 System Block Diagram

4.6 OVERVIEW

The ICM-56686 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor
- Three-axis MEMS accelerometer sensor
- I3C^{SM}, I^{2}C and SPI Host Interface
- SPI Auxiliary Interface for connection to OIS controllers
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.7 THREE-AXIS MEMS GYROSCOPE

The ICM-56686 includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, ±2000, and ±4000 degrees per second (dps).

4.8 THREE-AXIS MEMS ACCELEROMETER

The ICM-56686 includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-56686 architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, ±16*g*, and ±32*g*.

Accelerometer data is 19-bits (default) or 20-bits (when bandwidth <= ODR/4).

4.9 FULL-SCALE RANGE IN HIGH-RESOLUTION MODE (20-BITS FORMAT)

20-bit output format is enabled by default (see bit sreg_sifs_20bits_en). In this mode the gyroscope output resolution is 20-bits, and the accelerometer output resolution is 19-bits (default) or 20-bits (when accel bandwidth is lowered below the default value of ODR/2).

Optionally, the 20-bit data can also be routed to the FIFO (see fifo_hires_en).

In high-resolution mode, the digital full-scale ranges are always ±4000dps (131.1 LSB/dps) and ±32g (16384 LSB/g). Lowering the FSRs (via fields ap_accel_fs_sel and ap_gyro_fs_sel) will impact only the analog full-scale ranges. In high-resolution mode, it is recommended to set the FSR field appropriately so as not to exceed analog FSR.

4.10 FULL-SCALE RANGE IN 16-BITS FORMAT

If high-resolution mode is disabled, the output resolution is 16-bits and the FSR fields will set both the digital and analog FSRs (defaults are ±4000dps and ±32g).

For gyroscope, full scale settings lower than ±250dps provide less resolution than 16-bits as shown in the table below.

Full Scale (dps)	Number of significant bits	Resolution (mdps/bit)
±4000	16	122.07
±2000	16	61.04
±1000	16	30.52
±500	16	15.26
±250	16	7.63
±125	15	7.63
±62.5	14	7.63
±31.25	13	7.63
±15.625	12	7.63

4.11 EXAMPLE OF 16-BITS AND 20-BITS WORD SIZE

The following table shows an example of gyroscope 16-bits and 20-bits word size at sensor register with a constant input.

Input signal	Full Scale	16-bits word (tracks the full-scale)	20-bits word
250 dps	±4000 dps	0000 1000 0000 0000	0000 1000 0000 0000 0000
250 dps	±2000 dps	0001 0000 0000 0000	0000 1000 0000 0000 0000
250 dps	±1000 dps	0010 0000 0000 0000	0000 1000 0000 0000 0000
250 dps	±500 dps	0100 0000 0000 0000	0000 1000 0000 0000 0000
250 dps	±250 dps	0111 1111 1111 1111	0000 1000 0000 0000 0000

4.12 SIGNAL SATURATION IN 16-BITS AND 20-BITS MODES

In 16-bits mode:

- The saturation is determined by the hard clamp on the MSB alignment due to the digital word shift.

In 20-bits mode:

- The digital signal path typically exceeds the analog dynamic range (unless maximum full-scale is selected), so the signal saturation happens in the analog path.
- The specification performance is fully guaranteed within the configured full scale, but in practice it will extend beyond that level.

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4.13 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The ICM-56686 communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The ICM-56686 always acts as a slave when communicating to the application processor.

4.14 SPI AUXILIARY INTERFACE FOR CONNECTION TO OIS CONTROLLERS

The ICM-56686 has an SPI auxiliary interface for connection to OIS controllers. The ICM-56686 always acts as a slave when communicating with OIS controller over this interface.

4.15 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.16 CLOCKING

The ICM-56686 has a flexible clocking scheme, allowing external or internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers.

The CLKIN pin on ICM-56686 provides the ability to input an external clock. A highly accurate external clock may be used rather than the internal clocks sources, if greater clock accuracy is desired. External clock input supports highly accurate clock input from 20kHz to 40kHz.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

For internal sources, the only setting supporting specified performance in all modes is option b). It is recommended that option b) be used when using internal clock source.

4.17 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.18 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.19 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-56686 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature sensor register data TEMP_DATA is updated with new data at max(Accelerometer ODR, Gyroscope ODR).

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA / 2) + 25

4.20 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-56686.

4.21 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.22 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-56686.

Name	Gyro	Accel
Sleep Mode	Off	Off
Standby Mode	Drive On	Off
Accelerometer Low-Power Mode	Off	Duty-Cycled
Accelerometer Low-Noise Mode	Off	On
Gyroscope Low-Power Mode	Duty-Cycled	Off
Gyroscope Low-Noise Mode	On	Off
6-Axis Low-Power Mode	Duty-Cycled	Duty-Cycled
6-Axis Low-Noise Mode	On	On

Table 12. Standard Power Modes for ICM-56686

5 FIFO

The ICM-56686 contains up to 4kByte FIFO (user can configure FIFO_DEPTH for default FIFO size 2kByte, and can extend it up to 4kByte by disabling APEX functions; see FIFO_DEPTH register field settings in the register map section) that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

ICM-56686 includes FIFO Compression algorithm that allows storing compressed sensor data in FIFO frames, thus virtually providing more FIFO space. It allows to store up to 4 times the number of frames with respect to non-compressed data. Frame decompression must be performed on the Host which reads the FIFO. Compression algorithm uses a hardware lossless algorithm, based on data variation analysis of each axis. Compression ratios x2, x3, x4 are supported, providing up to 16kByte data storage capability.

FIFO packet decimation capability is provided for additional storage optimization. User can configure the FIFO Data Rate (FDR) to control the decimation rate for writing packets to the FIFO. User must disable sensors when initializing FDR control value or making changes to it.

5.1 PACKET STRUCTURE

FIFO packets are assembled in different packet sizes based on the enabled sensors. When internal sensors Accel and Gyro are enabled, the following packets are available:

- 8 bytes packet: Contains Accel-only or Gyro-only data and Temperature data (1 byte)
- 16 bytes packet: Contains Accel data, Gyro data, Temperature data (1 byte), Timestamp
- 20 bytes packet: Contains high-resolution Accel data, Gyro data, Temperature data (2 bytes), Timestamp

The following figure shows packets organization for each format (big endian mode).

Accel-only (8 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Temp (1 byte)	

Gyro-only (8 bytes)

	7	0
0	Header	
1	Gx H	
2	Gx L	
3	Gy H	
4	Gy L	
5	Gz H	
6	Gz L	
7	Temp (1 byte)	

Accel+Gyro (16 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Gx H	
8	Gx L	
9	Gy H	
10	Gy L	
11	Gz H	
12	Gz L	
13	Temp (1 byte)	
14	Timestamp H	
15	Timestamp L	

Accel+Gyro High Resolution (20 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Gx H	
8	Gx L	
9	Gy H	
10	Gy L	
11	Gz H	
12	Gz L	
13	Temp H	
14	Temp L	
15	Timestamp H	
16	Timestamp L	
17	Ax LSB	Gx LSB
18	Ay LSB	Gy LSB
19	Az LSB	Gz LSB

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5.2 FIFO HEADER

The following table shows the structure of the first byte of the FIFO header.

Bit Field	Item	Description
7	EXT_HEADER	1: FIFO header length is extended to 2 bytes. The second byte is used for compressed frame decoding fields 0: FIFO header length is 1 byte
6	ACCEL_EN	1: Accel is enabled or high resolution is enabled 0: Accel is not enabled and high resolution is not enabled
5	GYRO_EN	1: Gyro is enabled or high resolution is enabled 0: Gyro is not enabled and high resolution is not enabled
4	HIRES_EN	1: High-resolution is enabled (20-bytes format) 0: High-resolution is not enabled
3	TMST_FIELD_EN	1: Timestamp field is included in the packet. This requires that: a) high-resolution is enabled, or b) both Accel and Gyro are enabled The timestamp field contains the timestamp value or FSYNC-ODR delay depending on configuration 0: Timestamp field is not included in the packet
2	FSYNC_TAG_EN	1: FSYNC is triggered and the Timestamp field contains the FSYNC-ODR delay 0: FSYNC is not triggered and the Timestamp field does not contain the FSYNC-ODR delay
1	ACCEL_ODR	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel
0	GYRO_ODR	1: The ODR for gyro is different for this gyro data packet compared to the previous gyro packet 0: The ODR for gyro is the same as the previous packet with gyro

6 INTERRUPTS

The ICM-56686 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts:

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-56686 includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

7 EDMP

The on-chip Enhanced Digital Motion Processor (EDMP) is designed for motion processing of next-gen sensor products. It enables ultra-low power run-time and offloads computation of motion processing and sensor fusion algorithms from the host processor. It enables the host system to execute custom algorithms and issue software interrupts to the external environment. The EDMP can be deployed in the system to minimize system level power, simplify the software architecture, and save valuable MIPS on the host processor. The EDMP implements a motion sensor optimized custom ISA (1-4 byte) with special motion processing instructions.

8 APEX MOTION FUNCTIONS

The APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen) features of ICM-56686 consist of:

- Pedometer: Tracks Step Count, also issues Step Detect interrupt.
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds a programmable angle for more than a programmable time.
- Raise to Wake/Sleep: Gesture detection for raise to wake and sleep events to disable or enable a device screen. Interrupt is issued when either of these two events are detected.
- Single Tap / Double Tap / Triple Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Significant Motion Detection: Detects significant motion based on accelerometer data.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.
- No-Motion Detection: State detection of No motion. Detects the static phase of a device and gives high level information about its tilt angle and its “majority face up.”
- Shake Detection: Gesture detection when user shakes a device.
- Flat Detection: Issues interrupt when the angle between device orientation and a programmable reference axis changes by at least a programmable angle for more than a programmable time.
- Bring to See: Gesture detection for wrist wearable device when user brings up the device screen to visible position.

These functions are run as software on EDMP.

9 DIGITAL INTERFACE

9.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-56686 can be accessed using I3C^{SM} at 12.9 MHz (data rates up to 12.9Mbps in SDR mode, 25.8Mbps in DDR mode), I^{2}C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in section 4.

9.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility. The I3C^{SM} capability of this device is compliant with Version 1.0 of the MIPI Alliance Specification for I3C^{SM}.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-56686 supports the following features of I3C^{SM}:

- SDR data rate up to 12.9Mbps
- DDR data rate up to 25.8Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-56686 always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

The following table shows I3C^{SM} Common Command Code (CCC) commands supported by the device.

	CCC Description	Required or Optional per I3C v1.0	Supported by ICM-56686
1	ENEC, broadcast mode. (Enable Events)	Required	Yes
2	DISEC, broadcast mode. (Disable Events)	Required	Yes
3	ENTAS0, broadcast mode. (Enter Activity State 0)	Required	Yes
4	ENTAS1, broadcast mode. (Enter Activity State 1)	Optional	No
5	ENTAS2, broadcast mode. (Enter Activity State 0)	Optional	No
6	ENTAS3, broadcast mode. (Enter Activity State 0)	Optional	No
7	RSTDAA, broadcast mode. (Reset dynamic address assignment)	Required	Yes
8	ENTDAA, broadcast mode. (Enter dynamic address assignment)	Required	Yes
9	DEFSLVS, broadcast mode. (Define list of slaves)	Optional	No
10	SETMWL, broadcast mode. (Set Max Write Length)	Required	Yes
11	SETMRL, broadcast mode. (Set Max Read Length)	Required	Yes
12	ENTTM, broadcast mode. (Enter Test Mode)	Optional	No
13	ENTHDR0, broadcast mode. (Enter HDR DDR mode)	Optional	Yes
14	ENTHDR1, broadcast mode. (Enter HDR TSP mode)	Optional	No
15	ENTHDR2, broadcast mode. (Enter HDR TSL mode)	Optional	No
16	SETXTIME, broadcast mode. (Exchange Timing Information)		

	16.1	Defining byte = 0x7F (ST)	Optional	No
	16.2	Defining byte = 0xBF (DT)	Optional	No
	16.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
	16.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
	16.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
	16.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
	16.7	Defining byte = 0xFD (Async Trigger for Async Mode 3)	Optional	No
	16.8	Defining byte = 0x3F (TPH)	Optional	No
	16.9	Defining byte = 0x9f (TU)	Optional	No
	16.10	Defining byte = 0x8F (ODR)	Optional	No
	16.11	Defining byte = 0xff (disable all timing control function)	Optional	Yes
17	ENEC, direct mode. (Enable Events)		Required	Yes
18	DISEC, direct mode. (Disable Events)		Required	Yes
19	ENTAS0, direct mode. (Enter Activity State 0)		Required	Yes
20	ENTAS1, direct mode. (Enter Activity State 1)		Optional	No
21	ENTAS2, direct mode. (Enter Activity State 2)		Optional	No
22	ENTAS3, direct mode. (Enter Activity State 3)		Optional	No
23	RSTDAA, direct mode. (Reset dynamic address assignment)		Required	Yes
24	SETDASA, direct mode. (Set Dynamic address from static address)		Optional	Yes
25	SETNEWDA, direct mode. (Set new dynamic address)		Required	Yes
26	SETMWL, direct mode. (Set Max Write Length)		Required	Yes
27	SETMRL, direct mode. (Set Max Read length)		Required	Yes
28	GETMWL, direct mode. (Get Max write length)		Required	Yes
29	GETMRL, direct mode. (Get Max Read length)		Required	Yes
30	GETPID, direct mode. (Get provisional ID)		Required	Yes
31	GETBCR, direct mode. (Get Bus Characteristics Register)		Required	Yes
32	GETDCR, direct mode. (Get Device Characteristics Register)		Required	Yes
33	GETSTATUS, direct mode. (Get Device Status)		Required	Yes
34	GETACCMST, direct mode. (Get Accept Mastership)		Optional	No
35	SETBRGTGT, direct mode. (Set Bridge Targets)		Optional	No
36	GETMXDS, direct mod. (Get Max Data Speed)		Optional	Yes
37	GETHDRCAP, direct mode. (Get HDR capability)		Optional	Yes
38	SETXTIME, direct mode. (Set Exchange Timing information)			
	38.1	Defining byte = 0x7F (ST)	Optional	No
	38.2	Defining byte = 0xBF (DT)	Optional	No
	38.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
	38.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
	38.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
	38.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
	38.7	Defining byte = 0xFD (Async Trigger for Async Mode 3)	Optional	No
	38.8	Defining byte = 0x3F (TPH)	Optional	No
	38.9	Defining byte = 0x9f (TU)	Optional	No

	38.10	Defining byte = 0x8F (ODR)	Optional	No
	38.11	Defining byte = 0xff (disable all timing control function)	Optional	Yes
39	GETXTIME, direct mode. (Get Exchange Timing Information)		Optional	Yes

Table 13. I3C^{SM} CCC Commands

9.3 I^{2}C INTERFACE

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-56686 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-56686 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-56686s to be connected to the same I^{2}C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

9.4 SPI INTERFACE

The ICM-56686 supports 3-wire or 4-wire SPI for the host interface. The ICM-56686 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 20 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the Register Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

Register Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

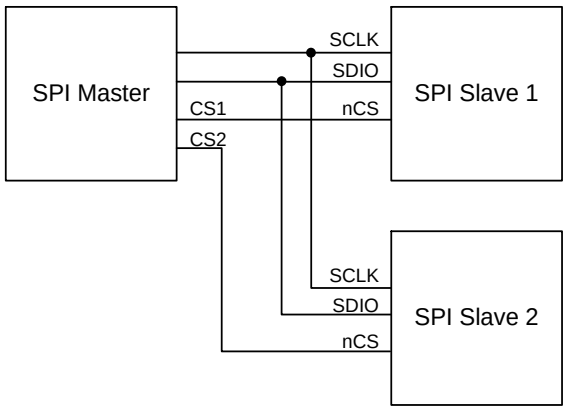


Figure 11. Typical SPI Master/Slave Configuration

10 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

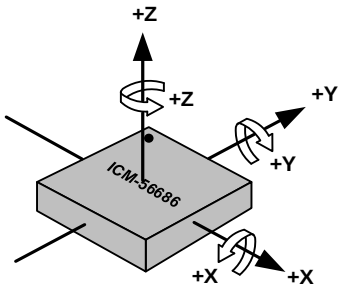
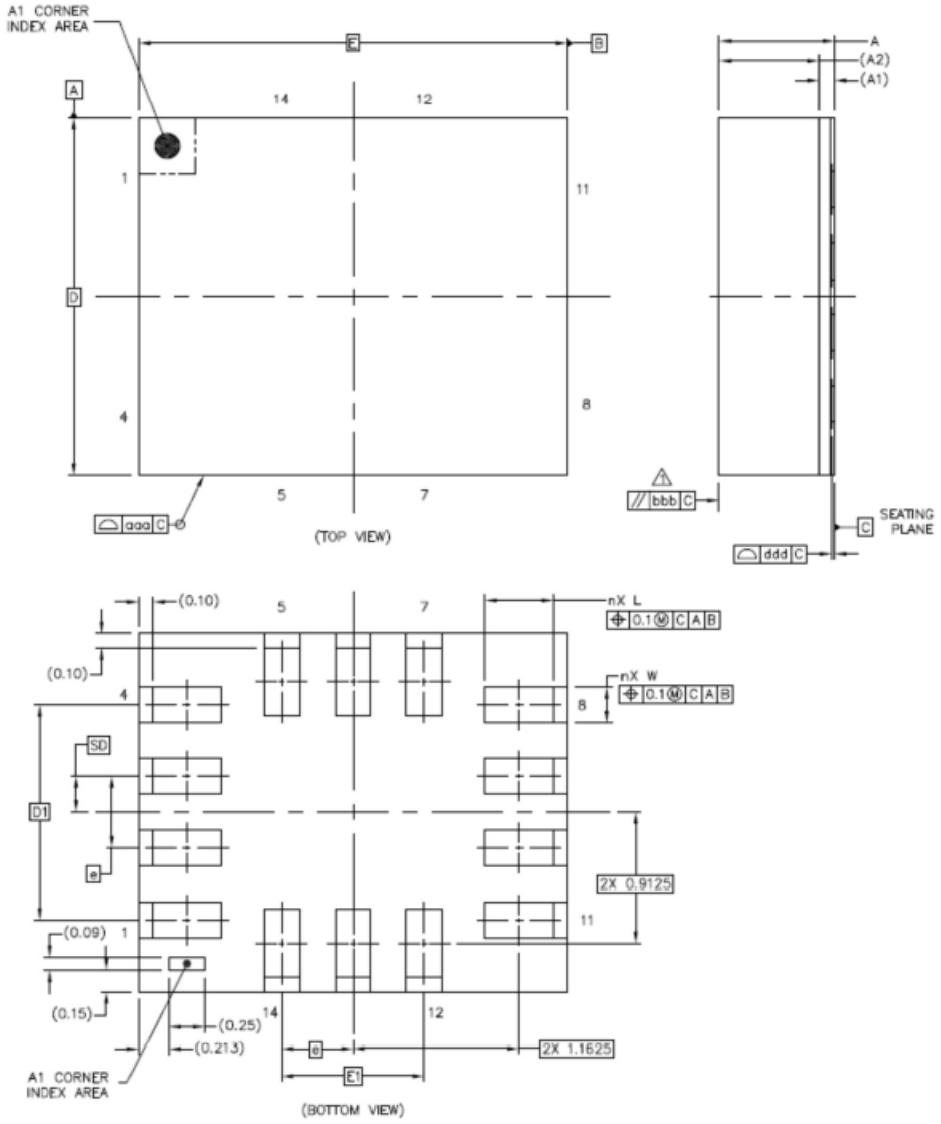


Figure 12. Orientation of Axes of Sensitivity and Polarity of Rotation

10.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.81) mm NiAu pad finish



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	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.76	0.81	0.86
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.7	REF
Body Size	D		2.5	BSC
	E		3	BSC
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.425	0.475	0.525
Lead Pitch	e		0.5	BSC
Lead Count	n		14	
Edge Ball Center to Center	D1		1.5	BSC
	E1		1	BSC
Body Center to Contact Ball	SD		0.25	BSC
	SE		---	BSC
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	

11 DEVICE PACKAGE IN TAPE AND REEL

ICM-56686 devices are packaged in the tape and reel as shown in the figures below.

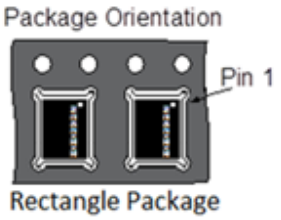

Figure 13. ICM-56686 Device Package in Tape and Reel

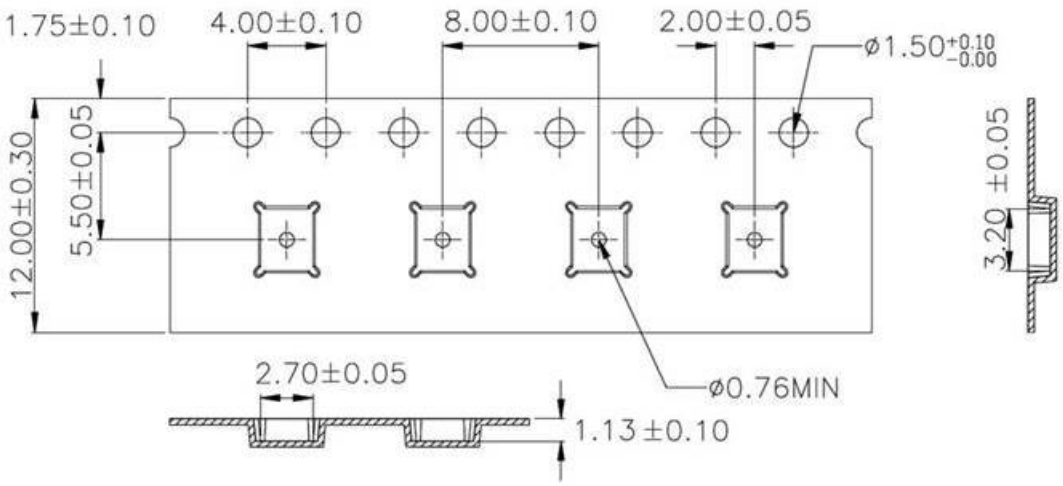

Figure 14. Tape Dimensions with ICM-56686 Device Package

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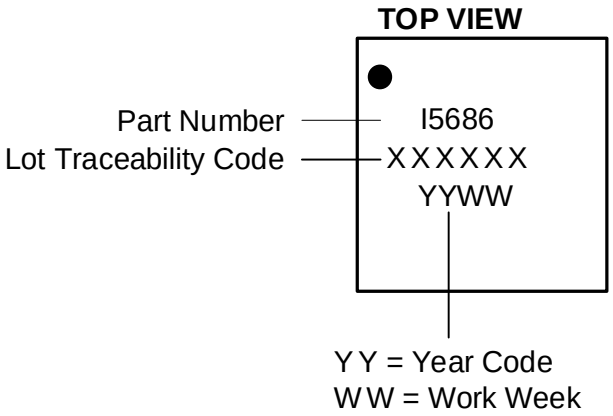
12 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-56686 devices is summarized below:

Part Number	Part Number Package Marking
ICM-56686	I5686



13 INDIRECT REGISTER ACCESS

13.1 HOST INDIRECT ACCESS REGISTER (IREG)

An IREG is a register or a memory storage element that is not addressed directly by a 7-bit address. IREGs can only be addressed using an internal 16-bit address. Indirect register access procedures described in this section must be used to access all IREGs.

The host configures the internal 16-bit address by programming following registers: {ireg_addr_15_8[7:0], ireg_addr_7_0[7:0]}.

13.2 GENERAL RULES FOR ACCESSING IREG

1. Burst-write and burst-read operations are not supported when accessing IREGs from the host.
2. Reading of an IREG is done on a read-pre-fetch basis (details in IREG READ section below).
3. A minimum wait time (refer to section MINIMUM WAIT TIME GAP below for details) is required between two consecutive read/write access to an IREG.

13.3 MINIMUM WAIT TIME-GAP

The minimum time gap between two consecutive IREG accesses for various IREG components is 4µs.

13.4 IREG WRITE

Procedure for writing to an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_ANA, it should add base address 0xA300 to the address of that register shown in the IPREG_ANA registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. The host programs the write data to the IREG_DATA register.
3. The above programming steps must be performed in a single burst-write transaction to prevent an un-intended read-pre-fetch operation.
4. After the IREG_DATA register is written, an internal operation is triggered to pass the contents from the IREG_DATA register to a register pointed by {IREG_ADDR_7_0, IREG_ADDR_15_8}.
5. After the contents from the IREG_DATA register is written to the selected register, the internal 16-bit address is auto-incremented.
6. After a minimum wait time-gap, the host can write to the IREG_DATA register again, which is effectively writing to the register pointed by the post-auto-incremented address.
7. Or, after a minimum wait time-gap, the host can program a new destination address for the next write operation.

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13.5 IREG READ

Procedure for reading from an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_ANA, it should add base address 0xA300 to the address of that register shown in the IPREG_ANA registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. Upon the CSB=1 (SPI) or STOP (I2C) after the above programming, an internal read-pre-fetch operation is triggered.
3. The internal read-pre-fetch operation returns the desired data, which is saved to the IREG_DATA register.
4. After a minimum wait time-gap, the host reads the IREG_DATA register to retrieve the read-data.
5. After the host reads the IREG_DATA register, the internal 16-bit address is auto-incremented, and another internal read-pre-fetch is automatically triggered, to fetch data from the IREG register pointed to by the post-auto-incremented address.
6. After a minimum wait time-gap, the host can either read the IREG_DATA register to get the read-data from the next address location, or it can program a new read address.

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14 REGISTER MAP

This section lists the register map for the ICM-56686.

14.1 USER BANK IPREG_BAR REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	IPREG_BAR_REG_56	PADS_AP_SCLK_PUD_TRIM_D2A[0]	PADS_AP_SCLK_PE_TRIM_D2A[0]	-	PADS_AP_CS_PUD_TRIM_D2A[0]	PADS_AP_CS_PE_TRIM_D2A[0]	-		
39	57	IPREG_BAR_REG_57	PADS_AUX_CS_TP3_TP_PE_TRIM_D2A[0]	-	PADS_AP_SDO_PUD_TRIM_D2A[0]	PADS_AP_SDO_PE_TRIM_D2A[0]	-	PADS_AP_SDI_PUD_TRIM_D2A[0]	PADS_AP_SDI_PE_TRIM_D2A[0]	-
3A	58	IPREG_BAR_REG_58	-	PADS_AUX_SDI_TP1_TP_PUD_TRIM_D2A[0]	PADS_AUX_SDI_TP1_TP_PE_TRIM_D2A[0]	-	PADS_AUX_SCLK_TP2_TP_PUD_TRIM_D2A[0]	PADS_AUX_SCLK_TP2_TP_PE_TRIM_D2A[0]	-	PADS_AUX_CS_TP3_TP_PUD_TRIM_D2A[0]
3B	59	IPREG_BAR_REG_59	PADS_INT2_PUD_TRIM_D2A[0]	PADS_INT2_PE_TRIM_D2A[0]	-	PADS_INT1_TP0_TP_PUD_TRIM_D2A[0]	PADS_INT1_TP0_TP_PE_TRIM_D2A[0]	-	PADS_AUX_SDO_PUD_TRIM_D2A[0]	PADS_AUX_SDO_PE_TRIM_D2A[0]
45	69	IPREG_BAR_REG_69	-						PADS_OD_PUD_STRENGTH_TRIM_D2A[1:0]	

14.2 USER BANK IPREG_ANA REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	08	IPREG_ANA_REG_8	-						PD_ACCEL_ST_B_D2A[0]	PD_ACCEL_CP45_ST_B_D2A[0]

14.3 USER BANK IMEM_SRAM REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	IMEM_SRAM_REG_0	GYRO_X_STR_FT[7:0]							
01	01	IMEM_SRAM_REG_1	GYRO_X_STR_FT[15:8]							
02	02	IMEM_SRAM_REG_2	GYRO_Y_STR_FT[7:0]							
03	03	IMEM_SRAM_REG_3	GYRO_Y_STR_FT[15:8]							
04	04	IMEM_SRAM_REG_4	GYRO_Z_STR_FT[7:0]							
05	05	IMEM_SRAM_REG_5	GYRO_Z_STR_FT[15:8]							
06	06	IMEM_SRAM_REG_6	GYRO_X_CMOS_GAIN_FT[7:0]							
07	07	IMEM_SRAM_REG_7	-				GYRO_X_CMOS_GAIN_FT[11:8]			
08	08	IMEM_SRAM_REG_8	GYRO_Y_CMOS_GAIN_FT[7:0]							
09	09	IMEM_SRAM_REG_9	-				GYRO_Y_CMOS_GAIN_FT[11:8]			
0A	10	IMEM_SRAM_REG_10	GYRO_Z_CMOS_GAIN_FT[7:0]							
0B	11	IMEM_SRAM_REG_11	-				GYRO_Z_CMOS_GAIN_FT[11:8]			
0C	12	IMEM_SRAM_REG_12	ACCEL_X_STR_FT[7:0]							
0D	13	IMEM_SRAM_REG_13	ACCEL_X_STR_FT[15:8]							
0E	14	IMEM_SRAM_REG_14	ACCEL_Y_STR_FT[7:0]							
0F	15	IMEM_SRAM_REG_15	ACCEL_Y_STR_FT[15:8]							
10	16	IMEM_SRAM_REG_16	ACCEL_Z_STR_FT[7:0]							
11	17	IMEM_SRAM_REG_17	ACCEL_Z_STR_FT[15:8]							

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14.4 USER BANK IMEM_SRAM_APEX REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	42	IMEM_SRAM_APEX_REG_42	ODR_FF[7:0]							
2B	43	IMEM_SRAM_APEX_REG_43	ODR_FF[15:8]							
2C	44	IMEM_SRAM_APEX_REG_44	ODR_TAP[7:0]							
2D	45	IMEM_SRAM_APEX_REG_45	ODR_TAP[15:8]							
2E	46	IMEM_SRAM_APEX_REG_46	ODR_R2W[7:0]							
2F	47	IMEM_SRAM_APEX_REG_47	ODR_R2W[15:8]							
30	48	IMEM_SRAM_APEX_REG_48	ODR_3AXIS[7:0]							
31	49	IMEM_SRAM_APEX_REG_49	ODR_3AXIS[15:8]							
32	50	IMEM_SRAM_APEX_REG_50	ODR_TILT[7:0]							
33	51	IMEM_SRAM_APEX_REG_51	ODR_TILT[15:8]							
34	52	IMEM_SRAM_APEX_REG_52	ODR_PED[7:0]							
35	53	IMEM_SRAM_APEX_REG_53	ODR_PED[15:8]							
36	54	IMEM_SRAM_APEX_REG_54	ODR_SMD[7:0]							
37	55	IMEM_SRAM_APEX_REG_55	ODR_SMD[15:8]							
38	56	IMEM_SRAM_APEX_REG_56	ODR_B2S[7:0]							
39	57	IMEM_SRAM_APEX_REG_57	ODR_B2S[15:8]							
3A	58	IMEM_SRAM_APEX_REG_58	ODR_SHAKE[7:0]							
3B	59	IMEM_SRAM_APEX_REG_59	ODR_SHAKE[15:8]							
3C	60	IMEM_SRAM_APEX_REG_60	ODR_NOMOTION[7:0]							
3D	61	IMEM_SRAM_APEX_REG_61	ODR_NOMOTION[15:8]							
3E	62	IMEM_SRAM_APEX_REG_62	ODR_FLAT[7:0]							
3F	63	IMEM_SRAM_APEX_REG_63	ODR_FLAT[15:8]							
62	98	IMEM_SRAM_APEX_REG_98	QUAT_RESET_EN[7:0]							
63	99	IMEM_SRAM_APEX_REG_99	TILT_RESET_EN[7:0]							
79	121	IMEM_SRAM_APEX_REG_121	PED_STEP_CADENCE[7:0]							
7A	122	IMEM_SRAM_APEX_REG_122	PED_ACTIVITY_CLASS[7:0]							
7C	124	IMEM_SRAM_APEX_REG_124	PED_STEP_CNT_BUF1[7:0]							
7D	125	IMEM_SRAM_APEX_REG_125	PED_STEP_CNT_BUF1[15:8]							
7E	126	IMEM_SRAM_APEX_REG_126	PED_STEP_CNT_BUF2[7:0]							
7F	127	IMEM_SRAM_APEX_REG_127	PED_STEP_CNT_BUF2[15:8]							
88	136	IMEM_SRAM_APEX_REG_136	FF_DURATION_BUF1[7:0]							
89	137	IMEM_SRAM_APEX_REG_137	FF_DURATION_BUF1[15:8]							
8A	138	IMEM_SRAM_APEX_REG_138	FF_DURATION_BUF2[7:0]							
8B	139	IMEM_SRAM_APEX_REG_139	FF_DURATION_BUF2[15:8]							
8E	142	IMEM_SRAM_APEX_REG_142	TAP_NUM[7:0]							
8F	143	IMEM_SRAM_APEX_REG_143	TAP_AXIS[7:0]							
90	144	IMEM_SRAM_APEX_REG_144	TAP_DIR[7:0]							
91	145	IMEM_SRAM_APEX_REG_145	DOUBLE_TAP_TIMING[7:0]							
92	146	IMEM_SRAM_APEX_REG_146	TRIPLE_TAP_TIMING[7:0]							
93	147	IMEM_SRAM_APEX_REG_147	SHAKE_OUTAXIS[7:0]							
94	148	IMEM_SRAM_APEX_REG_148	NOMOTION_OUTLOCK[7:0]							
95	149	IMEM_SRAM_APEX_REG_149	NOMOTION_MAJORITY_AXIS[7:0]							
96	150	IMEM_SRAM_APEX_REG_150	NOMOTION_SIGN_ANGLE[7:0]							
98	152	IMEM_SRAM_APEX_REG_152	NOMOTION_X_AXIS_REF[7:0]							
99	153	IMEM_SRAM_APEX_REG_153	NOMOTION_X_AXIS_REF[15:8]							
9A	154	IMEM_SRAM_APEX_REG_154	NOMOTION_Y_AXIS_REF[7:0]							
9B	155	IMEM_SRAM_APEX_REG_155	NOMOTION_Y_AXIS_REF[15:8]							
9C	156	IMEM_SRAM_APEX_REG_156	NOMOTION_TILT_ANGLE_RAW_FORMAT[7:0]							
9D	157	IMEM_SRAM_APEX_REG_157	NOMOTION_TILT_ANGLE_RAW_FORMAT[15:8]							
A8	168	IMEM_SRAM_APEX_REG_168	POWER_SAVE_TIME[7:0]							
A9	169	IMEM_SRAM_APEX_REG_169	POWER_SAVE_TIME[15:8]							
AA	170	IMEM_SRAM_APEX_REG_170	POWER_SAVE_TIME[23:16]							
AB	171	IMEM_SRAM_APEX_REG_171	POWER_SAVE_TIME[31:24]							

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BC	188	IMEM_SRAM_APEX_REG_188	FF_MIN_DURATION[7:0]							
BD	189	IMEM_SRAM_APEX_REG_189	FF_MIN_DURATION[15:8]							
BE	190	IMEM_SRAM_APEX_REG_190	FF_MIN_DURATION[23:16]							
BF	191	IMEM_SRAM_APEX_REG_191	FF_MIN_DURATION[31:24]							
C0	192	IMEM_SRAM_APEX_REG_192	FF_MAX_DURATION[7:0]							
C1	193	IMEM_SRAM_APEX_REG_193	FF_MAX_DURATION[15:8]							
C2	194	IMEM_SRAM_APEX_REG_194	FF_MAX_DURATION[23:16]							
C3	195	IMEM_SRAM_APEX_REG_195	FF_MAX_DURATION[31:24]							
C4	196	IMEM_SRAM_APEX_REG_196	FF_DEBOUNCE_DURATION[7:0]							
C5	197	IMEM_SRAM_APEX_REG_197	FF_DEBOUNCE_DURATION[15:8]							
C6	198	IMEM_SRAM_APEX_REG_198	FF_DEBOUNCE_DURATION[23:16]							
C7	199	IMEM_SRAM_APEX_REG_199	FF_DEBOUNCE_DURATION[31:24]							
CE	206	IMEM_SRAM_APEX_REG_206	HIGHG_PEAK_TH[7:0]							
CF	207	IMEM_SRAM_APEX_REG_207	HIGHG_PEAK_TH[15:8]							
D0	208	IMEM_SRAM_APEX_REG_208	HIGHG_PEAK_TH_HYST[7:0]							
D1	209	IMEM_SRAM_APEX_REG_209	HIGHG_PEAK_TH_HYST[15:8]							
D2	210	IMEM_SRAM_APEX_REG_210	HIGHG_TIME_TH[7:0]							
D3	211	IMEM_SRAM_APEX_REG_211	HIGHG_TIME_TH[15:8]							
DA	218	IMEM_SRAM_APEX_REG_218	LOWG_PEAK_TH[7:0]							
DB	219	IMEM_SRAM_APEX_REG_219	LOWG_PEAK_TH[15:8]							
DC	220	IMEM_SRAM_APEX_REG_220	LOWG_PEAK_TH_HYST[7:0]							
DD	221	IMEM_SRAM_APEX_REG_221	LOWG_PEAK_TH_HYST[15:8]							
DE	222	IMEM_SRAM_APEX_REG_222	LOWG_TIME_TH[7:0]							
DF	223	IMEM_SRAM_APEX_REG_223	LOWG_TIME_TH[15:8]							
E4	228	IMEM_SRAM_APEX_REG_228	TAP_TMAX[7:0]							
E5	229	IMEM_SRAM_APEX_REG_229	TAP_TMAX[15:8]							
E6	230	IMEM_SRAM_APEX_REG_230	TAP_TMIN[7:0]							
E7	231	IMEM_SRAM_APEX_REG_231	TAP_MIN_JERK[7:0]							
E8	232	IMEM_SRAM_APEX_REG_232	TAP_SMUDGE_REJECT_THR[7:0]							
E9	233	IMEM_SRAM_APEX_REG_233	TAP_MAX_PEAK_TOL[7:0]							
EA	234	IMEM_SRAM_APEX_REG_234	TAP_TAVG[7:0]							
EC	236	IMEM_SRAM_APEX_REG_236	TAP_MAX_TAP[7:0]							
ED	237	IMEM_SRAM_APEX_REG_237	TAP_MIN_TAP[7:0]							
EE	238	IMEM_SRAM_APEX_REG_238	TAP_MAX_ENERGY_PRIMARY_AXIS[7:0]							
EF	239	IMEM_SRAM_APEX_REG_239	TAP_MAX_ENERGY_PRIMARY_AXIS[15:8]							
F0	240	IMEM_SRAM_APEX_REG_240	TAP_MAX_ENERGY_SECONDARY_AXIS[7:0]							
F1	241	IMEM_SRAM_APEX_REG_241	TAP_MAX_ENERGY_SECONDARY_AXIS[15:8]							
F2	242	IMEM_SRAM_APEX_REG_242	TAP_AXIS_SELECT_MASK[7:0]							
16C	364	IMEM_SRAM_APEX_REG_364	R2W_SLEEP_TIME_OUT[7:0]							
16D	365	IMEM_SRAM_APEX_REG_365	R2W_SLEEP_TIME_OUT[15:8]							
16E	366	IMEM_SRAM_APEX_REG_366	R2W_SLEEP_TIME_OUT[23:16]							
16F	367	IMEM_SRAM_APEX_REG_367	R2W_SLEEP_TIME_OUT[31:24]							
170	368	IMEM_SRAM_APEX_REG_368	R2W_SLEEP_GESTURE_DELAY[7:0]							
171	369	IMEM_SRAM_APEX_REG_369	R2W_SLEEP_GESTURE_DELAY[15:8]							
172	370	IMEM_SRAM_APEX_REG_370	R2W_SLEEP_GESTURE_DELAY[23:16]							
173	371	IMEM_SRAM_APEX_REG_371	R2W_SLEEP_GESTURE_DELAY[31:24]							
174	372	IMEM_SRAM_APEX_REG_372	R2W_MOUNTING_MATRIX[7:0]							
175	373	IMEM_SRAM_APEX_REG_373	R2W_MOUNTING_MATRIX[15:8]							
176	374	IMEM_SRAM_APEX_REG_374	R2W_MOUNTING_MATRIX[23:16]							
177	375	IMEM_SRAM_APEX_REG_375	R2W_MOUNTING_MATRIX[31:24]							
178	376	IMEM_SRAM_APEX_REG_376	R2W_SAMPLING_PERIOD[7:0]							
179	377	IMEM_SRAM_APEX_REG_377	R2W_SAMPLING_PERIOD[15:8]							
17A	378	IMEM_SRAM_APEX_REG_378	R2W_SAMPLING_PERIOD[23:16]							
17B	379	IMEM_SRAM_APEX_REG_379	R2W_SAMPLING_PERIOD[31:24]							
17C	380	IMEM_SRAM_APEX_REG_380	R2W_GRAVITY_FILTER_GAIN[7:0]							
17D	381	IMEM_SRAM_APEX_REG_381	R2W_GRAVITY_FILTER_GAIN[15:8]							

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17E	382	IMEM_SRAM_APEX_REG_382	R2W_GRAVITY_FILTER_GAIN[23:16]							
17F	383	IMEM_SRAM_APEX_REG_383	R2W_GRAVITY_FILTER_GAIN[31:24]							
180	384	IMEM_SRAM_APEX_REG_384	R2W_MOTION_THR_ANGLE_COSINE[7:0]							
181	385	IMEM_SRAM_APEX_REG_385	R2W_MOTION_THR_ANGLE_COSINE[15:8]							
182	386	IMEM_SRAM_APEX_REG_386	R2W_MOTION_THR_ANGLE_COSINE[23:16]							
183	387	IMEM_SRAM_APEX_REG_387	R2W_MOTION_THR_ANGLE_COSINE[31:24]							
184	388	IMEM_SRAM_APEX_REG_388	R2W_MOTION_THR_TIMER_FAST[7:0]							
185	389	IMEM_SRAM_APEX_REG_389	R2W_MOTION_THR_TIMER_FAST[15:8]							
186	390	IMEM_SRAM_APEX_REG_390	R2W_MOTION_THR_TIMER_FAST[23:16]							
187	391	IMEM_SRAM_APEX_REG_391	R2W_MOTION_THR_TIMER_FAST[31:24]							
188	392	IMEM_SRAM_APEX_REG_392	R2W_MOTION_THR_TIMER_SLOW[7:0]							
189	393	IMEM_SRAM_APEX_REG_393	R2W_MOTION_THR_TIMER_SLOW[15:8]							
18A	394	IMEM_SRAM_APEX_REG_394	R2W_MOTION_THR_TIMER_SLOW[23:16]							
18B	395	IMEM_SRAM_APEX_REG_395	R2W_MOTION_THR_TIMER_SLOW[31:24]							
18C	396	IMEM_SRAM_APEX_REG_396	R2W_MOTION_PREV_GRAVITY_TIMEOUT[7:0]							
18D	397	IMEM_SRAM_APEX_REG_397	R2W_MOTION_PREV_GRAVITY_TIMEOUT[15:8]							
18E	398	IMEM_SRAM_APEX_REG_398	R2W_MOTION_PREV_GRAVITY_TIMEOUT[23:16]							
18F	399	IMEM_SRAM_APEX_REG_399	R2W_MOTION_PREV_GRAVITY_TIMEOUT[31:24]							
190	400	IMEM_SRAM_APEX_REG_400	R2W_LAST_GRAVITY_MOTION_TIMER[7:0]							
191	401	IMEM_SRAM_APEX_REG_401	R2W_LAST_GRAVITY_MOTION_TIMER[15:8]							
192	402	IMEM_SRAM_APEX_REG_402	R2W_LAST_GRAVITY_MOTION_TIMER[23:16]							
193	403	IMEM_SRAM_APEX_REG_403	R2W_LAST_GRAVITY_MOTION_TIMER[31:24]							
194	404	IMEM_SRAM_APEX_REG_404	R2W_LAST_GRAVITY_TIMEOUT[7:0]							
195	405	IMEM_SRAM_APEX_REG_405	R2W_LAST_GRAVITY_TIMEOUT[15:8]							
196	406	IMEM_SRAM_APEX_REG_406	R2W_LAST_GRAVITY_TIMEOUT[23:16]							
197	407	IMEM_SRAM_APEX_REG_407	R2W_LAST_GRAVITY_TIMEOUT[31:24]							
198	408	IMEM_SRAM_APEX_REG_408	R2W_GESTURE_VALIDITY_TIMEOUT[7:0]							
199	409	IMEM_SRAM_APEX_REG_409	R2W_GESTURE_VALIDITY_TIMEOUT[15:8]							
19A	410	IMEM_SRAM_APEX_REG_410	R2W_GESTURE_VALIDITY_TIMEOUT[23:16]							
19B	411	IMEM_SRAM_APEX_REG_411	R2W_GESTURE_VALIDITY_TIMEOUT[31:24]							
1EC	492	IMEM_SRAM_APEX_REG_492	THREEAXIS_ACCEL_ONLY_GAIN[7:0]							
1ED	493	IMEM_SRAM_APEX_REG_493	THREEAXIS_ACCEL_ONLY_GAIN[15:8]							
1EE	494	IMEM_SRAM_APEX_REG_494	THREEAXIS_ACCEL_ONLY_GAIN[23:16]							
1EF	495	IMEM_SRAM_APEX_REG_495	THREEAXIS_ACCEL_ONLY_GAIN[31:24]							
214	532	IMEM_SRAM_APEX_REG_532	TILT_WAIT_TIME[7:0]							
215	533	IMEM_SRAM_APEX_REG_533	TILT_WAIT_TIME[15:8]							
218	536	IMEM_SRAM_APEX_REG_536	TILT_ANGLE_TH[7:0]							
219	537	IMEM_SRAM_APEX_REG_537	TILT_ANGLE_TH[15:8]							
21A	538	IMEM_SRAM_APEX_REG_538	TILT_ANGLE_TH[23:16]							
21B	539	IMEM_SRAM_APEX_REG_539	TILT_ANGLE_TH[31:24]							
2FC	764	IMEM_SRAM_APEX_REG_764	PED_PREV_STEP_CNT_TH[7:0]							
2FD	765	IMEM_SRAM_APEX_REG_765	PED_PREV_STEP_CNT_TH[15:8]							
37E	894	IMEM_SRAM_APEX_REG_894	PED_STEP_CNT_TH[7:0]							
37F	895	IMEM_SRAM_APEX_REG_895	PED_STEP_CNT_TH[15:8]							
380	896	IMEM_SRAM_APEX_REG_896	PED_STEP_DET_TH[7:0]							
381	897	IMEM_SRAM_APEX_REG_897	PED_STEP_DET_TH[15:8]							
382	898	IMEM_SRAM_APEX_REG_898	PED_SB_TIMER_TH[7:0]							
383	899	IMEM_SRAM_APEX_REG_899	PED_SB_TIMER_TH[15:8]							
384	900	IMEM_SRAM_APEX_REG_900	PED_LOW_EN_AMP_TH[7:0]							
385	901	IMEM_SRAM_APEX_REG_901	PED_LOW_EN_AMP_TH[15:8]							
386	902	IMEM_SRAM_APEX_REG_902	PED_LOW_EN_AMP_TH[23:16]							
387	903	IMEM_SRAM_APEX_REG_903	PED_LOW_EN_AMP_TH[31:24]							
388	904	IMEM_SRAM_APEX_REG_904	PED_AMP_TH[7:0]							
389	905	IMEM_SRAM_APEX_REG_905	PED_AMP_TH[15:8]							
38A	906	IMEM_SRAM_APEX_REG_906	PED_AMP_TH[23:16]							
38B	907	IMEM_SRAM_APEX_REG_907	PED_AMP_TH[31:24]							

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38C	908	IMEM_SRAM_APEX_REG_908	PED_HI_EN_TH[7:0]							
38D	909	IMEM_SRAM_APEX_REG_909	PED_HI_EN_TH[15:8]							
38E	910	IMEM_SRAM_APEX_REG_910	PED_HI_EN_TH[23:16]							
38F	911	IMEM_SRAM_APEX_REG_911	PED_HI_EN_TH[31:24]							
390	912	IMEM_SRAM_APEX_REG_912	PED_SENSITIVITY_MODE[7:0]							
3AA	938	IMEM_SRAM_APEX_REG_938	SMD_SENSITIVITY[7:0]							
42C	1068	IMEM_SRAM_APEX_REG_1068	B2S_MOUNTING_MATRIX[7:0]							
430	1072	IMEM_SRAM_APEX_REG_1072	B2S_DEV_NORM_MAX[7:0]							
431	1073	IMEM_SRAM_APEX_REG_1073	B2S_DEV_NORM_MAX[15:8]							
432	1074	IMEM_SRAM_APEX_REG_1074	B2S_DEV_NORM_MAX[23:16]							
433	1075	IMEM_SRAM_APEX_REG_1075	B2S_DEV_NORM_MAX[31:24]							
434	1076	IMEM_SRAM_APEX_REG_1076	B2S_SIN_LIMIT[7:0]							
435	1077	IMEM_SRAM_APEX_REG_1077	B2S_SIN_LIMIT[15:8]							
436	1078	IMEM_SRAM_APEX_REG_1078	B2S_SIN_LIMIT[23:16]							
437	1079	IMEM_SRAM_APEX_REG_1079	B2S_SIN_LIMIT[31:24]							
438	1080	IMEM_SRAM_APEX_REG_1080	B2S_FAST_MOTION_AGE_LIMIT[7:0]							
439	1081	IMEM_SRAM_APEX_REG_1081	B2S_FAST_MOTION_AGE_LIMIT[15:8]							
43A	1082	IMEM_SRAM_APEX_REG_1082	B2S_FAST_MOTION_AGE_LIMIT[23:16]							
43B	1083	IMEM_SRAM_APEX_REG_1083	B2S_FAST_MOTION_AGE_LIMIT[31:24]							
43C	1084	IMEM_SRAM_APEX_REG_1084	B2S_FAST_LIMIT[7:0]							
43D	1085	IMEM_SRAM_APEX_REG_1085	B2S_FAST_LIMIT[15:8]							
43E	1086	IMEM_SRAM_APEX_REG_1086	B2S_FAST_LIMIT[23:16]							
43F	1087	IMEM_SRAM_APEX_REG_1087	B2S_FAST_LIMIT[31:24]							
440	1088	IMEM_SRAM_APEX_REG_1088	B2S_FAST_MOTION_TIME_LIMIT[7:0]							
441	1089	IMEM_SRAM_APEX_REG_1089	B2S_FAST_MOTION_TIME_LIMIT[15:8]							
442	1090	IMEM_SRAM_APEX_REG_1090	B2S_FAST_MOTION_TIME_LIMIT[23:16]							
443	1091	IMEM_SRAM_APEX_REG_1091	B2S_FAST_MOTION_TIME_LIMIT[31:24]							
444	1092	IMEM_SRAM_APEX_REG_1092	B2S_AGE_LIMIT[7:0]							
445	1093	IMEM_SRAM_APEX_REG_1093	B2S_AGE_LIMIT[15:8]							
446	1094	IMEM_SRAM_APEX_REG_1094	B2S_AGE_LIMIT[23:16]							
447	1095	IMEM_SRAM_APEX_REG_1095	B2S_AGE_LIMIT[31:24]							
448	1096	IMEM_SRAM_APEX_REG_1096	B2S_STATIC_LIMIT[7:0]							
449	1097	IMEM_SRAM_APEX_REG_1097	B2S_STATIC_LIMIT[15:8]							
44A	1098	IMEM_SRAM_APEX_REG_1098	B2S_STATIC_LIMIT[23:16]							
44B	1099	IMEM_SRAM_APEX_REG_1099	B2S_STATIC_LIMIT[31:24]							
44C	1100	IMEM_SRAM_APEX_REG_1100	B2S_THR_COS_ANGLE[7:0]							
44D	1101	IMEM_SRAM_APEX_REG_1101	B2S_THR_COS_ANGLE[15:8]							
44E	1102	IMEM_SRAM_APEX_REG_1102	B2S_THR_COS_ANGLE[23:16]							
44F	1103	IMEM_SRAM_APEX_REG_1103	B2S_THR_COS_ANGLE[31:24]							
450	1104	IMEM_SRAM_APEX_REG_1104	B2S_REVB2S_LATENCY_THR[7:0]							
451	1105	IMEM_SRAM_APEX_REG_1105	B2S_REVB2S_LATENCY_THR[15:8]							
452	1106	IMEM_SRAM_APEX_REG_1106	B2S_REVB2S_LATENCY_THR[23:16]							
453	1107	IMEM_SRAM_APEX_REG_1107	B2S_REVB2S_LATENCY_THR[31:24]							
500	1280	IMEM_SRAM_APEX_REG_1280	SHAKE_AXIS_MAJORITY_TH[7:0]							
501	1281	IMEM_SRAM_APEX_REG_1281	SHAKE_AXIS_MAJORITY_TH[15:8]							
502	1282	IMEM_SRAM_APEX_REG_1282	SHAKE_THR_STATIC[7:0]							
503	1283	IMEM_SRAM_APEX_REG_1283	SHAKE_THR_STATIC[15:8]							
504	1284	IMEM_SRAM_APEX_REG_1284	SHAKE_MIN_STATIC_DURATION[7:0]							
505	1285	IMEM_SRAM_APEX_REG_1285	SHAKE_MIN_STATIC_DURATION[15:8]							
506	1286	IMEM_SRAM_APEX_REG_1286	SHAKE_THR_MOTION[7:0]							
507	1287	IMEM_SRAM_APEX_REG_1287	SHAKE_THR_MOTION[15:8]							
508	1288	IMEM_SRAM_APEX_REG_1288	SHAKE_THR_SHAKE_X[7:0]							
509	1289	IMEM_SRAM_APEX_REG_1289	SHAKE_THR_SHAKE_X[15:8]							
50A	1290	IMEM_SRAM_APEX_REG_1290	SHAKE_THR_SHAKE_Y[7:0]							
50B	1291	IMEM_SRAM_APEX_REG_1291	SHAKE_THR_SHAKE_Y[15:8]							
50C	1292	IMEM_SRAM_APEX_REG_1292	SHAKE_THR_SHAKE_Z[7:0]							

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50D	1293	IMEM_SRAM_APEX_REG_1293	SHAKE_THR_SHAKE_Z[15:8]							
50E	1294	IMEM_SRAM_APEX_REG_1294	SHAKE_MIN_SHAKE_DURATION[7:0]							
50F	1295	IMEM_SRAM_APEX_REG_1295	SHAKE_MIN_SHAKE_DURATION[15:8]							
510	1296	IMEM_SRAM_APEX_REG_1296	SHAKE_MAX_SHAKE_DURATION[7:0]							
511	1297	IMEM_SRAM_APEX_REG_1297	SHAKE_MAX_SHAKE_DURATION[15:8]							
512	1298	IMEM_SRAM_APEX_REG_1298	SHAKE_INTERNAL_DURATION[7:0]							
513	1299	IMEM_SRAM_APEX_REG_1299	SHAKE_INTERNAL_DURATION[15:8]							
514	1300	IMEM_SRAM_APEX_REG_1300	SHAKE_AXIS_DETECTION_FACTOR[7:0]							
515	1301	IMEM_SRAM_APEX_REG_1301	SHAKE_AXIS_DETECTION_FACTOR[15:8]							
522	1314	IMEM_SRAM_APEX_REG_1314	NOMOTION_THR_STATIC[7:0]							
523	1315	IMEM_SRAM_APEX_REG_1315	NOMOTION_THR_STATIC[15:8]							
524	1316	IMEM_SRAM_APEX_REG_1316	NOMOTION_MIN_STATIC_DURATION[7:0]							
525	1317	IMEM_SRAM_APEX_REG_1317	NOMOTION_MIN_STATIC_DURATION[15:8]							
526	1318	IMEM_SRAM_APEX_REG_1318	NOMOTION_THR_MOTION[7:0]							
527	1319	IMEM_SRAM_APEX_REG_1319	NOMOTION_THR_MOTION[15:8]							
554	1364	IMEM_SRAM_APEX_REG_1364	ACCEL_ONLY_GAIN_FAST_CONV[7:0]							
555	1365	IMEM_SRAM_APEX_REG_1365	ACCEL_ONLY_GAIN_FAST_CONV[15:8]							
556	1366	IMEM_SRAM_APEX_REG_1366	ACCEL_ONLY_GAIN_FAST_CONV[23:16]							
557	1367	IMEM_SRAM_APEX_REG_1367	ACCEL_ONLY_GAIN_FAST_CONV[31:24]							
574	1396	IMEM_SRAM_APEX_REG_1396	FLAT_REF_AXIS_SELECTION[7:0]							
575	1397	IMEM_SRAM_APEX_REG_1397	FLAT_REF_AXIS_SELECTION[15:8]							
576	1398	IMEM_SRAM_APEX_REG_1398	FLAT_ISSYMETRICAL[7:0]							
577	1399	IMEM_SRAM_APEX_REG_1399	FLAT_ISSYMETRICAL[15:8]							
578	1400	IMEM_SRAM_APEX_REG_1400	FLAT_THREE_AXIS_CONV_TIME[7:0]							
579	1401	IMEM_SRAM_APEX_REG_1401	FLAT_THREE_AXIS_CONV_TIME[15:8]							
57A	1402	IMEM_SRAM_APEX_REG_1402	FLAT_WAIT_TIME[7:0]							
57B	1403	IMEM_SRAM_APEX_REG_1403	FLAT_WAIT_TIME[15:8]							
57C	1404	IMEM_SRAM_APEX_REG_1404	FLAT_COS_FLAT_ANGLE_TH[7:0]							
57D	1405	IMEM_SRAM_APEX_REG_1405	FLAT_COS_FLAT_ANGLE_TH[15:8]							
57E	1406	IMEM_SRAM_APEX_REG_1406	FLAT_COS_FLAT_ANGLE_TH[23:16]							
57F	1407	IMEM_SRAM_APEX_REG_1407	FLAT_COS_FLAT_ANGLE_TH[31:24]							
580	1408	IMEM_SRAM_APEX_REG_1408	FLAT_REF_AXIS_X[7:0]							
581	1409	IMEM_SRAM_APEX_REG_1409	FLAT_REF_AXIS_X[15:8]							
582	1410	IMEM_SRAM_APEX_REG_1410	FLAT_REF_AXIS_X[23:16]							
583	1411	IMEM_SRAM_APEX_REG_1411	FLAT_REF_AXIS_X[31:24]							
584	1412	IMEM_SRAM_APEX_REG_1412	FLAT_REF_AXIS_Y[7:0]							
585	1413	IMEM_SRAM_APEX_REG_1413	FLAT_REF_AXIS_Y[15:8]							
586	1414	IMEM_SRAM_APEX_REG_1414	FLAT_REF_AXIS_Y[23:16]							
587	1415	IMEM_SRAM_APEX_REG_1415	FLAT_REF_AXIS_Y[31:24]							
588	1416	IMEM_SRAM_APEX_REG_1416	FLAT_REF_AXIS_Z[7:0]							
589	1417	IMEM_SRAM_APEX_REG_1417	FLAT_REF_AXIS_Z[15:8]							
58A	1418	IMEM_SRAM_APEX_REG_1418	FLAT_REF_AXIS_Z[23:16]							
58B	1419	IMEM_SRAM_APEX_REG_1419	FLAT_REF_AXIS_Z[31:24]							

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14.5 USER BANK IMEM_SRAM_STC REGISTER MAP

Addr (Hex)	Addr (Dec.)	RegisteMr Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	IMEM_SRAM_STC_REG_56	STC_CONFIGPARAMS[7:0]							
39	57	IMEM_SRAM_STC_REG_57	STC_CONFIGPARAMS[15:8]							
3C	60	IMEM_SRAM_STC_REG_60	STC_PATCH_EN[7:0]							
40	64	IMEM_SRAM_STC_REG_64	STC_DEBUG_EN[7:0]							
41	65	IMEM_SRAM_STC_REG_65	STC_DEBUG_EN[15:8]							
42	66	IMEM_SRAM_STC_REG_66	STC_DEBUG_EN[23:16]							
43	67	IMEM_SRAM_STC_REG_67	STC_DEBUG_EN[31:24]							
44	68	IMEM_SRAM_STC_REG_68	STC_RESULTS[7:0]							

14.6 USER BANK IPREG_SYS1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	IPREG_SYS1_REG_0	SIGP_DATA_INJ_TMP[7:0]							
01	01	IPREG_SYS1_REG_1	SIGP_DATA_INJ_TMP[15:8]							
02	02	IPREG_SYS1_REG_2	GYRO_X_OFFUSER[7:0]							
03	03	IPREG_SYS1_REG_3	-		GYRO_X_OFFUSER[13:8]					
04	04	IPREG_SYS1_REG_4	GYRO_Y_OFFUSER[7:0]							
05	05	IPREG_SYS1_REG_5	-		GYRO_Y_OFFUSER[13:8]					
06	06	IPREG_SYS1_REG_6	GYRO_Z_OFFUSER[7:0]							
07	07	IPREG_SYS1_REG_7	-		GYRO_Z_OFFUSER[13:8]					
08	08	IPREG_SYS1_REG_8	GYRO_X_USERGAIN[7:0]							
09	09	IPREG_SYS1_REG_9	-				GYRO_X_USERGAIN[11:8]			
0A	10	IPREG_SYS1_REG_10	GYRO_Y_USERGAIN[7:0]							
0B	11	IPREG_SYS1_REG_11	-				GYRO_Y_USERGAIN[11:8]			
0C	12	IPREG_SYS1_REG_12	GYRO_Z_USERGAIN[7:0]							
0D	13	IPREG_SYS1_REG_13	-				GYRO_Z_USERGAIN[11:8]			
92	146	IPREG_SYS1_REG_146	GYRO_X_TMID_OFF[3:0]				GYRO_X_TMID_GAIN[3:0]			
94	148	IPREG_SYS1_REG_148	GYRO_Y_TMID_OFF[3:0]				GYRO_Y_TMID_GAIN[3:0]			
96	150	IPREG_SYS1_REG_150	GYRO_Z_TMID_OFF[3:0]				GYRO_Z_TMID_GAIN[3:0]			
9A	154	IPREG_SYS1_REG_154	-		GYRO_OIS_M6_BYP[0]	GYRO_AFSR_SHARED[0]	GYRO_SRC_CTRL[1:0]		-	GYRO_AFSR_ENABLE[0]
9B	155	IPREG_SYS1_REG_155	-						GYRO_LPF_BYPASS[0]	GYRO_OIS_HPF_BYP[0]
9D	157	IPREG_SYS1_REG_157	GYRO_NOTCH_BYPASS[0]	GYRO_OIS_HPFBW_SEL[2:0]			GYRO_LP_AVG_SEL[3:0]			
9E	158	IPREG_SYS1_REG_158	GYRO_UI_3RD_ORD_SEL[0]	GYRO_UI_LPFBW_SEL[2:0]			GYRO_OIS_3RD_ORD_SEL[0]	GYRO_OIS_LPFBW_SEL[2:0]		

14.7 USER BANK IPREG_SYS2 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0C	12	IPREG_SYS2_REG_12	ACCEL_X_OFFUSER[7:0]							
0D	13	IPREG_SYS2_REG_13	-		ACCEL_X_OFFUSER[13:8]					
0E	14	IPREG_SYS2_REG_14	ACCEL_Y_OFFUSER[7:0]							
0F	15	IPREG_SYS2_REG_15	-		ACCEL_Y_OFFUSER[13:8]					
10	16	IPREG_SYS2_REG_16	ACCEL_Z_OFFUSER[7:0]							
11	17	IPREG_SYS2_REG_17	-		ACCEL_Z_OFFUSER[13:8]					
12	18	IPREG_SYS2_REG_18	ACCEL_X_USERGAIN[7:0]							
13	19	IPREG_SYS2_REG_19	-				ACCEL_X_USERGAIN[11:8]			
14	20	IPREG_SYS2_REG_20	ACCEL_Y_USERGAIN[7:0]							
15	21	IPREG_SYS2_REG_21	-				ACCEL_Y_USERGAIN[11:8]			
16	22	IPREG_SYS2_REG_22	ACCEL_Z_USERGAIN[7:0]							

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Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17	23	IPREG_SYS2_REG_23	-				ACCEL_Z_USERGAIN[11:8]			
69	105	IPREG_SYS2_REG_105	ACCEL_X_TMID_OFF[3:0]				ACCEL_X_TMID_GAIN[3:0]			
6A	106	IPREG_SYS2_REG_106	ACCEL_Y_TMID_OFF[3:0]				ACCEL_Y_TMID_GAIN[3:0]			
6B	107	IPREG_SYS2_REG_107	ACCEL_Z_TMID_OFF[3:0]				ACCEL_Z_TMID_GAIN[3:0]			
6D	109	IPREG_SYS2_REG_109	-						ACCEL_SRC_CTRL[1:0]	
6E	110	IPREG_SYS2_REG_110	-	ACCEL_OIS_HPFBW_SEL[2:0]			ACCEL_LP_AVG_SEL[3:0]			
6F	111	IPREG_SYS2_REG_111	-				ACCEL_OIS_3RD_ORD_SEL[0]	ACCEL_OIS_LPFBW_SEL[2:0]		
70	112	IPREG_SYS2_REG_112	-	ACCEL_OIS_M6_BYP[0]	ACCEL_OIS_HPF_BYP[0]	ACCEL_LPF_BYPASS[0]	ACCEL_UI_3RD_ORD_SEL[0]	ACCEL_UI_LPFBW_SEL[2:0]		
75	117	IPREG_SYS2_REG_117	-	TMP_DEC_CFG[2:0]			TMP_LPF_CFG[2:0]			TMP_INJ_EN_GOS[0]

14.8 USER BANK IPREG_TOP1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4F	79	EDMP_PRGRM_IRQ0_0	PRGRM_STRT_ADDR_IRQ_0[7:0]							
50	80	EDMP_PRGRM_IRQ0_1	PRGRM_STRT_ADDR_IRQ_0[15:8]							
51	81	EDMP_PRGRM_IRQ1_0	PRGRM_STRT_ADDR_IRQ_1[7:0]							
52	82	EDMP_PRGRM_IRQ1_1	PRGRM_STRT_ADDR_IRQ_1[15:8]							
53	83	EDMP_PRGRM_IRQ2_0	PRGRM_STRT_ADDR_IRQ_2[7:0]							
54	84	EDMP_PRGRM_IRQ2_1	PRGRM_STRT_ADDR_IRQ_2[15:8]							
55	85	EDMP_SP_START_ADDR	SP_START_ADDR[7:0]							
58	88	SMC_CONTROL_0	-					TMST_FORCE_AUX_FINE_EN[0]	TMST_FSYNC_EN[0]	TMST_EN[0]
60	96	SREG_CTRL	-				SREG_SIFS_20BITS_EN[0]	-	SREG_DATA_ENDIAN_SEL[0]	-
62	98	INT_PULSE_MIN_ON_INTF0	-					INT0_TPULSE_DURATION[2:0]		
63	99	INT_PULSE_MIN_ON_INTF1	-					INT1_TPULSE_DURATION[2:0]		
64	100	INT_PULSE_MIN_OFF_INTF0	-					INT0_TDEASSERT_DISABLE[2:0]		
65	101	INT_PULSE_MIN_OFF_INTF1	-					INT1_TDEASSERT_DISABLE[2:0]		
6A	106	STATUS_MASK_PIN_0_7	-		INT_ON_DEMAND_PIN_0_DIS[0]	INT_WOM_DRDY_PIN_0_DIS[0]	-		INT_GYRO_DRDY_PIN_0_DIS[0]	INT_ACCEL_DRDY_PIN_0_DIS[0]
6B	107	STATUS_MASK_PIN_8_15	-		INT_ON_DEMAND_PIN_1_DIS[0]	INT_WOM_DRDY_PIN_1_DIS[0]	-		INT_GYRO_DRDY_PIN_1_DIS[0]	INT_ACCEL_DRDY_PIN_1_DIS[0]
6C	108	STATUS_MASK_PIN_16_23	-		INT_ON_DEMAND_PIN_2_DIS[0]	INT_WOM_DRDY_PIN_2_DIS[0]	-		INT_GYRO_DRDY_PIN_2_DIS[0]	INT_ACCEL_DRDY_PIN_2_DIS[0]
77	119	ACCEL_WOM_X_THR	WOM_X_TH[7:0]							
78	120	ACCEL_WOM_Y_THR	WOM_Y_TH[7:0]							
79	121	ACCEL_WOM_Z_THR	WOM_Z_TH[7:0]							
7D	125	IOC_PADS_CONFIG0	-		FSYNC_POLARITY[0]	-				
82	130	IREG_OTP_CFG	-						OTP_COPY_MODE[1:0]	
89	137	SELFTEST	-		EN_GZ_ST[0]	EN_GY_ST[0]	EN_GX_ST[0]	EN_AZ_ST[0]	EN_AY_ST[0]	EN_AX_ST[0]
90	144	IPREG_MISC	-						EDMP_IDLE[0]	-
A1	161	SW_RCOSC1_TRIM	SW_RCOSC1_TRIM[7:0]							
A2	162	SW_PLL1_TRIM	SW_PLL1_TRIM[7:0]							
A7	167	FIFO_SRAM_SLEEP	-							FIFO_GSLEEP_SHARED_SRAM[0]

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14.9 USER BANK DREG_BANK1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	ACCEL_DATA_X_0	ACCEL_DATA_X_AP[15:8]							
01	01	ACCEL_DATA_X_1	ACCEL_DATA_X_AP[7:0]							
02	02	ACCEL_DATA_Y_0	ACCEL_DATA_Y_AP[15:8]							
03	03	ACCEL_DATA_Y_1	ACCEL_DATA_Y_AP[7:0]							
04	04	ACCEL_DATA_Z_0	ACCEL_DATA_Z_AP[15:8]							
05	05	ACCEL_DATA_Z_1	ACCEL_DATA_Z_AP[7:0]							
06	06	GYRO_DATA_X_0	GYRO_DATA_X_AP[15:8]							
07	07	GYRO_DATA_X_1	GYRO_DATA_X_AP[7:0]							
08	08	GYRO_DATA_Y_0	GYRO_DATA_Y_AP[15:8]							
09	09	GYRO_DATA_Y_1	GYRO_DATA_Y_AP[7:0]							
0A	10	GYRO_DATA_Z_0	GYRO_DATA_Z_AP[15:8]							
0B	11	GYRO_DATA_Z_1	GYRO_DATA_Z_AP[7:0]							
0C	12	TEMP_DATA_0	TEMP_DATA_AP[15:8]							
0D	13	TEMP_DATA_1	TEMP_DATA_AP[7:0]							
0E	14	TMST_FSYNC_DATA_0	TMST_FSYNC_DATA_AP[15:8]							
0F	15	TMST_FSYNC_DATA_1	TMST_FSYNC_DATA_AP[7:0]							
10	16	EXT_DATA_X	EXT_ACCEL_DATA_X_AP[3:0]				EXT_GYRO_DATA_X_AP[3:0]			
11	17	EXT_DATA_Y	EXT_ACCEL_DATA_Y_AP[3:0]				EXT_GYRO_DATA_Y_AP[3:0]			
12	18	EXT_DATA_Z	EXT_ACCEL_DATA_Z_AP[3:0]				EXT_GYRO_DATA_Z_AP[3:0]			
14	20	PWR_MGMT0	-		ACCEL_LP_CLK_SEL[0]	-	GYRO_MODE[1:0]		ACCEL_MODE[1:0]	
16	22	FIFO_COUNT_0	FIFO_DATA_CNT[15:8]							
17	23	FIFO_COUNT_1	FIFO_DATA_CNT[7:0]							
18	24	FIFO_DATA	FIFO_RDATA[7:0]							
1A	26	INT1_CONFIG0	INT1_STATUS_EN_RESET_DONE[0]	INT1_STATUS_EN_AUX1_AGC_RDY[0]	INT1_STATUS_EN_AP_AGC_RDY[0]	INT1_STATUS_EN_AP_FSYNC[0]	INT1_STATUS_EN_AUX1_DRDY[0]	INT1_STATUS_EN_DRDY[0]	INT1_STATUS_EN_FIFO_THS[0]	INT1_STATUS_EN_FIFO_FULL[0]
1B	27	INT1_CONFIG1	-	INT1_STATUS_EN_APEX_EVENT[0]	-	INT1_STATUS_EN_I3C_PROTOCOL_ERR[0]	INT1_STATUS_EN_WOM_Z[0]	INT1_STATUS_EN_WOM_Y[0]	INT1_STATUS_EN_WOM_X[0]	INT1_STATUS_EN_PLL_RDY[0]
1C	28	INT1_CONFIG2	-					INT1_DRIVE[0]	INT1_MODE[0]	INT1_POLARITY[0]
1D	29	INT1_STATUS0	INT1_STATUS_RESET_DONE[0]	INT1_STATUS_AUX1_AGC_RDY[0]	INT1_STATUS_AP_AGC_RDY[0]	INT1_STATUS_AP_FSYNC[0]	INT1_STATUS_AUX1_DRDY[0]	INT1_STATUS_DRDY[0]	INT1_STATUS_FIFO_THS[0]	INT1_STATUS_FIFO_FULL[0]
1E	30	INT1_STATUS1	-	INT1_STATUS_APEX_EVENT[0]	-	INT1_STATUS_I3C_PROTOCOL_ERR[0]	INT1_STATUS_WOM_Z[0]	INT1_STATUS_WOM_Y[0]	INT1_STATUS_WOM_X[0]	INT1_STATUS_PLL_RDY[0]
1F	31	ACCEL_CONFIG0	-	AP_ACCEL_FS_SEL[2:0]			ACCEL_ODR[3:0]			
20	32	GYRO_CONFIG0	AP_GYRO_FS_SEL[3:0]				GYRO_ODR[3:0]			
21	33	FIFO_CONFIG0	FIFO_MODE[1:0]		FIFO_DEPTH[5:0]					
22	34	FIFO_CONFIG1_0	FIFO_WM_TH[7:0]							
23	35	FIFO_CONFIG1_1	FIFO_WM_TH[15:8]							
24	36	FIFO_CONFIG2	FIFO_FLUSH[0]	-		FIFO_INT_OVFL[0]	FIFO_WR_WM_GT_TH[0]	-		
25	37	FIFO_CONFIG3	-				FIFO_HIRES_EN[0]	FIFO_GYRO_EN[0]	FIFO_ACCEL_EN[0]	FIFO_IF_EN[0]
26	38	FIFO_CONFIG4	-			FIFO_COMP_NC_FLOW_CFG[2:0]			FIFO_COMP_EN[0]	FIFO_TMST_FSYNC_EN[0]
27	39	TMST_WOM_CONFIG	-	TMST_DELTA_EN[0]	TMST_RESOL[0]	WOM_EN[0]	WOM_MODE[0]	WOM_INT_MODE[0]	WOM_INT_DUR[1:0]	
28	40	FSYNC_CONFIG0	-				AP_FSYNC_FLAG_CLEAR_SEL[0]	AP_FSYNC_SEL[2:0]		
29	41	FSYNC_CONFIG1	-				AUX1_FSYNC_FLAG_CLEAR_SEL[0]	AUX1_FSYNC_SEL[2:0]		
2A	42	RTC_CONFIG	-	RTC_ALIGN[0]	RTC_MODE[0]	-				
2B	43	DMP_EXT_SEN_ODR_CFG	-					APEX_ODR[2:0]		

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2C	44	ODR_DECIMATE_CONFIG	GYRO_FIFO_ODR_DEC[3:0]				ACCEL_FIFO_ODR_DEC[3:0]			
2D	45	EDMP_APEX_EN0	SMD_EN[0]	R2W_EN[0]	FF_EN[0]	PEDO_EN[0]	TILT_EN[0]	SHAKE_EN[0]	NOMOTION_EN[0]	TAP_EN[0]
2E	46	EDMP_APEX_EN1	-	EDMP_ENABLE[0]	B2S_EN[0]	RESERVED2[0]	RESERVED1[0]	POWER_SAVE_EN[0]	INIT_EN[0]	FLAT_EN[0]
2F	47	APEX_BUFFER_MGMT	FF_DURATION_HOST_RPTR[1:0]		FF_DURATION_EDMP_WPTR[1:0]		STEP_COUNT_HOST_RPTR[1:0]		STEP_COUNT_EDMP_WPTR[1:0]	
30	48	INTF_CONFIG0	-		VIRTUAL_ACCESS_AUX1_EN	-			AP_SPI_34_MODE[0]	AP_SPI_MODE[0]
31	49	INTF_CONFIG1_OVRD	-				AP_SPI_34_MODE_OVRD[0]	AP_SPI_34_MODE_OVRD_VAL[0]	AP_SPI_MODE_OVRD[0]	AP_SPI_MODE_OVRD_VAL[0]
32	50	INTF_AUX_CONFIG	-						AUX1_SPI_34_MODE[0]	AUX1_SPI_MODE[0]
35	53	IOC_PAD_SCENARIO_OVRD	-					PADS_INT2_CFG_OVRD[0]	PADS_INT2_CFG_OVRD_VAL[1:0]	
36	54	DRIVE_CONFIG0	-		PADS_I2C_SLEW[2:0]			PADS_SPI_SLEW[2:0]		
38	56	DRIVE_CONFIG2	-					PADS_SLEW[2:0]		
3D	61	INT_APEX_CONFIG0	INT_STATUS_MASK_PIN_R2W_WAKE_DET[0]	INT_STATUS_MASK_PIN_FF_DET[0]	INT_STATUS_MASK_PIN_STEP_DET[0]	INT_STATUS_MASK_PIN_STEP_CNT_OVFL[0]	INT_STATUS_MASK_PIN_TILT_DET[0]	INT_STATUS_MASK_PIN_LOW_G_DET[0]	INT_STATUS_MASK_PIN_HIGH_G_DET[0]	INT_STATUS_MASK_PIN_TAP_DETECT[0]
3E	62	INT_APEX_CONFIG1	INT_STATUS_MASK_PIN_REVB2S_DET[0]	INT_STATUS_MASK_PIN_B2S_DET[0]	INT_STATUS_MASK_PIN_SHAKE_DET[0]	INT_STATUS_MASK_PIN_SA_DONE[0]	-	INT_STATUS_MASK_PIN_SELFTEST_DONE[0]	INT_STATUS_MASK_PIN_SMD_DET[0]	INT_STATUS_MASK_PIN_R2W_SLEEP_DET[0]
3F	63	INT_APEX_CONFIG2	-				INT_STATUS_MASK_PIN_FLAT_DET[0]	INT_STATUS_MASK_PIN_NOFLAT_DET[0]	INT_STATUS_MASK_PIN_MOTION_DET[0]	INT_STATUS_MASK_PIN_NOMOTION_DET[0]
40	64	INT_APEX_STATUS0	INT_STATUS_R2W_WAKE_DET[0]	INT_STATUS_FF_DET[0]	INT_STATUS_STEP_DET[0]	INT_STATUS_STEP_CNT_OVFL[0]	INT_STATUS_TILT_DET[0]	INT_STATUS_LOW_G_DET[0]	INT_STATUS_HIGH_G_DET[0]	INT_STATUS_TAP_DETECT[0]
41	65	INT_APEX_STATUS1	INT_STATUS_REVB2S_DET[0]	INT_STATUS_B2S_DET[0]	INT_STATUS_SHAKE_DET[0]	INT_STATUS_SA_DONE[0]	-	INT_STATUS_SELFTEST_DONE[0]	INT_STATUS_SMD_DET[0]	INT_STATUS_R2W_SLEEP_DET[0]
42	66	INT_APEX_STATUS2	-				INT_STATUS_FLAT_DET[0]	INT_STATUS_NOFLAT_DET[0]	INT_STATUS_MOTION_DET[0]	INT_STATUS_NOMOTION_DET[0]
46	70	INTF_CONFIG_OVRD_AUX1	-				AUX1_SPI_34_MODE_OVRD[0]	AUX1_SPI_34_MODE_OVRD_VAL[0]	AUX1_SPI_MODE_OVRD[0]	AUX1_SPI_MODE_OVRD_VAL[0]
48	72	ACCEL_DATA_X_AUX1_0	ACCEL_DATA_X_AUX1[15:8]							
49	73	ACCEL_DATA_X_AUX1_1	ACCEL_DATA_X_AUX1[7:0]							
4A	74	ACCEL_DATA_Y_AUX1_0	ACCEL_DATA_Y_AUX1[15:8]							
4B	75	ACCEL_DATA_Y_AUX1_1	ACCEL_DATA_Y_AUX1[7:0]							
4C	76	ACCEL_DATA_Z_AUX1_0	ACCEL_DATA_Z_AUX1[15:8]							
4D	77	ACCEL_DATA_Z_AUX1_1	ACCEL_DATA_Z_AUX1[7:0]							
4E	78	GYRO_DATA_X_AUX1_0	GYRO_DATA_X_AUX1[15:8]							
4F	79	GYRO_DATA_X_AUX1_1	GYRO_DATA_X_AUX1[7:0]							
50	80	GYRO_DATA_Y_AUX1_0	GYRO_DATA_Y_AUX1[15:8]							
51	81	GYRO_DATA_Y_AUX1_1	GYRO_DATA_Y_AUX1[7:0]							
52	82	GYRO_DATA_Z_AUX1_0	GYRO_DATA_Z_AUX1[15:8]							
53	83	GYRO_DATA_Z_AUX1_1	GYRO_DATA_Z_AUX1[7:0]							
54	84	TEMP_DATA_AUX1_0	TEMP_DATA_AUX1[15:8]							
55	85	TEMP_DATA_AUX1_1	TEMP_DATA_AUX1[7:0]							
56	86	TMST_FSYNC_DATA_AUX1_0	TMST_FSYNC_DATA_AUX1[15:8]							
57	87	TMST_FSYNC_DATA_AUX1_1	TMST_FSYNC_DATA_AUX1[7:0]							
58	88	PWR_MGMT_AUX1	-						GYRO_AUX1_EN[0]	ACCEL_AUX1_EN[0]
59	89	FS_SEL_AUX1	-	AUX1_GYRO_FS_SEL[3:0]				AUX1_ACCEL_FS_SEL[2:0]		
5A	90	INT2_CONFIG0	INT2_STATUS_EN_RESET_DONE[0]	INT2_STATUS_EN_AUX1_AGC_RDY[0]	INT2_STATUS_EN_AP_AGC_RDY[0]	INT2_STATUS_EN_AP_FSYNC[0]	INT2_STATUS_EN_AUX1_DRDY[0]	INT2_STATUS_EN_DRDY[0]	INT2_STATUS_EN_FIFO_THS[0]	INT2_STATUS_EN_FIFO_FULL[0]

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Addr (Hex)	Addr (Dec.)	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5B	91	INT2_CONFIG1	-	INT2_STATUS_EN_APEX_EVENT[0]	-	INT2_STATUS_EN_I3C_PROTOCOL_ERR[0]	INT2_STATUS_EN_WOM_Z[0]	INT2_STATUS_EN_WOM_Y[0]	INT2_STATUS_EN_WOM_X[0]	INT2_STATUS_EN_PLL_RDY[0]
5C	92	INT2_CONFIG2	-					INT2_DRIVE[0]	INT2_MODE[0]	INT2_POLARITY[0]
5D	93	INT2_STATUS0	INT2_STATUS_RESET_DONE[0]	INT2_STATUS_AUX1_AGC_RDY[0]	INT2_STATUS_AP_AGC_RDY[0]	INT2_STATUS_AP_FSYNC[0]	INT2_STATUS_AUX1_DRDY[0]	INT2_STATUS_DRDY[0]	INT2_STATUS_FIFO_THS[0]	INT2_STATUS_FIFO_FULL[0]
5E	94	INT2_STATUS1	-	INT2_STATUS_APEX_EVENT[0]	-	INT2_STATUS_I3C_PROTOCOL_ERR[0]	INT2_STATUS_WOM_Z[0]	INT2_STATUS_WOM_Y[0]	INT2_STATUS_WOM_X[0]	INT2_STATUS_PLL_RDY[0]
72	114	WHO_AM_I	WHO_AM_I[7:0]							
73	115	REG_HOST_MSG	-		EDMP_ON_DEMAND_EN[0]	-				TESTOPENABLE[0]
7C	124	IREG_ADDR_15_8	IREG_ADDR_15_8[7:0]							
7D	125	IREG_ADDR_7_0	IREG_ADDR_7_0[7:0]							
7E	126	IREG_DATA	IREG_DATA[7:0]							
7F	127	REG_MISC2	-						SOFT_RST[0]	IREG_DONE[0]

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as “can be changed on-the-fly.” These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

15 USER BANK IPREG_BAR REGISTER MAP – DESCRIPTIONS

15.1 IPREG_BAR_REG_56

Name: IPREG_BAR_REG_56
Address: 56 (38h)
Reset value: 0xDB
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	PADS_AP_SCLK_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up(1) or down(0)
[6]	R/W	PADS_AP_SCLK_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal pull resistor to pull pad up or down depending on direction.
[5]	-	-	Reserved
[4]	R/W	PADS_AP_CS_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up(1) or down(0)
[3]	R/W	PADS_AP_CS_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal pull resistor to pull pad up or down depending on direction.
[2:0]	-	-	Reserved

15.2 IPREG_BAR_REG_57

Name: IPREG_BAR_REG_57
Address: 57 (39h)
Reset value: 0xB6
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	PADS_AUX_CS_TP3_TP_PE_TRIM_D2A[0]	[Supports Dynamic Change] Selects pull direction of the pad using the internal resistor either up (1) or down (0)
[6]	-	-	Reserved
[5]	R/W	PADS_AP_SDO_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up (1) or down (0)
[4]	R/W	PADS_AP_SDO_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal resistor to pull pad up or down depending on direction choice.
[3]	-	-	Reserved
[2]	R/W	PADS_AP_SDI_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up (1) or down (0)
[1]	R/W	PADS_AP_SDI_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal resistor to pull pad up or down depending on direction choice.
[0]	-	-	Reserved

15.3 IPREG_BAR_REG_58

Name: IPREG_BAR_REG_58
Address: 58 (3Ah)
Reset value: 0x6D
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	PADS_AUX_SDI_TP1_TP_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Enables pull of the pad using the internal resistor depending on the direction
[5]	R/W	PADS_AUX_SDI_TP1_TP_PE_TRIM_D2A[0]	[Supports Dynamic Change] Selects pull direction of the pad using the internal resistor either up (1) or down (0)
[4]	-	-	Reserved
[3]	R/W	PADS_AUX_SCLK_TP2_TP_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Enables pull of the pad using the internal resistor depending on the direction
[2]	R/W	PADS_AUX_SCLK_TP2_TP_PE_TRIM_D2A[0]	[Supports Dynamic Change] Selects pull direction of the pad using the internal resistor either up (1) or down (0)
[1]	-	-	-
[0]	R/W	PADS_AUX_CS_TP3_TP_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Enables pull of the pad using the internal resistor depending on the direction

15.4 IPREG_BAR_REG_59

Name: IPREG_BAR_REG_59
Address: 59 (3Bh)
Reset value: 0xD7
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	PADS_INT2_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up (1) or down (0)
[6]	R/W	PADS_INT2_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal resistor to pull pad up or down depending on direction choice.
[5]	-	-	Reserved
[4]	R/W	PADS_INT1_TP0_TP_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Enables pull of the pad using the internal resistor depending on the direction
[3]	R/W	PADS_INT1_TP0_TP_PE_TRIM_D2A[0]	[Supports Dynamic Change] Selects pull direction of the pad using the internal resistor either up (1) or down (0)
[2]	-	-	Reserved
[1]	R/W	PADS_AUX_SDO_PUD_TRIM_D2A[0]	[Supports Dynamic Change] Selects internal resistor pull direction up (1) or down (0)
[0]	R/W	PADS_AUX_SDO_PE_TRIM_D2A[0]	[Supports Dynamic Change] Enables internal resistor to pull pad up or down depending on direction choice.

15.5 IPREG_BAR_REG_69

Name: IPREG_BAR_REG_69
Address: 69 (45h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1:0]	R/W	PADS_OD_PUD_STRENGTH_TRIM_D2A[1:0]	[Supports Dynamic Change] Configures drive strength for all output pins in OD mode, which in turn controls VOL level. 0 highest pull down strength, 3 weakest pull down strength.

16 USER BANK IPREG_ANA REGISTER MAP – DESCRIPTIONS

16.1 IPREG_ANA_REG_8

Name: IPREG_ANA_REG_8
Address: 08 (08h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R/W	PD_ACCEL_ST_B_D2A[0]	[Supports Dynamic Change] Override to power-down Self-Test Regulator
[0]	R/W	PD_ACCEL_CP45_ST_B_D2A[0]	[Supports Dynamic Change] Override to power-down 4.5V CP

17 USER BANK IMEM_SRAM REGISTER MAP – DESCRIPTIONS

17.1 IMEM_SRAM_REG_0

Name: IMEM_SRAM_REG_0
Address: 00 (00h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_X_STR_FT[7:0]	Gyro X axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.2 IMEM_SRAM_REG_1

Name: IMEM_SRAM_REG_1
Address: 01 (01h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_X_STR_FT[15:8]	Gyro X axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.3 IMEM_SRAM_REG_2

Name: IMEM_SRAM_REG_2
Address: 02 (02h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Y_STR_FT[7:0]	Gyro Y axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.4 IMEM_SRAM_REG_3

Name: IMEM_SRAM_REG_3
Address: 03 (03h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Y_STR_FT[15:8]	Gyro Y axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.5 IMEM_SRAM_REG_4

Name: IMEM_SRAM_REG_4
Address: 04 (04h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Z_STR_FT[7:0]	Gyro Z axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.6 IMEM_SRAM_REG_5

Name: IMEM_SRAM_REG_5
Address: 05 (05h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Z_STR_FT[15:8]	Gyro Z axis. Self-Test response factory measurement [kdps] Range: ±0.5 kdps Resolution: 2^-15 kdps = ~30.5 mdps

17.7 IMEM_SRAM_REG_6

Name: IMEM_SRAM_REG_6
Address: 06 (06h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_X_CMOS_GAIN_FT[7:0]	Gyro X axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.8 IMEM_SRAM_REG_7

Name: IMEM_SRAM_REG_7
Address: 07 (07h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_X_CMOS_GAIN_FT[11:8]	Gyro X axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.9 IMEM_SRAM_REG_8

Name: IMEM_SRAM_REG_8
Address: 08 (08h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Y_CMOS_GAIN_FT[7:0]	Gyro Y axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.10 IMEM_SRAM_REG_9

Name: IMEM_SRAM_REG_9
Address: 09 (09h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_Y_CMOS_GAIN_FT[11:8]	Gyro Y axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.11 IMEM_SRAM_REG_10

Name: IMEM_SRAM_REG_10
Address: 10 (0Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Z_CMOS_GAIN_FT[7:0]	Gyro Z axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.12 IMEM_SRAM_REG_11

Name: IMEM_SRAM_REG_11
Address: 11 (0Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_Z_CMOS_GAIN_FT[11:8]	Gyro Z axis. SC2V+ADC gain factory measurement [kdps]. Range: 0 to 0.5 kdps Resolution: 2^-13 kdps = ~122 mdps

17.13 IMEM_SRAM_REG_12

Name: IMEM_SRAM_REG_12
Address: 12 (0Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_X_STR_FT[7:0]	Accel X axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

17.14 IMEM_SRAM_REG_13

Name: IMEM_SRAM_REG_13
Address: 13 (0Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_X_STR_FT[15:8]	Accel X axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

17.15 IMEM_SRAM_REG_14

Name: IMEM_SRAM_REG_14
Address: 14 (0Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Y_STR_FT[7:0]	Accel Y axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

17.16 IMEM_SRAM_REG_15

Name: IMEM_SRAM_REG_15
Address: 15 (0Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Y_STR_FT[15:8]	Accel Y axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

17.17 IMEM_SRAM_REG_16

Name: IMEM_SRAM_REG_16
Address: 16 (10h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Z_STR_FT[7:0]	Accel Z axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

17.18 IMEM_SRAM_REG_17

Name: IMEM_SRAM_REG_17
Address: 17 (11h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Z_STR_FT[15:8]	Accel Z axis. Self-test response factory measurement [gee]. Range: ±1 gee Resolution: 2^-13 gee = ~0.122 mgee

18 USER BANK IMEM_SRAM_APEX REGISTER MAP – DESCRIPTIONS

18.1 IMEM_SRAM_APEX_REG_42

Name: IMEM_SRAM_APEX_REG_42
Address: 42 (2Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_FF[7:0]	Specify ODR of feature Free-Fall Unit: Hertz Default value: 400 Format: int16_t

18.2 IMEM_SRAM_APEX_REG_43

Name: IMEM_SRAM_APEX_REG_43
Address: 43 (2Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_FF[15:8]	Specify ODR of feature Free-Fall Unit: Hertz Default value: 400 Format: int16_t

18.3 IMEM_SRAM_APEX_REG_44

Name: IMEM_SRAM_APEX_REG_44
Address: 44 (2Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_TAP[7:0]	Specify ODR of feature Tap Unit: Hertz Default value: 400 Format: int16_t

18.4 IMEM_SRAM_APEX_REG_45

Name: IMEM_SRAM_APEX_REG_45
Address: 45 (2Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_TAP[15:8]	Specify ODR of feature Tap Unit: Hertz Default value: 400 Format: int16_t

18.5 IMEM_SRAM_APEX_REG_46

Name: IMEM_SRAM_APEX_REG_46
Address: 46 (2Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_R2W[7:0]	Specify ODR of feature Raise-to-Wake Unit: Hertz Default value: 25 Format: int16_t

18.6 IMEM_SRAM_APEX_REG_47

Name: IMEM_SRAM_APEX_REG_47
Address: 47 (2Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_R2W[15:8]	Specify ODR of feature Raise-to-Wake Unit: Hertz Default value: 25 Format: int16_t

18.7 IMEM_SRAM_APEX_REG_48

Name: IMEM_SRAM_APEX_REG_48
Address: 48 (30h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_3AXIS[7:0]	Specify ODR of Three-Axis Unit: Hertz Default value: 50 Format: int16_t

18.8 IMEM_SRAM_APEX_REG_49

Name: IMEM_SRAM_APEX_REG_49
Address: 49 (31h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_3AXIS[15:8]	Specify ODR of Three-Axis Unit: Hertz Default value: 50 Format: int16_t

18.9 IMEM_SRAM_APEX_REG_50

Name: IMEM_SRAM_APEX_REG_50
Address: 50 (32h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_TILT[7:0]	Specify ODR of feature Tilt Unit: Hertz Default value: 50 Format: int16_t

18.10 IMEM_SRAM_APEX_REG_51

Name: IMEM_SRAM_APEX_REG_51
Address: 51 (33h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_TILT[15:8]	Specify ODR of feature Tilt Unit: Hertz Default value: 50 Format: int16_t

18.11 IMEM_SRAM_APEX_REG_52

Name: IMEM_SRAM_APEX_REG_52
Address: 52 (34h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_PED[7:0]	Specify ODR of feature Pedometer Unit: Hertz Default value: 50 Format: int16_t

18.12 IMEM_SRAM_APEX_REG_53

Name: IMEM_SRAM_APEX_REG_53
Address: 53 (35h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_PED[15:8]	Specify ODR of feature Pedometer Unit: Hertz Default value: 50 Format: int16_t

18.13 IMEM_SRAM_APEX_REG_54

Name: IMEM_SRAM_APEX_REG_54
Address: 54 (36h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_SMD[7:0]	Specify ODR of feature Significant-Motion-Detection Unit: Hertz Default value: 50 Format: int16_t

18.14 IMEM_SRAM_APEX_REG_55

Name: IMEM_SRAM_APEX_REG_55
Address: 55 (37h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_SMD[15:8]	Specify ODR of feature Significant-Motion-Detection Unit: Hertz Default value: 50 Format: int16_t

18.15 IMEM_SRAM_APEX_REG_56

Name: IMEM_SRAM_APEX_REG_56
Address: 56 (38h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_B2S[7:0]	Specify ODR of feature Bring-to-See Unit: Hertz Default value: 50 Format: int16_t

18.16 IMEM_SRAM_APEX_REG_57

Name: IMEM_SRAM_APEX_REG_57
Address: 57 (39h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_B2S[15:8]	Specify ODR of feature Bring-to-See Unit: Hertz Default value: 50 Format: int16_t

18.17 IMEM_SRAM_APEX_REG_58

Name: IMEM_SRAM_APEX_REG_58
Address: 58 (3Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_SHAKE[7:0]	Specify ODR of feature Shake Unit: Hertz Default value: 50 Format: int16_t

18.18 IMEM_SRAM_APEX_REG_59

Name: IMEM_SRAM_APEX_REG_59
Address: 59 (3Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_SHAKE[15:8]	Specify ODR of feature Shake Unit: Hertz Default value: 50 Format: int16_t

18.19 IMEM_SRAM_APEX_REG_60

Name: IMEM_SRAM_APEX_REG_60
Address: 60 (3Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_NOMOTION[7:0]	Specify ODR of feature No-Motion Unit: Hertz Default value: 50 Format: int16_t

18.20 IMEM_SRAM_APEX_REG_61

Name: IMEM_SRAM_APEX_REG_61
Address: 61 (3Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_NOMOTION[15:8]	Specify ODR of feature No-Motion Unit: Hertz Default value: 50 Format: int16_t

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18.21 IMEM_SRAM_APEX_REG_62

Name: IMEM_SRAM_APEX_REG_62
Address: 62 (3Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_FLAT[7:0]	Specify ODR of feature Flat Unit: Hertz Default value: 50 Format: int16_t

18.22 IMEM_SRAM_APEX_REG_63

Name: IMEM_SRAM_APEX_REG_63
Address: 63 (3Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ODR_FLAT[15:8]	Specify ODR of feature Flat Unit: Hertz Default value: 50 Format: int16_t

18.23 IMEM_SRAM_APEX_REG_98

Name: IMEM_SRAM_APEX_REG_98
Address: 98 (62h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	QUAT_RESET_EN[7:0]	Set 1 to force reset 3-axis quaternion when next tilt reset is done This is applicable only if tilt_reset_en is also set to 1 Format: uint8_t

18.24 IMEM_SRAM_APEX_REG_99

Name: IMEM_SRAM_APEX_REG_99
Address: 99 (63h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_RESET_EN[7:0]	Set 1 to reset tilt prior to any further tilt processing on next sensor data Format: uint8_t

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18.25 IMEM_SRAM_APEX_REG_121

Name: IMEM_SRAM_APEX_REG_121
Address: 121 (79h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CADENCE[7:0]	Instant step cadence measured by the algorithm Unit: 4*number of samples between two consecutive steps. Cadency (step/s) = (ped_step_cadence / 4) / (pedometer_ ODR). Format: uint8_t

18.26 IMEM_SRAM_APEX_REG_122

Name: IMEM_SRAM_APEX_REG_122
Address: 122 (7Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_ACTIVITY_CLASS[7:0]	Activity classification of step detected Unit: Enum: unknown (0), walk(1), run(2) Format: uint8_t

18.27 IMEM_SRAM_APEX_REG_124

Name: IMEM_SRAM_APEX_REG_124
Address: 124 (7Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_BUF1[7:0]	Number of steps done since the last init of the pedometer feature. Filled in alternatively with ped_step_cnt_buf2. Format: uint16_t

18.28 IMEM_SRAM_APEX_REG_125

Name: IMEM_SRAM_APEX_REG_125
Address: 125 (7Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_BUF1[15:8]	Number of steps done since the last init of the pedometer feature. Filled in alternatively with ped_step_cnt_buf2. Format: uint16_t

18.29 IMEM_SRAM_APEX_REG_126

Name: IMEM_SRAM_APEX_REG_126
Address: 126 (7Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_BUF2[7:0]	Number of steps done since the last init of the pedometer feature. Filled in alternatively with ped_step_cnt_buf1. Unit: number of steps Format: uint16_t

18.30 IMEM_SRAM_APEX_REG_127

Name: IMEM_SRAM_APEX_REG_127
Address: 127 (7Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_BUF2[15:8]	Number of steps done since the last init of the pedometer feature. Filled in alternatively with ped_step_cnt_buf1. Unit: number of steps Format: uint16_t

18.31 IMEM_SRAM_APEX_REG_136

Name: IMEM_SRAM_APEX_REG_136
Address: 136 (88h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DURATION_BUF1[7:0]	Duration of the freefall. Filled in alternatively with ff_duration_buf2. Unit: time in sample number Format: int16_t

18.32 IMEM_SRAM_APEX_REG_137

Name: IMEM_SRAM_APEX_REG_137
Address: 137 (89h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DURATION_BUF1[15:8]	Duration of the freefall. Filled in alternatively with ff_duration_buf2. Unit: time in sample number Format: int16_t

18.33 IMEM_SRAM_APEX_REG_138

Name: IMEM_SRAM_APEX_REG_138
Address: 138 (8Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DURATION_BUF2[7:0]	Duration of the freefall Filled in alternatively with ff_duration_buf1 Unit: time in sample number Format: int16_t

18.34 IMEM_SRAM_APEX_REG_139

Name: IMEM_SRAM_APEX_REG_139
Address: 139 (8Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DURATION_BUF2[15:8]	Duration of the freefall Filled in alternatively with ff_duration_buf1 Unit: time in sample number Format: int16_t

18.35 IMEM_SRAM_APEX_REG_142

Name: IMEM_SRAM_APEX_REG_142
Address: 142 (8Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_NUM[7:0]	Enum of the tap type. Unit: enum, 0: no tap 1: single tap 2: double tap 3: triple tap Format: uint8_t

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18.36 IMEM_SRAM_APEX_REG_143

Name: IMEM_SRAM_APEX_REG_143
Address: 143 (8Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_AXIS[7:0]	Indicate the axis of the tap in the device frame Unit: enum, 0: ax, 1: ay, 2: az. Format: uint8_t

18.37 IMEM_SRAM_APEX_REG_144

Name: IMEM_SRAM_APEX_REG_144
Address: 144 (90h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_DIR[7:0]	Indicate the direction of the tap in the device frame Unit: enum, 0: positive, 1: negative Format: uint8_t

18.38 IMEM_SRAM_APEX_REG_145

Name: IMEM_SRAM_APEX_REG_145
Address: 145 (91h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	DOUBLE_TAP_TIMING[7:0]	Indicate in case of double tap, the sample count of the second pulse detected in the detection window Unit: time in sample number Format: uint8_t

18.39 IMEM_SRAM_APEX_REG_146

Name: IMEM_SRAM_APEX_REG_146
Address: 146 (92h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TRIPLE_TAP_TIMING[7:0]	Indicate in case of triple tap, the sample count of the triple pulse detected in the detection window Unit: time in sample number Format: uint8_t

18.40 IMEM_SRAM_APEX_REG_147

Name: IMEM_SRAM_APEX_REG_147
Address: 147 (93h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_OUTAXIS[7:0]	0: undefined axis 1: X axis shake 2: Y axis shake 3: Z axis shake Format: uint8_t

18.41 IMEM_SRAM_APEX_REG_148

Name: IMEM_SRAM_APEX_REG_148
Address: 148 (94h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_OUTLOCK[7:0]	noMotion output lock Format: uint8_t

18.42 IMEM_SRAM_APEX_REG_149

Name: IMEM_SRAM_APEX_REG_149
Address: 149 (95h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_MAJORITY_AXIS[7:0]	Bit mapping 0 => minus X axis, 4 + X axis, 1 => minus y axis, 5 + Y axis, 2 => minus Z axis, 6 + Z axis Format: uint8_t

18.43 IMEM_SRAM_APEX_REG_150

Name: IMEM_SRAM_APEX_REG_150
Address: 150 (96h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_SIGN_ANGLE[7:0]	Sign to be applied to tilt angle to determined if the device point up or down Format: int8_t

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18.44 IMEM_SRAM_APEX_REG_152

Name: IMEM_SRAM_APEX_REG_152
Address: 152 (98h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_X_AXIS_REF[7:0]	x axis reference in q12 of the static position Format: int16_t

18.45 IMEM_SRAM_APEX_REG_153

Name: IMEM_SRAM_APEX_REG_153
Address: 153 (99h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_X_AXIS_REF[15:8]	x axis reference in q12 of the static position Format: int16_t

18.46 IMEM_SRAM_APEX_REG_154

Name: IMEM_SRAM_APEX_REG_154
Address: 154 (9Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_Y_AXIS_REF[7:0]	y axis reference in q12 of the static position Format: int16_t

18.47 IMEM_SRAM_APEX_REG_155

Name: IMEM_SRAM_APEX_REG_155
Address: 155 (9Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_Y_AXIS_REF[15:8]	y axis reference in q12 of the static position Format: int16_t

18.48 IMEM_SRAM_APEX_REG_156

Name: IMEM_SRAM_APEX_REG_156
Address: 156 (9Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_TILT_ANGLE_RAW_FORMAT[7:0]	Tilt angle in raw forma, to be convert in degree by using this formula: sign_angle*57.2958f*acosf(tilt_angle_raw_format/4096.0f) Format: int16_t

18.49 IMEM_SRAM_APEX_REG_157

Name: IMEM_SRAM_APEX_REG_157
Address: 157 (9Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_TILT_ANGLE_RAW_FORMAT[15:8]	Tilt angle in raw forma, to be convert in degree by using this formula: sign_angle*57.2958f*acosf(tilt_angle_raw_format/4096.0f) Format: int16_t

18.50 IMEM_SRAM_APEX_REG_168

Name: IMEM_SRAM_APEX_REG_168
Address: 168 (A8h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	POWER_SAVE_TIME[7:0]	The time (in sample number) after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400 Format: uint32_t

18.51 IMEM_SRAM_APEX_REG_169

Name: IMEM_SRAM_APEX_REG_169
Address: 169 (A9h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	POWER_SAVE_TIME[15:8]	The time (in sample number) after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400 Format: uint32_t

18.52 IMEM_SRAM_APEX_REG_170

Name: IMEM_SRAM_APEX_REG_170
Address: 170 (AAh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	POWER_SAVE_TIME[23:16]	The time (in sample number) after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400 Format: uint32_t

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18.53 IMEM_SRAM_APEX_REG_171

Name: IMEM_SRAM_APEX_REG_171
Address: 171 (ABh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	POWER_SAVE_TIME[31:24]	The time (in sample number) after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400 Format: uint32_t

18.54 IMEM_SRAM_APEX_REG_188

Name: IMEM_SRAM_APEX_REG_188
Address: 188 (BCh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MIN_DURATION[7:0]	Minimum duration between a lowG and HighG event to trigger freefall Unit: in sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] For information, it corresponds to approximately a fall of 10cm Format: uint32_t

18.55 IMEM_SRAM_APEX_REG_189

Name: IMEM_SRAM_APEX_REG_189
Address: 189 (BDh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MIN_DURATION[15:8]	Minimum duration between a lowG and HighG event to trigger freefall Unit: in sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] For information, it corresponds to approximately a fall of 10cm Format: uint32_t

18.56 IMEM_SRAM_APEX_REG_190

Name: IMEM_SRAM_APEX_REG_190
Address: 190 (BEh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MIN_DURATION[23:16]	Minimum duration between a lowG and HighG event to trigger freefall Unit: in sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] For information, it corresponds to approximately a fall of 10cm Format: uint32_t

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18.57 IMEM_SRAM_APEX_REG_191

Name: IMEM_SRAM_APEX_REG_191
Address: 191 (BFh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MIN_DURATION[31:24]	Minimum duration between a lowG and HighG event to trigger freefall Unit: in sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] For information, it corresponds to approximately a fall of 10cm Format: uint32_t

18.58 IMEM_SRAM_APEX_REG_192

Name: IMEM_SRAM_APEX_REG_192
Address: 192 (C0h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MAX_DURATION[7:0]	Maximum duration after a lowG event to wait HighG event before reset freefall algorithm Unit: in sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] For information, it corresponds to approximately a fall of 2.5 meter Format: uint32_t

18.59 IMEM_SRAM_APEX_REG_193

Name: IMEM_SRAM_APEX_REG_193
Address: 193 (C1h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MAX_DURATION[15:8]	Maximum duration after a lowG event to wait HighG event before reset freefall algorithm Unit: in sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] For information, it corresponds to approximately a fall of 2.5 meter Format: uint32_t

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18.60 IMEM_SRAM_APEX_REG_194

Name: IMEM_SRAM_APEX_REG_194
Address: 194 (C2h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MAX_DURATION[23:16]	Maximum duration after a lowG event to wait HighG event before reset freefall algorithm Unit: in sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] For information, it corresponds to approximately a fall of 2.5 meter Format: uint32_t

18.61 IMEM_SRAM_APEX_REG_195

Name: IMEM_SRAM_APEX_REG_195
Address: 195 (C3h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_MAX_DURATION[31:24]	Maximum duration after a lowG event to wait HighG event before reset freefall algorithm Unit: in sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] For information, it corresponds to approximately a fall of 2.5 meter Format: uint32_t

18.62 IMEM_SRAM_APEX_REG_196

Name: IMEM_SRAM_APEX_REG_196
Address: 196 (C4h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DEBOUNCE_DURATION[7:0]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: in sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

18.63 IMEM_SRAM_APEX_REG_197

Name: IMEM_SRAM_APEX_REG_197
Address: 197 (C5h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DEBOUNCE_DURATION[15:8]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: in sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

18.64 IMEM_SRAM_APEX_REG_198

Name: IMEM_SRAM_APEX_REG_198
Address: 198 (C6h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DEBOUNCE_DURATION[23:16]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: in sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

18.65 IMEM_SRAM_APEX_REG_199

Name: IMEM_SRAM_APEX_REG_199
Address: 199 (C7h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FF_DEBOUNCE_DURATION[31:24]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: in sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

18.66 IMEM_SRAM_APEX_REG_206

Name: IMEM_SRAM_APEX_REG_206
Ad dress: 206 (CEh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_PEAK_TH[7:0]	Any of the absolute accelerometer axis surpasses high_peak_thres will potentially trigger the start of HighG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 29696 (corresponding to 7.25g) Recommended range value: [1024-32768]

18.67 IMEM_SRAM_APEX_REG_207

Name: IMEM_SRAM_APEX_REG_207
Address: 207 (CFh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_PEAK_TH[15:8]	Any of the absolute accelerometer axis surpasses high_peak_thres will potentially trigger the start of HighG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 29696 (corresponding to 7.25g) Recommended range value: [1024-32768]

18.68 IMEM_SRAM_APEX_REG_208

Name: IMEM_SRAM_APEX_REG_208
Address: 208 (D0h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_PEAK_TH_HYST[7:0]	A hysteresis high_peak_thres_hyst is substracted from the threshold (high_peak_thres) after the initial threshold is met Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 640 (corresponding to 0.1563g) Recommended range value: [128 - 1024] Format: int16_t

18.69 IMEM_SRAM_APEX_REG_209

Name: IMEM_SRAM_APEX_REG_209
Address: 209 (D1h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_PEAK_TH_HYST[15:8]	A hysteresis high_peak_thres_hyst is substracted from the threshold (high_peak_thres) after the initial threshold is met Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 640 (corresponding to 0.1563g) Recommended range value: [128 - 1024] Format: int16_t

18.70 IMEM_SRAM_APEX_REG_210

Name: IMEM_SRAM_APEX_REG_210
Address: 210 (D2h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_TIME_TH[7:0]	The number of samples the device should stay above (highg_peak_th - highg_peak_th_hyst) before HighG state is triggered Unit: in sample number - ODR dependent Default value: 1 (corresponding to 2.5ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

18.71 IMEM_SRAM_APEX_REG_211

Name: IMEM_SRAM_APEX_REG_211
Address: 211 (D3h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	HIGHG_TIME_TH[15:8]	The number of samples the device should stay above (highg_peak_th - highg_peak_th_hyst) before HighG state is triggered Unit: in sample number - ODR dependent Default value: 1 (corresponding to 2.5ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

18.72 IMEM_SRAM_APEX_REG_218

Name: IMEM_SRAM_APEX_REG_218
Address: 218 (DAh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_PEAK_TH[7:0]	Sum of absolute accelerometer axis falls lowg_peak_th will potentially trigger the start of LowG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 0.5g) Recommended range value: [128 - 4096] Format: int16_t

18.73 IMEM_SRAM_APEX_REG_219

Name: IMEM_SRAM_APEX_REG_219
Address: 219 (DBh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_PEAK_TH[15:8]	Sum of absolute accelerometer axis falls lowg_peak_th will potentially trigger the start of LowG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 0.5g) Recommended range value: [128 - 4096] Format: int16_t

18.74 IMEM_SRAM_APEX_REG_220

Name: IMEM_SRAM_APEX_REG_220
Address: 220 (DCh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_PEAK_TH_HYST[7:0]	Hysteresis added to the threshold to confirm the triggering of the LowG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 128 (corresponding to 31.2mg) Recommended range value: [128 - 1024] Format: int16_t

18.75 IMEM_SRAM_APEX_REG_221

Name: IMEM_SRAM_APEX_REG_221
Address: 221 (DDh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_PEAK_TH_HYST[15:8]	Hysteresis added to the threshold to confirm the triggering of the LowG state Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 128 (corresponding to 31.2mg) Recommended range value: [128 - 1024] Format: int16_t

18.76 IMEM_SRAM_APEX_REG_222

Name: IMEM_SRAM_APEX_REG_222
Address: 222 (DEh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_TIME_TH[7:0]	The number of samples device should stay below (lowg_peak_th + lowg_peak_th_hyst) before LowG state is triggered Unit: in sample number - ODR dependent Default value: 13 (corresponding to 32ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

18.77 IMEM_SRAM_APEX_REG_223

Name: IMEM_SRAM_APEX_REG_223
Address: 223 (DFh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	LOWG_TIME_TH[15:8]	The number of samples device should stay below (lowg_peak_th + lowg_peak_th_hyst) before LowG state is triggered Unit: in sample number - ODR dependent Default value: 13 (corresponding to 32ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

18.78 IMEM_SRAM_APEX_REG_228

Name: IMEM_SRAM_APEX_REG_228
Address: 228 (E4h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_TMAX[7:0]	Time window since the jerk maximum value, used to observe a single-tap, double-tap, triple-tap or rejection of the tap event. Unit: in sample number, ODR dependent Default: 198 at 400Hz, corresponding to 0.495s Format: uint16_t

18.79 IMEM_SRAM_APEX_REG_229

Name: IMEM_SRAM_APEX_REG_229
Address: 229 (E5h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_TMAX[15:8]	Time window since the jerk maximum value, used to observe a single-tap, double-tap, triple-tap or rejection of the tap event. Unit: in sample number, ODR dependent Default: 198 at 400Hz, corresponding to 0.495s Format: uint16_t

18.80 IMEM_SRAM_APEX_REG_230

Name: IMEM_SRAM_APEX_REG_230
Address: 230 (E6h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_TMIN[7:0]	Single tap window, sub-window within the TAP_TMAX to detect tap event Unit: in sample number, ODR dependent Default value: 66 at 400Hz, representing 0.1650s Format: uint8_t

18.81 IMEM_SRAM_APEX_REG_231

Name: IMEM_SRAM_APEX_REG_231
Address: 231 (E7h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MIN_JERK[7:0]	The minimal value of jerk to be considered as a tap candidate Unit: in LSB with 1 LSB = 1g / 2^4 (of the jerk value) Default value: 18 corresponding to 1.125 g Format: uint8_t

18.82 IMEM_SRAM_APEX_REG_232

Name: IMEM_SRAM_APEX_REG_232
Address: 232 (E8h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_SMUDGE_REJECT_THR[7:0]	Corresponding to the maximum time spent over a threshold before rejecting the tap candidate, at the end of tap_tmin window, if internal counter of number of samples over the smudge threshold is below the tap_smudge_reject_th, single-tap is detected. Unit: in sample number, ODR dependent Default value: 34 at 400Hz, representing 0.085 s Format: uint8_t

18.83 IMEM_SRAM_APEX_REG_233

Name: IMEM_SRAM_APEX_REG_233
Address: 233 (E9h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_PEAK_TOL[7:0]	Maximum peak tolerance is the percentage of pulse amplitude to get the smudge threshold of rejection Unit: enum - use range [1 - 4] Default value: 2 (corresponding to 25 %) Format: uint8_t

18.84 IMEM_SRAM_APEX_REG_234

Name: IMEM_SRAM_APEX_REG_234
Address: 234 (EAh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_TAVG[7:0]	Energy measurement window size to determine the tap axis associated with the 1st tap Unit: in sample number, ODR dependent Use value limited to [1, 2, 4, 8] Default value: 8 Format: uint8_t

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18.85 IMEM_SRAM_APEX_REG_236

Name: IMEM_SRAM_APEX_REG_236
Address: 236 (ECh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_TAP[7:0]	Maximal number of tap quantity detected to be valid Unit: in enum Use value limited to [1, 2, 3] corresponding to [single, double, triple] Default value: 2 Format: uint8_t

18.86 IMEM_SRAM_APEX_REG_237

Name: IMEM_SRAM_APEX_REG_237
Address: 237 (EDh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MIN_TAP[7:0]	Minimal number of tap quantity detected to be valid Unit: in enum Use value limited to [1, 2, 3] corresponding to [single, double, triple] Default value: 2 Format: uint8_t

18.87 IMEM_SRAM_APEX_REG_238

Name: IMEM_SRAM_APEX_REG_238
Address: 238 (EEh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_ENERGY_PRIMARY_AXIS[7:0]	Threshold on maximal energy on primary axis to check validity of tap - Note: only for tap directional rejection Unit: No unit Use value in range [1000 - 10000] Default value: 3000, use 0 to disable this checking Format: uint8_t

18.88 IMEM_SRAM_APEX_REG_239

Name: IMEM_SRAM_APEX_REG_239
Address: 239 (EFh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_ENERGY_PRIMARY_AXIS[15:8]	Threshold on maximal energy on primary axis to check validity of tap - Note: only for tap directional rejection Unit: No unit Use value in range [1000 - 10000] Default value: 3000, use 0 to disable this checking Format: uint8_t

18.89 IMEM_SRAM_APEX_REG_240

Name: IMEM_SRAM_APEX_REG_240
Address: 240 (F0h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_ENERGY_SECONDARY_AXIS[7:0]	Threshold on maximal energy on secondary axis to check validity of tap detection - Note: only for tap directional rejection Unit: No unit Use value in range [200 - 1000] Default value: 500, use 0 to disable this checking Format: uint8_t

18.90 IMEM_SRAM_APEX_REG_241

Name: IMEM_SRAM_APEX_REG_241
Address: 241 (F1h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_MAX_ENERGY_SECONDARY_AXIS[15:8]	Threshold on maximal energy on secondary axis to check validity of tap detection - Note: only for tap directional rejection Unit: No unit Use value in range [200 - 1000] Default value: 500, use 0 to disable this checking Format: uint8_t

18.91 IMEM_SRAM_APEX_REG_242

Name: IMEM_SRAM_APEX_REG_242
Address: 242 (F2h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TAP_AXIS_SELECT_MASK[7:0]	Mask used to select the reported axis and direction of the tap feature Unit: bit mask: 1 for +X, 2 for -X, 4 for +Y, 8 for -Y, 16 for +Z and 32 for -Z Use value in range [1 - 63] Default value: 32, algorithm will detect only -Z tap (also called backtap) - Note use value 63 to detect tap in all axis directions Format: uint8_t

18.92 IMEM_SRAM_APEX_REG_364

Name: IMEM_SRAM_APEX_REG_364
Address: 364 (16Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_TIME_OUT[7:0]	Defines the duration after wake event to report sleep event no matter if position change or not Unit: Time in ms, not ODR dependent Default value: 640, corresponding to 0.64s Recommendation: use range value between [100 - 10000] Format: int32_t

18.93 IMEM_SRAM_APEX_REG_365

Name: IMEM_SRAM_APEX_REG_365
Address: 365 (16Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_TIME_OUT[15:8]	Defines the duration after wake event to report sleep event no matter if position change or not Unit: Time in ms, not ODR dependent Default value: 640, corresponding to 0.64s Recommendation: use range value between [100 - 10000] Format: int32_t

18.94 IMEM_SRAM_APEX_REG_366

Name: IMEM_SRAM_APEX_REG_366
Address: 366 (16Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_TIME_OUT[23:16]	Defines the duration after wake event to report sleep event no matter if position change or not Unit: Time in ms, not ODR dependent Default value: 640, corresponding to 0.64s Recommendation: use range value between [100 - 10000] Format: int32_t

18.95 IMEM_SRAM_APEX_REG_367

Name: IMEM_SRAM_APEX_REG_367
Address: 367 (16Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_TIME_OUT[31:24]	Defines the duration after wake event to report sleep event no matter if position change or not Unit: Time in ms, not ODR dependent Default value: 640, corresponding to 0.64s Recommendation: use range value between [100 - 10000] Format: int32_t

18.96 IMEM_SRAM_APEX_REG_368

Name: IMEM_SRAM_APEX_REG_368
Address: 368 (170h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_GESTURE_DELAY[7:0]	Defines the minimal duration of sleep position before trigger the sleep event Unit: Time in ms, not ODR dependent Default value: 96, corresponding to 0.096s Recommendation: use range value between [0 - 256] Format: int32_t

18.97 IMEM_SRAM_APEX_REG_369

Name: IMEM_SRAM_APEX_REG_369
Address: 369 (171h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_GESTURE_DELAY[15:8]	Defines the minimal duration of sleep position before trigger the sleep event Unit: Time in ms, not ODR dependent Default value: 96, corresponding to 0.096s Recommendation: use range value between [0 - 256] Format: int32_t

18.98 IMEM_SRAM_APEX_REG_370

Name: IMEM_SRAM_APEX_REG_370
Address: 370 (172h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_GESTURE_DELAY[23:16]	Defines the minimal duration of sleep position before trigger the sleep event Unit: Time in ms, not ODR dependent Default value: 96, corresponding to 0.096s Recommendation: use range value between [0 - 256] Format: int32_t

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18.99 IMEM_SRAM_APEX_REG_371

Name: IMEM_SRAM_APEX_REG_371
Address: 371 (173h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SLEEP_GESTURE_DELAY[31:24]	Defines the minimal duration of sleep position before trigger the sleep event Unit: Time in ms, not ODR dependent Default value: 96, corresponding to 0.096s Recommendation: use range value between [0 - 256] Format: int32_t

18.100 IMEM_SRAM_APEX_REG_372

Name: IMEM_SRAM_APEX_REG_372
Address: 372 (174h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOUNTING_MATRIX[7:0]	Mounting matrix to rotate data from chip frame to device frame 3 bits are used [b2 b1 b0]: when b2 = 1 swap X and Y; when b1 = 1 flip X sign; when b0 = 1 flip Y sign Default value: 0 Format: int32_t

18.101 IMEM_SRAM_APEX_REG_373

Name: IMEM_SRAM_APEX_REG_373
Address: 373 (175h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOUNTING_MATRIX[15:8]	Mounting matrix to rotate data from chip frame to device frame 3 bits are used [b2 b1 b0]: when b2 = 1 swap X and Y; when b1 = 1 flip X sign; when b0 = 1 flip Y sign Default value: 0 Format: int32_t

18.102 IMEM_SRAM_APEX_REG_374

Name: IMEM_SRAM_APEX_REG_374
Address: 374 (176h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOUNTING_MATRIX[23:16]	Mounting matrix to rotate data from chip frame to device frame 3 bits are used [b2 b1 b0]: when b2 = 1 swap X and Y; when b1 = 1 flip X sign; when b0 = 1 flip Y sign Default value: 0 Format: int32_t

18.103 IMEM_SRAM_APEX_REG_375

Name: IMEM_SRAM_APEX_REG_375
Address: 375 (177h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOUNTING_MATRIX[31:24]	Mounting matrix to rotate data from chip frame to device frame 3 bits are used [b2 b1 b0]: when b2 = 1 swap X and Y; when b1 = 1 flip X sign; when b0 = 1 flip Y sign Default value: 0 Format: int32_t

18.104 IMEM_SRAM_APEX_REG_376

Name: IMEM_SRAM_APEX_REG_376
Address: 376 (178h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SAMPLING_PERIOD[7:0]	Sampling period corresponding to sensor ODR Unit: Time in ms Default value is 10, corresponding to 40ms (for 100Hz) Recommendation: use value between [10 - 40] Format: int32_t

18.105 IMEM_SRAM_APEX_REG_377

Name: IMEM_SRAM_APEX_REG_377
Address: 377 (179h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SAMPLING_PERIOD[15:8]	Sampling period corresponding to sensor ODR Unit: Time in ms Default value is 10, corresponding to 40ms (for 100Hz) Recommendation: use value between [10 - 40] Format: int32_t

18.106 IMEM_SRAM_APEX_REG_378

Name: IMEM_SRAM_APEX_REG_378
Address: 378 (17Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SAMPLING_PERIOD[23:16]	Sampling period corresponding to sensor ODR Unit: Time in ms Default value is 10, corresponding to 40ms (for 100Hz) Recommendation: use value between [10 - 40] Format: int32_t

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18.107 IMEM_SRAM_APEX_REG_379

Name: IMEM_SRAM_APEX_REG_379
Address: 379 (17Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_SAMPLING_PERIOD[31:24]	Sampling period corresponding to sensor ODR Unit: Time in ms Default value is 10, corresponding to 40ms (for 100Hz) Recommendation: use value between [10 - 40] Format: int32_t

18.108 IMEM_SRAM_APEX_REG_380

Name: IMEM_SRAM_APEX_REG_380
Address: 380 (17Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GRAVITY_FILTER_GAIN[7:0]	Gain used to filter the accelerometer data to obtain an estimation of the gravity (low-pass filter) Defined: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32) Unit: N/A Default value: is 8 at 25Hz and 6 for 50 and 100Hz Format: int32_t

18.109 IMEM_SRAM_APEX_REG_381

Name: IMEM_SRAM_APEX_REG_381
Address: 381 (17Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GRAVITY_FILTER_GAIN[15:8]	Gain used to filter the accelerometer data to obtain an estimation of the gravity (low-pass filter) Defined: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32) Unit: N/A Default value: is 8 at 25Hz and 6 for 50 and 100Hz Format: int32_t

18.110 IMEM_SRAM_APEX_REG_382

Name: IMEM_SRAM_APEX_REG_382
Address: 382 (17Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GRAVITY_FILTER_GAIN[23:16]	Gain used to filter the accelerometer data to obtain an estimation of the gravity (low-pass filter) Defined: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32) Unit: N/A Default value: is 8 at 25Hz and 6 for 50 and 100Hz Format: int32_t

18.111 IMEM_SRAM_APEX_REG_383

Name: IMEM_SRAM_APEX_REG_383
Address: 383 (17Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GRAVITY_FILTER_GAIN[31:24]	Gain used to filter the accelerometer data to obtain an estimation of the gravity (low-pass filter) Defined: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32) Unit: N/A Default value: is 8 at 25Hz and 6 for 50 and 100Hz Format: int32_t

18.112 IMEM_SRAM_APEX_REG_384

Name: IMEM_SRAM_APEX_REG_384
Address: 384 (180h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_ANGLE_COSINE[7:0]	Set the motion detection resolution, the bigger angle (smaller value of cosine) needs bigger amplitude motion to trigger a R2W, Unit: cosine value of angle in q30 Default: 1046221864 corresponding to 13 degrees Recommended range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Format: int32_t

18.113 IMEM_SRAM_APEX_REG_385

Name: IMEM_SRAM_APEX_REG_385
Address: 385 (181h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_ANGLE_COSINE[15:8]	Set the motion detection resolution, the bigger angle (smaller value of cosine) needs bigger amplitude motion to trigger a R2W, Unit: cosine value of angle in q30 Default: 1046221864 corresponding to 13 degrees Recommended range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Format: int32_t

18.114 IMEM_SRAM_APEX_REG_386

Name: IMEM_SRAM_APEX_REG_386
Address: 386 (182h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_ANGLE_COSINE[23:16]	Set the motion detection resolution, the bigger angle (smaller value of cosine) needs bigger amplitude motion to trigger a R2W, Unit: cosine value of angle in q30 Default: 1046221864 corresponding to 13 degrees Recommended range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Format: int32_t

18.115 IMEM_SRAM_APEX_REG_387

Name: IMEM_SRAM_APEX_REG_387
Address: 387 (183h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_ANGLE_COSINE[31:24]	Set the motion detection resolution, the bigger angle (smaller value of cosine) needs bigger amplitude motion to trigger a R2W, Unit: cosine value of angle in q30 Default: 1046221864 corresponding to 13 degrees Recommended range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Format: int32_t

18.116 IMEM_SRAM_APEX_REG_388

Name: IMEM_SRAM_APEX_REG_388
Address: 388 (184h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_FAST[7:0]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30° of inclination) Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 500] Format: int32_t

18.117 IMEM_SRAM_APEX_REG_389

Name: IMEM_SRAM_APEX_REG_389
Address: 389 (185h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_FAST[15:8]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30° of inclination) Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 500] Format: int32_t

18.118 IMEM_SRAM_APEX_REG_390

Name: IMEM_SRAM_APEX_REG_390
Address: 390 (186h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_FAST[23:16]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30° of inclination) Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 500] Format: int32_t

18.119 IMEM_SRAM_APEX_REG_391

Name: IMEM_SRAM_APEX_REG_391
Address: 391 (187h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_FAST[31:24]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30° of inclination) Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 500] Format: int32_t

18.120 IMEM_SRAM_APEX_REG_392

Name: IMEM_SRAM_APEX_REG_392
Address: 392 (188h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_SLOW[7:0]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is over 30° on the Y axis Unit: Time in ms (not ODR dependent) Default value: 500 Recommended range: [240- 1000] Format: int32_t

18.121 IMEM_SRAM_APEX_REG_393

Name: IMEM_SRAM_APEX_REG_393
Address: 393 (189h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_SLOW[15:8]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is over 30° on the Y axis Unit: Time in ms (not ODR dependent) Default value: 500 Recommended range: [240- 1000] Format: int32_t

18.122 IMEM_SRAM_APEX_REG_394

Name: IMEM_SRAM_APEX_REG_394
Address: 394 (18Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_SLOW[23:16]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is over 30° on the Y axis Unit: Time in ms (not ODR dependent) Default value: 500 Recommended range: [240- 1000] Format: int32_t

18.123 IMEM_SRAM_APEX_REG_395

Name: IMEM_SRAM_APEX_REG_395
Address: 395 (18Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_THR_TIMER_SLOW[31:24]	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is over 30° on the Y axis Unit: Time in ms (not ODR dependent) Default value: 500 Recommended range value: [240- 1000] Format: int32_t

18.124 IMEM_SRAM_APEX_REG_396

Name: IMEM_SRAM_APEX_REG_396
Address: 396 (18Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_PREV_GRAVITY_TIMEOUT[7:0]	Time delay to update internal value of previous gravity when no motion is detected Longer time enables detection of motion during slower gesture Unit: Time in ms (not ODR dependent) Default value: 300 Recommended range: [100- 1000] Format: int32_t

18.125 IMEM_SRAM_APEX_REG_397

Name: IMEM_SRAM_APEX_REG_397
Address: 397 (18Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_PREV_GRAVITY_TIMEOUT[15:8]	Time delay to update internal value of previous gravity when no motion is detected Longer time enables detection of motion during slower gesture Unit: Time in ms (not ODR dependent) Default value: 300 Recommended range: [100- 1000] Format: int32_t

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18.126 IMEM_SRAM_APEX_REG_398

Name: IMEM_SRAM_APEX_REG_398
Address: 398 (18Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_PREV_GRAVITY_TIMEOUT[23:16]	Time delay to update internal value of previous gravity when no motion is detected Longer time enables detection of motion during slower gesture Unit: Time in ms (not ODR dependent) Default value: 300 Recommended range: [100- 1000] Format: int32_t

18.127 IMEM_SRAM_APEX_REG_399

Name: IMEM_SRAM_APEX_REG_399
Address: 399 (18Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_MOTION_PREV_GRAVITY_TIMEOUT[31:24]	Time delay to update internal value of previous gravity when no motion is detected Longer time enables detection of motion during slower gesture Unit: Time in ms (not ODR dependent) Default value: 300 Recommended range: [100- 1000] Format: int32_t

18.128 IMEM_SRAM_APEX_REG_400

Name: IMEM_SRAM_APEX_REG_400
Address: 400 (190h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_MOTION_TIMER[7:0]	Time delay to update the current gravity estimator when no motion is detected Unit: Time in ms (not ODR dependent) Default value: 480 Recommended range: [100- 1000] Format: int32_t

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18.129 IMEM_SRAM_APEX_REG_401

Name: IMEM_SRAM_APEX_REG_401
Address: 401 (191h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_MOTION_TIMER[15:8]	Time delay to update the current gravity estimator when no motion is detected Unit: Time in ms (not ODR dependent) Default value: 480 Recommended range: [100- 1000] Format: int32_t

18.130 IMEM_SRAM_APEX_REG_402

Name: IMEM_SRAM_APEX_REG_402
Address: 402 (192h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_MOTION_TIMER[23:16]	Time delay to update the current gravity estimator when no motion is detected Unit: Time in ms (not ODR dependent) Default value: 480 Recommended range: [100- 1000] Format: int32_t

18.131 IMEM_SRAM_APEX_REG_403

Name: IMEM_SRAM_APEX_REG_403
Address: 403 (193h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_MOTION_TIMER[31:24]	Time delay to update the current gravity estimator when no motion is detected Unit: Time in ms (not ODR dependent) Default value: 480 Recommended range: [100- 1000] Format: int32_t

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18.132 IMEM_SRAM_APEX_REG_404

Name: IMEM_SRAM_APEX_REG_404
Address: 404 (194h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_TIMEOUT[7:0]	Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable Unit: Time in ms (not ODR dependent) Default value: 2600 Recommended range: [1000- 10000] Format: int32_t

18.133 IMEM_SRAM_APEX_REG_405

Name: IMEM_SRAM_APEX_REG_405
Address: 405 (195h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_TIMEOUT[15:8]	Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable Unit: Time in ms (not ODR dependent) Default value: 2600 Recommended range: [1000- 10000] Format: int32_t

18.134 IMEM_SRAM_APEX_REG_406

Name: IMEM_SRAM_APEX_REG_406
Address: 406 (196h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_TIMEOUT[23:16]	Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable Unit: Time in ms (not ODR dependent) Default value: 2600 Recommended range: [1000- 10000] Format: int32_t

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18.135 IMEM_SRAM_APEX_REG_407

Name: IMEM_SRAM_APEX_REG_407
Address: 407 (197h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_LAST_GRAVITY_TIMEOUT[31:24]	Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable Unit: Time in ms (not ODR dependent) Default value: 2600 Recommended range: [1000- 10000] Format: int32_t

18.136 IMEM_SRAM_APEX_REG_408

Name: IMEM_SRAM_APEX_REG_408
Address: 408 (198h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GESTURE_VALIDITY_TIMEOUT[7:0]	Gesture validity timeout, if gesture is not completed in this timeout limit, gesture is invalid Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 2000] Format: int32_t

18.137 IMEM_SRAM_APEX_REG_409

Name: IMEM_SRAM_APEX_REG_409
Address: 409 (199h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GESTURE_VALIDITY_TIMEOUT[15:8]	Gesture validity timeout, if gesture is not completed in this timeout limit, gesture is invalid Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 2000] Format: int32_t

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18.138 IMEM_SRAM_APEX_REG_410

Name: IMEM_SRAM_APEX_REG_410
Address: 410 (19Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GESTURE_VALIDITY_TIMEOUT[23:16]	Gesture validity timeout, if gesture is not completed in this timeout limit, gesture is invalid Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 2000] Format: int32_t

18.139 IMEM_SRAM_APEX_REG_411

Name: IMEM_SRAM_APEX_REG_411
Address: 411 (19Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	R2W_GESTURE_VALIDITY_TIMEOUT[31:24]	Gesture validity timeout, if gesture is not completed in this timeout limit, gesture is invalid Unit: Time in ms (not ODR dependent) Default value: 240 Recommended range: [100- 2000] Format: int32_t

18.140 IMEM_SRAM_APEX_REG_492

Name: IMEM_SRAM_APEX_REG_492
Address: 492 (1ECh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	THREEAXIS_ACCEL_ONLY_GAIN[7:0]	Gain value to handle smoothing of 3axis reactivity Unit: N/A Default: 67108864 = q30(0.0625) Format: int32_t

18.141 IMEM_SRAM_APEX_REG_493

Name: IMEM_SRAM_APEX_REG_493
Address: 493 (1EDh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	THREEAXIS_ACCEL_ONLY_GAIN[15:8]	Gain value to handle smoothing of 3axis reactivity Unit: N/A Default: 67108864 = q30(0.0625) Format: int32_t

18.142 IMEM_SRAM_APEX_REG_494

Name: IMEM_SRAM_APEX_REG_494
Address: 494 (1EEh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	THREEAXIS_ACCEL_ONLY_GAIN[23:16]	Gain value to handle smoothing of 3axis reactivity Unit: N/A Default: 67108864 = q30(0.0625) Format: int32_t

18.143 IMEM_SRAM_APEX_REG_495

Name: IMEM_SRAM_APEX_REG_495
Address: 495 (1EFh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	THREEAXIS_ACCEL_ONLY_GAIN[31:24]	Gain value to handle smoothing of 3axis reactivity Unit: N/A Default: 67108864 = q30(0.0625) Format: int32_t

18.144 IMEM_SRAM_APEX_REG_532

Name: IMEM_SRAM_APEX_REG_532
Address: 532 (214h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_WAIT_TIME[7:0]	Wait time in sample number before triggering the tilt event when the tilt threshold is reached or over pass Unit: in sample number - ODR dependent Default value: 200 (corresponding to 4s at 50Hz) Recommended range value: [25 - 1000] Format: int16_t

18.145 IMEM_SRAM_APEX_REG_533

Name: IMEM_SRAM_APEX_REG_533
Address: 533 (215h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_WAIT_TIME[15:8]	Wait time in sample number before triggering the tilt event when the tilt threshold is reached or over pass Unit: in sample number - ODR dependent Default value: 200 (corresponding to 4s at 50Hz) Recommended range value: [25 - 1000] Format: int16_t

18.146 IMEM_SRAM_APEX_REG_536

Name: IMEM_SRAM_APEX_REG_536
Address: 536 (218h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_ANGLE_TH[7:0]	The tilt angle threshold to trigger tilt event Unit: cosine value of angle in q30 Default value: 879557810 corresponding to 35° Format: int32_t

18.147 IMEM_SRAM_APEX_REG_537

Name: IMEM_SRAM_APEX_REG_537
Address: 537 (219h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_ANGLE_TH[15:8]	The tilt angle threshold to trigger tilt event Unit: cosine value of angle in q30 Default value: 879557810 corresponding to 35° Format: int32_t

18.148 IMEM_SRAM_APEX_REG_538

Name: IMEM_SRAM_APEX_REG_538
Address: 538 (21Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_ANGLE_TH[23:16]	The tilt angle threshold to trigger tilt event Unit: cosine value of angle in q30 Default value: 879557810 corresponding to 35° Format: int32_t

18.149 IMEM_SRAM_APEX_REG_539

Name: IMEM_SRAM_APEX_REG_539
Address: 539 (21Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	TILT_ANGLE_TH[31:24]	The tilt angle threshold to trigger tilt event Unit: cosine value of angle in q30 Default value: 879557810 corresponding to 35° Format: int32_t

18.150 IMEM_SRAM_APEX_REG_764

Name: IMEM_SRAM_APEX_REG_764
Address: 764 (2FCh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_PREV_STEP_CNT_TH[7:0]	While Pedometer is running, the number of last steps is incremented in an intermediate buffer. The total step count value is incremented by this intermediate buffer count, only when the number of last steps in the intermediate buffer reaches ped_step_cnt_th. When one would want to change ped_step_cnt_th while the Algo is running, *without algo reinitialization,* and without loss of the step count currently present in the intermediate buffer, one needs to set ped_prev_step_cnt_th to the previous value of ped_step_cnt_th (before the change). Note, at initialization one should set both ped_step_cnt_th and ped_prev_step_cnt_th to the same value. Unit: number of steps Range: [0-15] Default value: 5 Recommendation: set same value as ped_step_cnt_th. Format: int16_t

18.151 IMEM_SRAM_APEX_REG_765

Name: IMEM_SRAM_APEX_REG_765
Address: 765 (2FDh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_PREV_STEP_CNT_TH[15:8]	While Pedometer is running, the number of last steps is incremented in an intermediate buffer. The total step count value is incremented by this intermediate buffer count, only when the number of last steps in the intermediate buffer reaches ped_step_cnt_th. When one would want to change ped_step_cnt_th while the Algo is running, *without algo reinitialization,* and without loss of the step count currently present in the intermediate buffer, one needs to set ped_prev_step_cnt_th to the previous value of ped_step_cnt_th (before the change). Note, at initialization one should set both ped_step_cnt_th and ped_prev_step_cnt_th to the same value. Unit: number of steps Range: [0-15] Default value: 5 Recommendation: set same value as ped_step_cnt_th. Format: int16_t

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18.152 IMEM_SRAM_APEX_REG_894

Name: IMEM_SRAM_APEX_REG_894
Address: 894 (37Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_TH[7:0]	Minimum number of steps needed to be buffered before starting to increment step count in real time. Unit: number of steps Range: [0-15] Default value: 5 Recommendation: For a better rejection rate the value can be increased. If the user does less steps than the value, these steps will not be counted. Format: int16_t

18.153 IMEM_SRAM_APEX_REG_895

Name: IMEM_SRAM_APEX_REG_895
Address: 895 (37Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_CNT_TH[15:8]	Minimum number of steps needed to be buffered before starting to increment step count in real time. Unit: number of steps Range: [0-15] Default value: 5 Recommendation: For a better rejection rate the value can be increased. If the user does less steps than the value, these steps will not be counted. Format: int16_t

18.154 IMEM_SRAM_APEX_REG_896

Name: IMEM_SRAM_APEX_REG_896
Address: 896 (380h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_DET_TH[7:0]	Minimum number of steps needed to be initially detected before starting to report instantaneous step events. Unit: Number of steps Range: [0-7] Default value: 2 Recommendation: For a better rejection rate the value can be increased. Format: int16_t

18.155 IMEM_SRAM_APEX_REG_897

Name: IMEM_SRAM_APEX_REG_897
Address: 897 (381h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_STEP_DET_TH[15:8]	Minimum number of steps needed to be initially detected before starting to report instantaneous step events. Unit: Number of steps Range: [0-7] Default value: 2 Recommendation: For a better rejection rate the value can be increased. Format: int16_t

18.156 IMEM_SRAM_APEX_REG_898

Name: IMEM_SRAM_APEX_REG_898
Address: 898 (382h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_SB_TIMER_TH[7:0]	Maximum permitted time between two consecutive steps. While in the step buffer state, the step buffer count resets to 0 if a new step is not detected for this amount of time (user is considered to have "stopped walking") Unit: time in samples number Range: [0 - 225] Default value: 150 for ODR = 50 Hz Format: int16_t

18.157 IMEM_SRAM_APEX_REG_899

Name: IMEM_SRAM_APEX_REG_899
Address: 899 (383h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_SB_TIMER_TH[15:8]	Maximum permitted time between two consecutive steps. While in the step buffer state, the step buffer count resets to 0 if a new step is not detected for this amount of time (user is considered to have "stopped walking") Unit: time in samples number Range: [0 - 225] Default value: 150 for ODR = 50 Hz Format: int16_t

18.158 IMEM_SRAM_APEX_REG_900

Name: IMEM_SRAM_APEX_REG_900
Address: 900 (384h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_LOW_EN_AMP_TH[7:0]	Threshold on signal amplitude on filtered accelerometer to identify a valid step in slow walk mode. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [1006632 - 3523215] Default value: 2684354 Recommendation: Only used when sensitivity_mode is equal to 1 (slow walk), lower the value to detect smoother steps Format: int32_t

18.159 IMEM_SRAM_APEX_REG_901

Name: IMEM_SRAM_APEX_REG_901
Address: 901 (385h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_LOW_EN_AMP_TH[15:8]	Threshold on signal amplitude on filtered accelerometer to identify a valid step in slow walk mode. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [1006632 - 3523215] Default value: 2684354 Recommendation: Only used when sensitivity_mode is equal to 1 (slow walk), lower the value to detect smoother steps Format: int32_t

18.160 IMEM_SRAM_APEX_REG_902

Name: IMEM_SRAM_APEX_REG_902
Address: 902 (386h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_LOW_EN_AMP_TH[23:16]	Threshold on signal amplitude on filtered accelerometer to identify a valid step in slow walk mode. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [1006632 - 3523215] Default value: 2684354 Recommendation: Only used when sensitivity_mode is equal to 1 (slow walk), lower the value to detect smoother steps Format: int32_t

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18.161 IMEM_SRAM_APEX_REG_903

Name: IMEM_SRAM_APEX_REG_903
Address: 903 (387h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_LOW_EN_AMP_TH[31:24]	Threshold on signal amplitude on filtered accelerometer to identify a valid step in slow walk mode. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [1006632 - 3523215] Default value: 2684354 Recommendation: Only used when sensitivity_mode is equal to 1 (slow walk), lower the value to detect smoother steps Format: int32_t

18.162 IMEM_SRAM_APEX_REG_904

Name: IMEM_SRAM_APEX_REG_904
Address: 904 (388h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_AMP_TH[7:0]	Threshold on the absolute value of the filtered accelerometer data, above which a valid step will be counted. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value. Range: [1006632 - 3019898] Default value: 2080374 Recommendation: At lower value, smoother steps can be detected. Format: int32_t

18.163 IMEM_SRAM_APEX_REG_905

Name: IMEM_SRAM_APEX_REG_905
Address: 905 (389h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_AMP_TH[15:8]	Threshold on the absolute value of the filtered accelerometer data, above which a valid step will be counted. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value. Range: [1006632 - 3019898] Default value: 2080374 Recommendation: At lower value, smoother steps can be detected. Format: int32_t

18.164 IMEM_SRAM_APEX_REG_906

Name: IMEM_SRAM_APEX_REG_906
Address: 906 (38Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_AMP_TH[23:16]	Threshold on the absolute value of the filtered accelerometer data, above which a valid step will be counted. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value. Range: [1006632 - 3019898] Default value: 2080374 Recommendation: At lower value, smoother steps can be detected. Format: int32_t

18.165 IMEM_SRAM_APEX_REG_907

Name: IMEM_SRAM_APEX_REG_907
Address: 907 (38Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_AMP_TH[31:24]	Threshold on the absolute value of the filtered accelerometer data, above which a valid step will be counted. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value. Range: [1006632 - 3019898] Default value: 2080374 Recommendation: At lower value, smoother steps can be detected. Format: int32_t

18.166 IMEM_SRAM_APEX_REG_908

Name: IMEM_SRAM_APEX_REG_908
Address: 908 (38Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_HI_EN_TH[7:0]	Threshold on signal's energy in frequency band corresponding to walking/running. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [2949120 - 5210112] Default value: 3506176 Recommendation: if some walking steps are classified as running, higher the value, if some running steps are classified as walking, lower the value Format: int32_t

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18.167 IMEM_SRAM_APEX_REG_909

Name: IMEM_SRAM_APEX_REG_909
Address: 909 (38Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_HI_EN_TH[15:8]	Threshold on signal's energy in frequency band corresponding to walking/running. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [2949120 - 5210112] Default value: 3506176 Recommendation: if some walking steps are classified as running, higher the value, if some running steps are classified as walking, lower the value Format: int32_t

18.168 IMEM_SRAM_APEX_REG_910

Name: IMEM_SRAM_APEX_REG_910
Address: 910 (38Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_HI_EN_TH[23:16]	Threshold on signal's energy in frequency band corresponding to walking/running. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [2949120 - 5210112] Default value: 3506176 Recommendation: if some walking steps are classified as running, higher the value, if some running steps are classified as walking, lower the value Format: int32_t

18.169 IMEM_SRAM_APEX_REG_911

Name: IMEM_SRAM_APEX_REG_911
Address: 911 (38Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_HI_EN_TH[31:24]	Threshold on signal's energy in frequency band corresponding to walking/running. Unit: LSB with 1 LSB = 1 g/225 from accel filtered value Range: [2949120 - 5210112] Default value: 3506176 Recommendation: if some walking steps are classified as running, higher the value, if some running steps are classified as walking, lower the value Format: int32_t

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18.170 IMEM_SRAM_APEX_REG_912

Name: IMEM_SRAM_APEX_REG_912
Address: 912 (390h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PED_SENSITIVITY_MODE[7:0]	Set the sensitivity to low energy, 0/1 value. 1 is more sensitive to low energy steps Unit: No unit Range: [0 - 1] Default value: 0 Recommendation: To detect very slow walk (with a frequency lower that 1 Hz), value can be set to 1, warning the false detection on no-walking use case may increase. Format: uint8_t

18.171 IMEM_SRAM_APEX_REG_938

Name: IMEM_SRAM_APEX_REG_938
Address: 938 (3AAh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SMD_SENSITIVITY[7:0]	Sensitivity to motion Bit shift of the initial threshold of low value variance, representing the algorithm robustness to rejection use case Acceptable value: 0 to 4 => 0 bike and transport detected some false SMD detection in rejection use case 4=> missing bike and almost no transport detected, minimal SMD detection in rejection use case Unit: integer, from 0 to 4 Default value 0 Format: int8_t

18.172 IMEM_SRAM_APEX_REG_1068

Name: IMEM_SRAM_APEX_REG_1068
Address: 1068 (42Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_MOUNTING_MATRIX[7:0]	Used for b2smounting matrix. 3 bits are used [b2 b1 b0]: When b2 = 1 swap X and Y; When b1 = 1 flip X sign; When b0 = 1 flip Y sign Format: uint8_t

18.173 IMEM_SRAM_APEX_REG_1072

Name: IMEM_SRAM_APEX_REG_1072
Address: 1072 (430h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_DEV_NORM_MAX[7:0]	Hysteresis added or removed to norm estimate and Y axis constraints value for RevB2S Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range: [1 - 2048] Format: int32_t

18.174 IMEM_SRAM_APEX_REG_1073

Name: IMEM_SRAM_APEX_REG_1073
Address: 1073 (431h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_DEV_NORM_MAX[15:8]	Hysteresis added or removed to norm estimate and Y axis constraints value for RevB2S Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range: [1 - 2048] Format: int32_t

18.175 IMEM_SRAM_APEX_REG_1074

Name: IMEM_SRAM_APEX_REG_1074
Address: 1074 (432h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_DEV_NORM_MAX[23:16]	Hysteresis added or removed to norm estimate and Y axis constraints value for RevB2S Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range: [1 - 2048] Format: int32_t

18.176 IMEM_SRAM_APEX_REG_1075

Name: IMEM_SRAM_APEX_REG_1075
Address: 1075 (433h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_DEV_NORM_MAX[31:24]	Hysteresis added or removed to norm estimate and Y axis constraints value for RevB2S Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range: [1 - 2048] Format: int32_t

18.177 IMEM_SRAM_APEX_REG_1076

Name: IMEM_SRAM_APEX_REG_1076
Address: 1076 (434h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_SIN_LIMIT[7:0]	Maximum threshold on absolute value of X axis in b2s position Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range: [300 - 3000] Format: int32_t

18.178 IMEM_SRAM_APEX_REG_1077

Name: IMEM_SRAM_APEX_REG_1077
Address: 1077 (435h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_SIN_LIMIT[15:8]	Maximum threshold on absolute value of X axis in b2s position Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range: [300 - 3000] Format: int32_t

18.179 IMEM_SRAM_APEX_REG_1078

Name: IMEM_SRAM_APEX_REG_1078
Address: 1078 (436h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_SIN_LIMIT[23:16]	Maximum threshold on absolute value of X axis in b2s position Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range: [300 - 3000] Format: int32_t

18.180 IMEM_SRAM_APEX_REG_1079

Name: IMEM_SRAM_APEX_REG_1079
Address: 1079 (437h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_SIN_LIMIT[31:24]	Maximum threshold on absolute value of X axis in b2s position Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range: [300 - 3000] Format: int32_t

18.181 IMEM_SRAM_APEX_REG_1080

Name: IMEM_SRAM_APEX_REG_1080
Address: 1080 (438h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_AGE_LIMIT[7:0]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

18.182 IMEM_SRAM_APEX_REG_1081

Name: IMEM_SRAM_APEX_REG_1081
Address: 1081 (439h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_AGE_LIMIT[15:8]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

18.183 IMEM_SRAM_APEX_REG_1082

Name: IMEM_SRAM_APEX_REG_1082
Address: 1082 (43Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_AGE_LIMIT[23:16]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

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18.184 IMEM_SRAM_APEX_REG_1083

Name: IMEM_SRAM_APEX_REG_1083
Address: 1083 (43Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_AGE_LIMIT[31:24]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

18.185 IMEM_SRAM_APEX_REG_1084

Name: IMEM_SRAM_APEX_REG_1084
Address: 1084 (43Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_LIMIT[7:0]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

18.186 IMEM_SRAM_APEX_REG_1085

Name: IMEM_SRAM_APEX_REG_1085
Address: 1085 (43Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_LIMIT[15:8]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

18.187 IMEM_SRAM_APEX_REG_1086

Name: IMEM_SRAM_APEX_REG_1086
Address: 1086 (43Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_LIMIT[23:16]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

18.188 IMEM_SRAM_APEX_REG_1087

Name: IMEM_SRAM_APEX_REG_1087
Address: 1087 (43Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_LIMIT31:24]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

18.189 IMEM_SRAM_APEX_REG_1088

Name: IMEM_SRAM_APEX_REG_1088
Address: 1088 (440h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_TIME_LIMIT[7:0]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: in sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

18.190 IMEM_SRAM_APEX_REG_1089

Name: IMEM_SRAM_APEX_REG_1089
Address: 1089 (441h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_TIME_LIMIT[15:8]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: in sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

18.191 IMEM_SRAM_APEX_REG_1090

Name: IMEM_SRAM_APEX_REG_1090
Address: 1090 (442h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_TIME_LIMIT[23:16]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: in sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

18.192 IMEM_SRAM_APEX_REG_1091

Name: IMEM_SRAM_APEX_REG_1091
Address: 1091 (443h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_FAST_MOTION_TIME_LIMIT[31:24]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: in sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

18.193 IMEM_SRAM_APEX_REG_1092

Name: IMEM_SRAM_APEX_REG_1092
Address: 1092 (444h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_AGE_LIMIT[7:0]	Minimum time between 2 event b2s Unit: in sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

18.194 IMEM_SRAM_APEX_REG_1093

Name: IMEM_SRAM_APEX_REG_1093
Address: 1093 (445h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_AGE_LIMIT[15:8]	Minimum time between 2 event b2s Unit: in sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

18.195 IMEM_SRAM_APEX_REG_1094

Name: IMEM_SRAM_APEX_REG_1094
Address: 1094 (446h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_AGE_LIMIT[23:16]	Minimum time between 2 event b2s Unit: in sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

18.196 IMEM_SRAM_APEX_REG_1095

Name: IMEM_SRAM_APEX_REG_1095
Address: 1095 (447h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_AGE_LIMIT[31:24]	Minimum time between 2 event b2s Unit: in sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

18.197 IMEM_SRAM_APEX_REG_1096

Name: IMEM_SRAM_APEX_REG_1096
Address: 1096 (448h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_STATIC_LIMIT[7:0]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

18.198 IMEM_SRAM_APEX_REG_1097

Name: IMEM_SRAM_APEX_REG_1097
Address: 1097 (449h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_STATIC_LIMIT[15:8]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

18.199 IMEM_SRAM_APEX_REG_1098

Name: IMEM_SRAM_APEX_REG_1098
Address: 1098 (44Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_STATIC_LIMIT[23:16]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

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18.200 IMEM_SRAM_APEX_REG_1099

Name: IMEM_SRAM_APEX_REG_1099
Address: 1099 (44Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_STATIC_LIMIT[31:24]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

18.201 IMEM_SRAM_APEX_REG_1100

Name: IMEM_SRAM_APEX_REG_1100
Address: 1100 (44Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_THR_COS_ANGLE[7:0]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

18.202 IMEM_SRAM_APEX_REG_1101

Name: IMEM_SRAM_APEX_REG_1101
Address: 1101 (44Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_THR_COS_ANGLE[15:8]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

18.203 IMEM_SRAM_APEX_REG_1102

Name: IMEM_SRAM_APEX_REG_1102
Address: 1102 (44Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_THR_COS_ANGLE[23:16]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

18.204 IMEM_SRAM_APEX_REG_1103

Name: IMEM_SRAM_APEX_REG_1103
Address: 1103 (44Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_THR_COS_ANGLE[31:24]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

18.205 IMEM_SRAM_APEX_REG_1104

Name: IMEM_SRAM_APEX_REG_1104
Address: 1104 (450h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_REVB2S_LATENCY_THR[7:0]	Condition of RevB2S should be maintained at least during RevB2sLatencyTh Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

18.206 IMEM_SRAM_APEX_REG_1105

Name: IMEM_SRAM_APEX_REG_1105
Address: 1105 (451h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_REVB2S_LATENCY_THR[15:8]	Condition of RevB2S should be maintained at least during RevB2sLatencyTh Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

18.207 IMEM_SRAM_APEX_REG_1106

Name: IMEM_SRAM_APEX_REG_1106
Address: 1106 (452h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_REVB2S_LATENCY_THR[23:16]	Condition of RevB2S should be maintained at least during RevB2sLatencyTh Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

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18.208 IMEM_SRAM_APEX_REG_1107

Name: IMEM_SRAM_APEX_REG_1107
Address: 1107 (453h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	B2S_REVB2S_LATENCY_THR[31:24]	Condition of RevB2S should be maintained at least during RevB2sLatencyTh Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

18.209 IMEM_SRAM_APEX_REG_1280

Name: IMEM_SRAM_APEX_REG_1280
Address: 1280 (500h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_AXIS_MAJORITY_TH[7:0]	Used for shake axis detection. Axis detection threshold added before comparison between two axis to select the majority axis with this formula majority_axis_nb > minority_axis_nb + shake_axis_majority_th Unit: No unit, integer value Default value: 1 Format: int8_t

18.210 IMEM_SRAM_APEX_REG_1281

Name: IMEM_SRAM_APEX_REG_1281
Address: 1281 (501h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_AXIS_MAJORITY_TH[15:8]	Used for shake axis detection. Axis detection threshold added before comparison between two axis to select the majority axis with this formula majority_axis_nb > minority_axis_nb + shake_axis_majority_th Unit: No unit, integer value Default value: 1 Format: int8_t

18.211 IMEM_SRAM_APEX_REG_1282

Name: IMEM_SRAM_APEX_REG_1282
Address: 1282 (502h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_STATIC[7:0]	Threshold to stay below it before internal detection of static phase One threshold common for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2000, corresponding to 488mg Recommendation: Can be set lower to be more restrictive on static situation, can be set higher to allow static detection when user in movement (like medium walking, running) Format: int16_t

18.212 IMEM_SRAM_APEX_REG_1283

Name: IMEM_SRAM_APEX_REG_1283
Address: 1283 (503h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_STATIC[15:8]	Threshold to stay below it before internal detection of static phase One threshold common for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2000, corresponding to 488mg Recommendation: Can be set lower to be more restrictive on static situation, can be set higher to allow static detection when user in movement (like medium walking, running) Format: int16_t

18.213 IMEM_SRAM_APEX_REG_1284

Name: IMEM_SRAM_APEX_REG_1284
Address: 1284 (504h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MIN_STATIC_DURATION[7:0]	Time threshold to define the minimal duration of static phase to be valid Unit: In sample number, has ODR dependency Default value: 25, corresponding to 0.5s at 50Hz Recommendation: Use range value between [0.5s - 1.5s] Format: int16_t

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18.214 IMEM_SRAM_APEX_REG_1285

Name: IMEM_SRAM_APEX_REG_1285
Address: 1285 (505h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MIN_STATIC_DURATION[15:8]	Time threshold to define the minimal duration of static phase to be valid Unit: In sample number, has ODR dependency Default value: 25, corresponding to 0.5s at 50Hz Recommendation: Use range value between [0.5s - 1.5s] Format: int16_t

18.215 IMEM_SRAM_APEX_REG_1286

Name: IMEM_SRAM_APEX_REG_1286
Address: 1286 (506h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_MOTION[7:0]	Threshold to get out of the static phase and detect any motion (not specific to shake) One threshold common for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Can be set lower to be more restrictive on motion situation, can be set higher to allow keep in the static phase when user in movement (like medium walking, running) Format: int16_t

18.216 IMEM_SRAM_APEX_REG_1287

Name: IMEM_SRAM_APEX_REG_1287
Address: 1287 (507h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_MOTION[15:8]	Threshold to get out of the static phase and detect any motion (not specific to shake) One threshold common for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Can be set lower to be more restrictive on motion situation, can be set higher to allow keep in the static phase when user in movement (like medium walking, running) Format: int16_t

18.217 IMEM_SRAM_APEX_REG_1288

Name: IMEM_SRAM_APEX_REG_1288
Address: 1288 (508h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_X[7:0]	Threshold to be reached by the feature extracted during shake classification on x axis Link the amplitude of the signal on x axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.218 IMEM_SRAM_APEX_REG_1289

Name: IMEM_SRAM_APEX_REG_1289
Address: 1289 (509h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_X[15:8]	Threshold to be reached by the feature extracted during shake classification on x axis Link the amplitude of the signal on x axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.219 IMEM_SRAM_APEX_REG_1290

Name: IMEM_SRAM_APEX_REG_1290
Address: 1290 (50Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_Y[7:0]	Threshold to be reached by the feature extracted during shake classification on y axis Link the amplitude of the signal on y axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.220 IMEM_SRAM_APEX_REG_1291

Name: IMEM_SRAM_APEX_REG_1291
Address: 1291 (50Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_Y[15:8]	Threshold to be reached by the feature extracted during shake classification on y axis Link the amplitude of the signal on y axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.221 IMEM_SRAM_APEX_REG_1292

Name: IMEM_SRAM_APEX_REG_1292
Address: 1292 (50Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_Z[7:0]	Threshold to be reached by the feature extracted during shake classification on z axis Link the amplitude of the signal on z axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.222 IMEM_SRAM_APEX_REG_1293

Name: IMEM_SRAM_APEX_REG_1293
Address: 1293 (50Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_THR_SHAKE_Z[15:8]	Threshold to be reached by the feature extracted during shake classification on z axis Link the amplitude of the signal on z axis during the WINDOW_SHAKE Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2400, corresponding to 585mg Recommendation: Use lower value to detect shake with lower intensity Format: int16_t

18.223 IMEM_SRAM_APEX_REG_1294

Name: IMEM_SRAM_APEX_REG_1294
Address: 1294 (50Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MIN_SHAKE_DURATION[7:0]	Time threshold to define the minimal duration of shake to be valid Unit: In sample number, has ODR dependency Default value: 24, corresponding to 480ms at 50Hz Recommendation: Set the value as a multiple of internal_duration parameter Format: int16_t

18.224 IMEM_SRAM_APEX_REG_1295

Name: IMEM_SRAM_APEX_REG_1295
Address: 1295 (50Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MIN_SHAKE_DURATION[15:8]	Time threshold to define the minimal duration of shake to be valid Unit: In sample number, has ODR dependency Default value: 24, corresponding to 480ms at 50Hz Recommendation: Set the value as a multiple of internal_duration parameter Format: int16_t

18.225 IMEM_SRAM_APEX_REG_1296

Name: IMEM_SRAM_APEX_REG_1296
Address: 1296 (510h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MAX_SHAKE_DURATION[7:0]	Time threshold to define the maximal duration of shake to be valid Unit: In sample number, has ODR dependency Default value: 72, corresponding to 1.44s at 50Hz Recommendation: Set the value as a multiple of internal_duration parameter Format: int16_t

18.226 IMEM_SRAM_APEX_REG_1297

Name: IMEM_SRAM_APEX_REG_1297
Address: 1297 (511h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_MAX_SHAKE_DURATION[15:8]	Time threshold to define the maximal duration of shake to be valid Unit: In sample number, has ODR dependency Default value: 72, corresponding to 1.44s at 50Hz Recommendation: Set the value as a multiple of internal_duration parameter Format: int16_t

18.227 IMEM_SRAM_APEX_REG_1298

Name: IMEM_SRAM_APEX_REG_1298
Address: 1298 (512h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_INTERNAL_DURATION[7:0]	Internal time window for feature extraction to classify shake in progress once motion is internally detected Unit: In sample number, has ODR dependency Default value: 8, corresponding to 160ms at 50Hz Recommendation: Use range [8-16] Format: int16_t

18.228 IMEM_SRAM_APEX_REG_1299

Name: IMEM_SRAM_APEX_REG_1299
Address: 1299 (513h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_INTERNAL_DURATION[15:8]	Internal time window for feature extraction to classify shake in progress once motion is internally detected Unit: In sample number, has ODR dependency Default value: 8, corresponding to 160ms at 50Hz Recommendation: Use range [8-16] Format: int16_t

18.229 IMEM_SRAM_APEX_REG_1300

Name: IMEM_SRAM_APEX_REG_1300
Address: 1300 (514h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_AXIS_DETECTION_FACTOR[7:0]	Axis detection factor to consider an axis as major one Formula is major_axis_feature*axis_detection_factor > minor_axis_feature Unit: No unit, with a q12 coding value Default value: 2048, corresponding to value 0.5 Format: int16_t

18.230 IMEM_SRAM_APEX_REG_1301

Name: IMEM_SRAM_APEX_REG_1301
Address: 1301 (515h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SHAKE_AXIS_DETECTION_FACTOR[15:8]	Axis detection factor to consider an axis as major one Formula is major_axis_feature*axis_detection_factor > minor_axis_feature Unit: No unit, with a q12 coding value Default value: 2048, corresponding to value 0.5 Format: int16_t

18.231 IMEM_SRAM_APEX_REG_1314

Name: IMEM_SRAM_APEX_REG_1314
Address: 1314 (522h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_THR_STATIC[7:0]	Amplitude threshold of the static criteria for each axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 80, corresponding to 19 mg - relative to sensor noise Format: int16_t

18.232 IMEM_SRAM_APEX_REG_1315

Name: IMEM_SRAM_APEX_REG_1315
Address: 1315 (523h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_THR_STATIC[15:8]	Amplitude threshold of the static criteria for each axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 80, corresponding to 19 mg - relative to sensor noise Format: int16_t

18.233 IMEM_SRAM_APEX_REG_1316

Name: IMEM_SRAM_APEX_REG_1316
Address: 1316 (524h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_MIN_STATIC_DURATION[7:0]	Minimal duration of static detection before triggering the status no motion Unit: In sample number - ODR dependent Default value: 150, corresponding to 3s at 50Hz Format: int16_t

18.234 IMEM_SRAM_APEX_REG_1317

Name: IMEM_SRAM_APEX_REG_1317
Address: 1317 (525h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_MIN_STATIC_DURATION[15:8]	Minimal duration of static detection before triggering the status no motion Unit: In sample number - ODR dependent Default value: 150, corresponding to 3s at 50Hz Format: int16_t

18.235 IMEM_SRAM_APEX_REG_1318

Name: IMEM_SRAM_APEX_REG_1318
Address: 1318 (526h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_THR_MOTION[7:0]	Amplitude threshold of the motion criteria for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 819, corresponding to 200mg Format: int16_t

18.236 IMEM_SRAM_APEX_REG_1319

Name: IMEM_SRAM_APEX_REG_1319
Address: 1319 (527h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	NOMOTION_THR_MOTION[15:8]	Amplitude threshold of the motion criteria for each axis Unit: in LSB, with 1 LBS = 1g / 2^12 Default value: 819, corresponding to 200mg Format: int16_t

18.237 IMEM_SRAM_APEX_REG_1364

Name: IMEM_SRAM_APEX_REG_1364
Address: 1364 (554h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_ONLY_GAIN_FAST_CONV[7:0]	Gain value to handle smoothing of 3axis reactivity Format: q30 in int32_t Unit: N/A Default: 100663296 = q30(0.09375)

18.238 IMEM_SRAM_APEX_REG_1365

Name: IMEM_SRAM_APEX_REG_1365
Address: 1365 (555h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_ONLY_GAIN_FAST_CONV[15:8]	Gain value to handle smoothing of 3axis reactivity Format: q30 in int32_t Unit: N/A Default: 100663296 = q30(0.09375)

18.239 IMEM_SRAM_APEX_REG_1366

Name: IMEM_SRAM_APEX_REG_1366
Address: 1366 (556h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_ONLY_GAIN_FAST_CONV[23:16]	Gain value to handle smoothing of 3axis reactivity Format: q30 in int32_t Unit: N/A Default: 100663296 = q30(0.09375)

18.240 IMEM_SRAM_APEX_REG_1367

Name: IMEM_SRAM_APEX_REG_1367
Address: 1367 (557h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_ONLY_GAIN_FAST_CONV[31:24]	Gain value to handle smoothing of 3axis reactivity Format: q30 in int32_t Unit: N/A Default: 100663296 = q30(0.09375)

18.241 IMEM_SRAM_APEX_REG_1396

Name: IMEM_SRAM_APEX_REG_1396
Address: 1396 (574h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_SELECTION[7:0]	Specify which axis to consider as reference and set ref_axis in consequence 0 -> X axis (1,0,0) 1 -> Y axis (0,1,0) 2 -> Z axis (0,0,1) 3 -> Advanced (a 3d vector must be provided by the user) Default value: 2, Z axis corresponding to vertical in android reference Format: uint16_t

18.242 IMEM_SRAM_APEX_REG_1397

Name: IMEM_SRAM_APEX_REG_1397
Address: 1397 (575h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_SELECTION[15:8]	Specify which axis to consider as reference and set ref_axis in consequence 0 -> X axis (1,0,0) 1 -> Y axis (0,1,0) 2 -> Z axis (0,0,1) 3 -> Advanced (a 3d vector must be provided by the user) Default value: 2, Z axis corresponding to vertical in android reference Format: uint16_t

18.243 IMEM_SRAM_APEX_REG_1398

Name: IMEM_SRAM_APEX_REG_1398
Address: 1398 (576h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_ISSYMETRICAL[7:0]	Symmetry flag defining algo behavior (symmetrical or asymmetrical with ref_axis) Unit: enum, 1 for symmetrical, 0 for asymmetrical Default value: 1, symmetrical Format: uint16_t

18.244 IMEM_SRAM_APEX_REG_1399

Name: IMEM_SRAM_APEX_REG_1399
Address: 1399 (577h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_ISSYMETRICAL[15:8]	Symmetry flag defining algo behavior (symmetrical or asymmetrical with ref_axis) Unit: enum, 1 for symmetrical, 0 for asymmetrical Default value: 1, symmetrical Format: uint16_t

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18.245 IMEM_SRAM_APEX_REG_1400

Name: IMEM_SRAM_APEX_REG_1400
Address: 1400 (578h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_THREE_AXIS_CONV_TIME[7:0]	Specify convergence time (in samples) for convergence of orientation estimation Unit: In sample number - ODR dependent Algorithm detection is disabled during initialization Default value: 50, corresponding to 1s at 50Hz Format: uint16_t

18.246 IMEM_SRAM_APEX_REG_1401

Name: IMEM_SRAM_APEX_REG_1401
Address: 1401 (579h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_THREE_AXIS_CONV_TIME[15:8]	Specify convergence time (in samples) for convergence of orientation estimation Unit: In sample number - ODR dependent Algorithm detection is disabled during initialization Default value: 50, corresponding to 1s at 50Hz Format: uint16_t

18.247 IMEM_SRAM_APEX_REG_1402

Name: IMEM_SRAM_APEX_REG_1402
Address: 1402 (57Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_WAIT_TIME[7:0]	Wait time after the flat/no flat angle is reached and maintained to trigger the flat/no flat event Unit: In sample number - ODR dependent Default value: 10, corresponding to 200ms at 50Hz Format: uint16_t

18.248 IMEM_SRAM_APEX_REG_1403

Name: IMEM_SRAM_APEX_REG_1403
Address: 1403 (57Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_WAIT_TIME[15:8]	Wait time after the flat/no flat angle is reached and maintained to trigger the flat/no flat event Unit: In sample number - ODR dependent Default value: 10, corresponding to 200ms at 50Hz Format: uint16_t

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Revision: 1.0

18.249 IMEM_SRAM_APEX_REG_1404

Name: IMEM_SRAM_APEX_REG_1404
Address: 1404 (57Ch)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_COS_FLAT_ANGLE_TH[7:0]	The threshold tilt angle compared to reference vector to detect flat / no flat Unit: Cosine value of angle in q30 Default value: 1057429273, corresponding to 10° Format: int32_t

18.250 IMEM_SRAM_APEX_REG_1405

Name: IMEM_SRAM_APEX_REG_1405
Address: 1405 (57Dh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_COS_FLAT_ANGLE_TH[15:8]	The threshold tilt angle compared to reference vector to detect flat / no flat Unit: Cosine value of angle in q30 Default value: 1057429273, corresponding to 10° Format: int32_t

18.251 IMEM_SRAM_APEX_REG_1406

Name: IMEM_SRAM_APEX_REG_1406
Address: 1406 (57Eh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_COS_FLAT_ANGLE_TH[23:16]	The threshold tilt angle compared to reference vector to detect flat / no flat Unit: Cosine value of angle in q30 Default value: 1057429273, corresponding to 10° Format: int32_t

18.252 IMEM_SRAM_APEX_REG_1407

Name: IMEM_SRAM_APEX_REG_1407
Address: 1407 (57Fh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_COS_FLAT_ANGLE_TH[31:24]	The threshold tilt angle compared to reference vector to detect flat / no flat Unit: Cosine value of angle in q30 Default value: 1057429273, corresponding to 10° Format: int32_t

18.253 IMEM_SRAM_APEX_REG_1408

Name: IMEM_SRAM_APEX_REG_1408
Address: 1408 (580h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_X[7:0]	Reference value for x axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.254 IMEM_SRAM_APEX_REG_1409

Name: IMEM_SRAM_APEX_REG_1409
Address: 1409 (581h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_X[15:8]	Reference value for x axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.255 IMEM_SRAM_APEX_REG_1410

Name: IMEM_SRAM_APEX_REG_1410
Address: 1410 (582h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_X[23:16]	Reference value for x axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.256 IMEM_SRAM_APEX_REG_1411

Name: IMEM_SRAM_APEX_REG_1411
Address: 1411 (583h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_X[31:24]	Reference value for x axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.257 IMEM_SRAM_APEX_REG_1412

Name: IMEM_SRAM_APEX_REG_1412
Address: 1412 (584h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Y[7:0]	Reference value for y axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.258 IMEM_SRAM_APEX_REG_1413

Name: IMEM_SRAM_APEX_REG_1413
Address: 1413 (585h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Y[15:8]	Reference value for y axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.259 IMEM_SRAM_APEX_REG_1414

Name: IMEM_SRAM_APEX_REG_1414
Address: 1414 (586h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Y[23:16]	Reference value for y axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.260 IMEM_SRAM_APEX_REG_1415

Name: IMEM_SRAM_APEX_REG_1415
Address: 1415 (587h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Y[31:24]	Reference value for y axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.261 IMEM_SRAM_APEX_REG_1416

Name: IMEM_SRAM_APEX_REG_1416
Address: 1416 (588h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Z[7:0]	Reference value for z axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.262 IMEM_SRAM_APEX_REG_1417

Name: IMEM_SRAM_APEX_REG_1417
Address: 1417 (589h)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Z[15:8]	Reference value for z axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.263 IMEM_SRAM_APEX_REG_1418

Name: IMEM_SRAM_APEX_REG_1418
Address: 1418 (58Ah)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Z[23:16]	Reference value for z axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

18.264 IMEM_SRAM_APEX_REG_1419

Name: IMEM_SRAM_APEX_REG_1419
Address: 1419 (58Bh)
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FLAT_REF_AXIS_Z[31:24]	Reference value for z axis Unit: in LSB, with 1 LBS = 1g / 2^30 Default value: 0 Format: int32_t

19 USER BANK IMEM_SRAM_STC REGISTER MAP – DESCRIPTIONS

19.1 IMEM_SRAM_STC_REG_56

Name: IMEM_SRAM_STC_REG_56
Address: 56 (38h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_configparams[7:0]	bit0 (self_test_init_en) 0: Disabled; 1: Enabled bit1 (accel_self_test_en) 0: Disabled; 1: Enabled bit2 (gyro_self_test_en) 0: Disabled; 1: Enabled bits3-6: Reserved bits7-9 (self_test_average_time) 0: 10ms; 1: 20ms; 2: 40ms; 3: 80ms; 4: 160ms; 5: 320ms (correspond respectively to 8/16/32/64/128/256 samples @800Hz) bits10-12 (accel_self_test_threshold) 0: 5; 1: 10; 2: 15; 3: 20; 4: 25; 5: 30; 6: 40; 7: 50 bits13-15 (gyro_self_test_threshold) 0: 5; 1: 10; 2: 15; 3: 20; 4: 25; 5: 30; 6: 40; 7: 50 bits16-31: Reserved

19.2 IMEM_SRAM_STC_REG_57

Name: IMEM_SRAM_STC_REG_57
Address: 57 (39h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_configparams[15:8]	bit0 (self_test_init_en) 0: Disabled; 1: Enabled bit1 (accel_self_test_en) 0: Disabled; 1: Enabled bit2 (gyro_self_test_en) 0: Disabled; 1: Enabled bits3-6: Reserved bits7-9 (self_test_average_time) 0: 10ms; 1: 20ms; 2: 40ms; 3: 80ms; 4: 160ms; 5: 320ms (correspond respectively to 8/16/32/64/128/256 samples @800Hz) bits10-12 (accel_self_test_threshold) 0: 5; 1: 10; 2: 15; 3: 20; 4: 25; 5: 30; 6: 40; 7: 50 bits13-15 (gyro_self_test_threshold) 0: 5; 1: 10; 2: 15; 3: 20; 4: 25; 5: 30; 6: 40; 7: 50 bits16-31: Reserved

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19.3 IMEM_SRAM_STC_REG_60

Name: IMEM_SRAM_STC_REG_60
Address: 60 (3Ch)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_patch_en[7:0]	bit0 (patch_en_self_test_accel_phase1) 0: Disabled; 1: Enabled bit1 (patch_en_self_test_accel_phase2) 0: Disabled; 1: Enabled bit2 (patch_en_self_test_gyro1_phase1) 0: Disabled; 1: Enabled bit3 (patch_en_self_test_gyro1_phase2) 0: Disabled; 1: Enabled bits4-7: Reserved

19.4 IMEM_SRAM_STC_REG_64

Name: IMEM_SRAM_STC_REG_64
Address: 64 (40h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_debug_en[7:0]	Debug capability of self-test feature. Must be set to 0 when self-test is requested.

19.5 IMEM_SRAM_STC_REG_65

Name: IMEM_SRAM_STC_REG_65
Address: 65 (41h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_debug_en[15:8]	Debug capability of self-test feature. Must be set to 0 when self-test is requested.

19.6 IMEM_SRAM_STC_REG_66

Name: IMEM_SRAM_STC_REG_66
Address: 66 (42h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_debug_en[23:16]	Debug capability of self-test feature. Must be set to 0 when self-test is requested.

19.7 IMEM_SRAM_STC_REG_67

Name: IMEM_SRAM_STC_REG_67
Address: 67 (43h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_debug_en[31:24]	Debug capability of self-test feature. Must be set to 0 when self-test is requested.

19.8 IMEM_SRAM_STC_REG_68

Name: IMEM_SRAM_STC_REG_68
Address: 68 (44h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	stc_results[7:0]	bit0 (accel_x_self_test_result) 0: Passed; 1: Failed bit1 (accel_y_self_test_result) 0: Passed; 1: Failed bit2 (accel_z_self_test_result) 0: Passed; 1: Failed bit3 (gyro_x_self_test_result) 0: Passed; 1: Failed bit4 (gyro_y_self_test_result) 0: Passed; 1: Failed bit5 (gyro_z_self_test_result) 0: Passed; 1: Failed bits6-7 (self_test_status) 0: Done 1: In-Progress 2: Error

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20 USER BANK IPREG_SYS1 REGISTER MAP – DESCRIPTIONS

20.1 IPREG_SYS1_REG_0

Name: IPREG_SYS1_REG_0
Address: 00 (00h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SIGP_DATA_INJ_TMP[7:0]	Temperature sensor signal path test mode data injection value

20.2 IPREG_SYS1_REG_1

Name: IPREG_SYS1_REG_1
Address: 01 (01h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SIGP_DATA_INJ_TMP[15:8]	Temperature sensor signal path test mode data injection value

20.3 IPREG_SYS1_REG_2

Name: IPREG_SYS1_REG_2
Address: 02 (02h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_X_OFFUSER[7:0]	Gyro X axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

20.4 IPREG_SYS1_REG_3

Name: IPREG_SYS1_REG_3
Address: 03 (03h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	GYRO_X_OFFUSER[13:8]	Gyro X axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

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20.5 IPREG_SYS1_REG_4

Name: IPREG_SYS1_REG_4
Address: 04 (04h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Y_OFFUSER[7:0]	Gyro Y axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

20.6 IPREG_SYS1_REG_5

Name: IPREG_SYS1_REG_5
Address: 05 (05h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	GYRO_Y_OFFUSER[13:8]	Gyro Y axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

20.7 IPREG_SYS1_REG_6

Name: IPREG_SYS1_REG_6
Address: 06 (06h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Z_OFFUSER[7:0]	Gyro Z axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

20.8 IPREG_SYS1_REG_7

Name: IPREG_SYS1_REG_7
Address: 07 (07h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	GYRO_Z_OFFUSER[13:8]	Gyro Z axis USER offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps

20.9 IPREG_SYS1_REG_8

Name: IPREG_SYS1_REG_8
Address: 08 (08h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_X_USERGAIN[7:0]	Gyro X axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.10 IPREG_SYS1_REG_9

Name: IPREG_SYS1_REG_9
Address: 09 (09h)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_X_USERGAIN[11:8]	Gyro X axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.11 IPREG_SYS1_REG_10

Name: IPREG_SYS1_REG_10
Address: 10 (0Ah)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Y_USERGAIN[7:0]	Gyro Y axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.12 IPREG_SYS1_REG_11

Name: IPREG_SYS1_REG_11
Address: 11 (0Bh)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_Y_USERGAIN[11:8]	Gyro Y axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.13 IPREG_SYS1_REG_12

Name: IPREG_SYS1_REG_12
Address: 12 (0Ch)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	GYRO_Z_USERGAIN[7:0]	Gyro Z axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.14 IPREG_SYS1_REG_13

Name: IPREG_SYS1_REG_13
Address: 13 (0Dh)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	GYRO_Z_USERGAIN[11:8]	Gyro Z axis USER gain Range: 0 to 2 Resolution: 2^-11 (~0.05%)

20.15 IPREG_SYS1_REG_146

Name: IPREG_SYS1_REG_146
Address: 146 (92h)
Reset value: 0x86
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	GYRO_X_TMID_OFF[3:0]	Gyro X-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	GYRO_X_TMID_GAIN[3:0]	Gyro X-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

20.16 IPREG_SYS1_REG_148

Name: IPREG_SYS1_REG_148
Address: 148 (94h)
Reset value: 0x86
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	GYRO_Y_TMID_OFF[3:0]	Gyro Y-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	GYRO_Y_TMID_GAIN[3:0]	Gyro Y-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

20.17 IPREG_SYS1_REG_150

Name: IPREG_SYS1_REG_150
Address: 150 (96h)
Reset value: 0x86
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	GYRO_Z_TMID_OFF[3:0]	Gyro Z-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	GYRO_Z_TMID_GAIN[3:0]	Gyro Z-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

20.18 IPREG_SYS1_REG_154

Name: IPREG_SYS1_REG_154
Address: 154 (9Ah)
Reset value: 0x20
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	GYRO_OIS_M6_BYP[0]	Gyro OIS path M6 filter bypass Filter with zeros at 1.066 kHz and multiples 0: M6 filter is enabled 1: M6 filter is bypassed
[4]	-	-	Reserved
[3:2]	R/W	GYRO_SRC_CTRL[1:0]	Gyro Sample Rate Converter (SRC) Control. 0: SRC off and Pre-filter off 1: SRC off and Pre-filter on 2: SRC on and Pre-filter on 3: Reserved
[1:0]	-	-	Reserved

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20.19 IPREG_SYS1_REG_155

Name: IPREG_SYS1_REG_155
Address: 155 (9Bh)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R/W	GYRO_LPF_BYPASS[0]	Gyro UI path Low Pass Filter bypass 0: LPF is enabled 1: LPF is bypassed
[0]	R/W	GYRO_OIS_HPF_BYP[0]	Gyro OIS path High Pass Filter bypass 0: HPF is enabled 1: HPF is bypassed

20.20 IPREG_SYS1_REG_157

Name: IPREG_SYS1_REG_157
Address: 157 (9Dh)
Reset value: 0x05
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	GYRO_NOTCH_BYPASS[0]	Gyro UI/OIS/LPM path: disable the Notch Filter 0: Notch Filter enabled 1: Notch Filter bypassed
[6:4]	R/W	GYRO_OIS_HPFBW_SEL[2:0]	Gyro OIS path: High Pass Filter cutoff frequency 0: bypass 1: 1Hz 2: 0.25Hz 3: 0.062Hz 4: 0.016Hz
[3:0]	R/W	GYRO_LP_AVG_SEL[3:0]	Gyro Low Power Mode Average Selection 0: Avgs=1 1: Avgs=2 2: Avgs=4 3: Avgs=5 4: Avgs=7 5: Avgs=8 6: Avgs=10 7: Avgs=11 8: Avgs=16 9: Avgs=18 10: Avgs=20 11: Avgs=32 12-15: Avgs=64

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20.21 IPREG_SYS1_REG_158

Name: IPREG_SYS1_REG_158
Address: 158 (9Eh)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	GYRO_UI_3RD_ORD_SEL[0]	Gyro UI path: Anti-Alias and low pass filter order selection 0: 1st order low-pass 1: 3rd order low-pass
[6:4]	R/W	GYRO_UI_LPFBW_SEL[2:0]	Gyro UI path: Low Pass Filter nominal cutoff frequency 0: ODR/2 (LP bypass) 1: ODR/4 2: ODR/8 3: ODR/16 4: ODR/32 5: ODR/64 6,7: ODR/128 NOTE: The real bandwidth is smaller than the nominal one at high ODR or BW
[3]	R/W	GYRO_OIS_3RD_ORD_SEL[0]	Gyro OIS path: low pass filter order selection 0: 1st order low-pass 1: 3rd order low-pass
[2:0]	R/W	GYRO_OIS_LPFBW_SEL[2:0]	Gyro OIS path: Low Pass Filter cutoff frequency 0: 1650 Hz (LP bypass) 1: 1250 Hz 2: 727 Hz 3: 390 Hz 4: 198 Hz 5: 99 Hz 6,7: 49 Hz

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21 USER BANK IPREG_SYS2 REGISTER MAP – DESCRIPTIONS

21.1 IPREG_SYS2_REG_12

Name: IPREG_SYS2_REG_12
Address: 12 (0Ch)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_X_OFFUSER[7:0]	Accel X axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

21.2 IPREG_SYS2_REG_13

Name: IPREG_SYS2_REG_13
Address: 13 (0Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	ACCEL_X_OFFUSER[13:8]	Accel X axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

21.3 IPREG_SYS2_REG_14

Name: IPREG_SYS2_REG_14
Address: 14 (0Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Y_OFFUSER[7:0]	Accel Y axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

21.4 IPREG_SYS2_REG_15

Name: IPREG_SYS2_REG_15
Address: 15 (0Fh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	ACCEL_Y_OFFUSER[13:8]	Accel Y axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

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21.5 IPREG_SYS2_REG_16

Name: IPREG_SYS2_REG_16
Address: 16 (10h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Z_OFFUSER[7:0]	Accel Z axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

21.6 IPREG_SYS2_REG_17

Name: IPREG_SYS2_REG_17
Address: 17 (11h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:0]	R/W	ACCEL_Z_OFFUSER[13:8]	Accel Z axis USER Offset adjustment Range: ±1 gee Resolution: 0.122 mgee

21.7 IPREG_SYS2_REG_18

Name: IPREG_SYS2_REG_18
Address: 18 (12h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_X_USERGAIN[7:0]	Accel X axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.8 IPREG_SYS2_REG_19

Name: IPREG_SYS2_REG_19
Address: 19 (13h)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	ACCEL_X_USERGAIN[11:8]	Accel X axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.9 IPREG_SYS2_REG_20

Name: IPREG_SYS2_REG_20
Address: 20 (14h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Y_USERGAIN[7:0]	Accel Y axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.10 IPREG_SYS2_REG_21

Name: IPREG_SYS2_REG_21
Address: 21 (15h)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	ACCEL_Y_USERGAIN[11:8]	Accel Y axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.11 IPREG_SYS2_REG_22

Name: IPREG_SYS2_REG_22
Address: 22 (16h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	ACCEL_Z_USERGAIN[7:0]	Accel Z axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.12 IPREG_SYS2_REG_23

Name: IPREG_SYS2_REG_23
Address: 23 (17h)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3:0]	R/W	ACCEL_Z_USERGAIN[11:8]	Accel Z axis USER gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%)

21.13 IPREG_SYS2_REG_105

Name: IPREG_SYS2_REG_105
Address: 105 (69h)
Reset value: 0x66
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	ACCEL_X_TMID_OFF[3:0]	Accel X-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	ACCEL_X_TMID_GAIN[3:0]	Accel X-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

21.14 IPREG_SYS2_REG_106

Name: IPREG_SYS2_REG_106
Address: 106 (6Ah)
Reset value: 0x66
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	ACCEL_Y_TMID_OFF[3:0]	Accel Y-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	ACCEL_Y_TMID_GAIN[3:0]	Accel Y-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

21.15 IPREG_SYS2_REG_107

Name: IPREG_SYS2_REG_107
Address: 107 (6Bh)
Reset value: 0x66
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	ACCEL_Z_TMID_OFF[3:0]	Accel Z-axis dual-slope Offset: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC
[3:0]	R/W	ACCEL_Z_TMID_GAIN[3:0]	Accel Z-axis dual-slope Gain: Temperature inflection point (Tmid) 0: Tmid = -28 ºC 1: Tmid = -20 ºC 2: Tmid = -12 ºC 3: Tmid = -4 ºC 4: Tmid = 4 ºC 5: Tmid = 12 ºC 6: Tmid = 20 ºC 7: Tmid = 28 ºC 8: Tmid = 36 ºC 9: Tmid = 44 ºC 10: Tmid = 52 ºC >=11: Tmid = 60 ºC

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21.16 IPREG_SYS2_REG_109

Name: IPREG_SYS2_REG_109
Address: 109 (6Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1:0]	R/W	ACCEL_SRC_CTRL[1:0]	Accel Sample Rate Converter (SRC) Control. 0: SRC off and Pre-filter off 1: SRC off and Pre-filter on 2: SRC on and Pre-filter on 3: Reserved

21.17 IPREG_SYS2_REG_110

Name: IPREG_SYS2_REG_110
Address: 110 (6Eh)
Reset value: 0x02
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6:4]	R/W	ACCEL_OIS_HPFBW_SEL[2:0]	Accel OIS path: High Pass Filter cutoff frequency 0: Bypass 1: 1Hz 2: 250MHz 3: 62MHz 4: 16MHz
[3:0]	R/W	ACCEL_LP_AVG_SEL[3:0]	Accel Low Power Mode Average Selection 0: Avgs=1 1: Avgs=2 2: Avgs=4 3: Avgs=5 4: Avgs=7 5: Avgs=8 6: Avgs=10 7: Avgs=11 8: Avgs=16 9: Avgs=18 10: Avgs=20 11: Avgs=32 12-15: Avgs=64

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21.18 IPREG_SYS2_REG_111

Name: IPREG_SYS2_REG_111
Address: 111 (6Fh)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	ACCEL_OIS_3RD_ORD_SEL[0]	Accel OIS path: low pass filter order selection 0: 1st order low-pass 1: 3rd order low-pass
[2:0]	R/W	ACCEL_OIS_LPFBW_SEL[2:0]	Accel OIS path: Low Pass Filter cutoff frequency 0: 1650 Hz (LP bypass) 1: 1250 Hz 2: 727 Hz 3: 390 Hz 4: 198 Hz 5: 99 Hz 6,7: 49 Hz

21.19 IPREG_SYS2_REG_112

Name: IPREG_SYS2_REG_112
Address: 112 (70h)
Reset value: 0x20
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	ACCEL_OIS_M6_BYP[0]	Accel OIS path M6 filter bypass Filter with zeros at 1.066 kHz and multiples 0: M6 filter is enabled 1: M6 filter is bypassed
[5]	R/W	ACCEL_OIS_HPF_BYP[0]	Accel OIS path High Pass Filter bypass 0: HPF is enabled 1: HPF is bypassed
[4]	R/W	ACCEL_LPF_BYPASS[0]	Accel UI path Low Pass Filter bypass 0: LPF is enabled 1: LPF is bypassed
[3]	R/W	ACCEL_UI_3RD_ORD_SEL[0]	Accel UI path: Anti-Alias and low pass filter order selection 0: 1st order low-pass 1: 3rd order low-pass
[2:0]	R/W	ACCEL_UI_LPFBW_SEL[2:0]	Accel UI path: Low Pass Filter nominal cutoff frequency 0: ODR/2 (LP bypass) 1: ODR/4 2: ODR/8 3: ODR/16 4: ODR/32 5: ODR/64 6,7: ODR/128 NOTE: The real bandwidth is smaller than the nominal one at high ODR or BW

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21.20 IPREG_SYS2_REG_117

Name: IPREG_SYS2_REG_117
Address: 117 (75h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6:4]	R/W	TMP_DEC_CFG[2:0]	Temperature Sensor ODR selection (Dec config). ADC_CLK depends on power mode, ACCEL_ODR_TEMP and GYRO_ODR_TEMP values 0: ADC_CLK 1: ADC_CLK/2 2: ADC_CLK/4 3: ADC_CLK/8 4: ADC_CLK/16 5: ADC_CLK/32 6: ADC_CLK/64 7: ADC_CLK/128
[3:1]	R/W	TMP_LPF_CFG[2:0]	Temperature sensor. Low-Pass filter BW selection (LNM) 0: LPF bypass 1: 1/4 Temp Data Rate 2: 1/6 Temp Data Rate 3: 1/10 Temp Data Rate 4: 1/20 Temp Data Rate 5: 1/50 Temp Data Rate 6,7: 1/100 Temp Data Rate
[0]	R/W	TMP_INJ_EN_GOS[0]	Temperature Sensor signal path test mode 0: No data injected into GOS input 1: Data injected into GOS input and LPF (see SIGP_DATA_INJ_TMP field)

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22.1 EDMP_PRGRM_IRQ0_0

Name: EDMP_PRGRM_IRQ0_0
Address: 79 (4Fh)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_0[7:0]	Start address of IRQ_0 vector. Can be changed on-the-fly.

22.2 EDMP_PRGRM_IRQ0_1

Name: EDMP_PRGRM_IRQ0_1
Address: 80 (50h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_0[15:8]	Start address of IRQ_0 vector. Can be changed on-the-fly.

22.3 EDMP_PRGRM_IRQ1_0

Name: EDMP_PRGRM_IRQ1_0
Address: 81 (51h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_1[7:0]	Start address of IRQ_1 vector. Can be changed on-the-fly.

22.4 EDMP_PRGRM_IRQ1_1

Name: EDMP_PRGRM_IRQ1_1
Address: 82 (52h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_1[15:8]	Start address of IRQ_1 vector. Can be changed on-the-fly.

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22.5 EDMP_PRGRM_IRQ2_0

Name: EDMP_PRGRM_IRQ2_0
Address: 83 (53h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_2[7:0]	Start address of IRQ_2 vector. Can be changed on-the-fly.

22.6 EDMP_PRGRM_IRQ2_1

Name: EDMP_PRGRM_IRQ2_1
Address: 84 (54h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	PRGRM_STRT_ADDR_IRQ_2[15:8]	Start address of IRQ_2 vector. Can be changed on-the-fly.

22.7 EDMP_SP_START_ADDR

Name: EDMP_SP_START_ADDR
Address: 85 (55h)
Reset value: 0x00
Clock Domain(s): MCLK

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	SP_START_ADDR[7:0]	Sets eDMP stack address. Can be changed on-the-fly.

22.8 SMC_CONTROL_0

Name: SMC_CONTROL_0
Address: 88 (58h)
Reset value: 0x60
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2]	R/W	TMST_FORCE_AUX_FINE_EN[0]	1 forces Time Stamp fine counting also on OIS/AUX interfaces. Otherwise, if 0, Time Stamp fine counting is enabled only on UI/AP interface.
[1]	R/W	TMST_FSYNC_EN[0]	Time Stamp register FSYNC Enable When set to 1, the contents of the Timestamp feature of FSYNC is enabled
[0]	R/W	TMST_EN[0]	Time Stamp register Enable

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22.9 SREG_CTRL

Name: SREG_CTRL Address: 96 (60h) Reset value: 0x0A Clock Domain(s): mclk			
BIT	**ACCESS**	**NAME**	**DESCRIPTION**
[7:4]	-	-	Reserved
[3]	R/W	SREG_SIFS_20BITS_EN[0]	Select the resolution of the sensor registers outputs 0: 16-bits sensor register output 1: 20-bits sensor register output. Registers ACCEL_DATA_X_0/1, ACCEL_DATA_Y_0/1, ACCEL_DATA_Z_0/1, GYRO_DATA_X_0/1, GYRO_DATA_Y_0/1, GYRO_DATA_Z_0/1 contain the most significant bits [19:4], while registers EXT_DATA_X, EXT_DATA_Y, EXT_DATA_Z contains the least significant bits [3:0] for both Accel and Gyro
[2]	-	-	Reserved
[1]	R/W	SREG_DATA_ENDIAN_SEL[0]	Select the endianness of the Sensor Data Registers and FIFO data 0: Sensor Registers and FIFO data is in Little Endian format 1: Sensor Registers and FIFO data is in Big Endian format
[0]	-	-	Reserved

22.10 INT_PULSE_MIN_ON_INTF0

Name: INT_PULSE_MIN_ON_INTF0 Address: 98 (62h) Reset value: 0x01 Clock Domain(s): mclk			
BIT	**ACCESS**	**NAME**	**DESCRIPTION**
[7:3]	-	-	Reserved
[2:0]	R/W	INT0_TPULSE_DURATION[2:0]	UI/AP Interface: INT0 pulse Min "on" duration, indicates minimum interrupt assertion duration when in pulse mode. 0: Interrupt pulse duration is 100us. Use only if ODR < 4KHz (Default). 1: Interrupt pulse duration is 8us. Required if ODR >= 4KHz, optional for ODR < 4KHz. 2,3,4,5,6,7: Reserved.

22.11 INT_PULSE_MIN_ON_INTF1

Name: INT_PULSE_MIN_ON_INTF1
Address: 99 (63h)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2:0]	R/W	INT1_TPULSE_DURATION[2:0]	UI/AP Interface: INT1 pulse Min "on" duration, indicates minimum interrupt assertion duration when in pulse mode. 0: Interrupt pulse duration is 100us. Use only if ODR < 4KHz (Default). 1: Interrupt pulse duration is 8us. Required if ODR >= 4KHz, optional for ODR < 4KHz. 2,3,4,5,6,7: Reserved.

22.12 INT_PULSE_MIN_OFF_INTF0

Name: INT_PULSE_MIN_OFF_INTF0
Address: 100 (64h)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2:0]	R/W	INT0_TDEASSERT_DISABLE[2:0]	Interface UI/AP: INT0 min "off" duration, indicates Minimum interrupt de-assertion duration. 0: 100us [default] 1: 8us 2: No minimum interrupt de-assertion duration requirement. Two back-to-back interrupt assertions could be separated by at least one MCLK cycle. This option should be used for MCU and IBI interface only. 3,4,5,6,7: Reserved.

22.13 INT_PULSE_MIN_OFF_INTF1

Name: INT_PULSE_MIN_OFF_INTF1
Address: 101 (65h)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2:0]	R/W	INT1_TDEASSERT_DISABLE[2:0]	Interface UI/AP: INT1 min "off" duration, indicates Minimum interrupt de-assertion duration. 0: 100us [default] 1: 8us 2: No minimum interrupt de-assertion duration requirement. Two back-to-back interrupt assertions could be separated by at least one MCLK cycle. This option should be used for MCU and IBI interface only. 3,4,5,6,7: Reserved.

22.14 STATUS_MASK_PIN_0_7

Name: STATUS_MASK_PIN_0_7
Address: 106 (6Ah)
Reset value: 0x3F
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	INT_ON_DEMAND_PIN_0_DIS[0]	For edmp (irq0) interface, indicates on demand masking bit for irq0 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[4]	R/W	INT_WOM_DRDY_PIN_0_DIS[0]	For edmp (irq0) interface, indicates Wake On Motion event ORing of X, Y, and Z axis masking bit for irq0 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[3:2]	-	-	Reserved
[1]	R/W	INT_GYRO_DRDY_PIN_0_DIS[0]	For edmp (irq0) interface, indicates gyro data ready masking bit for irq0 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[0]	R/W	INT_ACCEL_DRDY_PIN_0_DIS[0]	For edmp (irq0) interface, Indicates accel data ready masking bit for irq0 line. For UI/AP interface, indicates if FIFO full interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

22.15 STATUS_MASK_PIN_8_15

Name: STATUS_MASK_PIN_8_15
Address: 107 (6Bh)
Reset value: 0x3F
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	INT_ON_DEMAND_PIN_1_DIS[0]	For edmp (irq1) interface, indicates on demand masking bit for irq1 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[4]	R/W	INT_WOM_DRDY_PIN_1_DIS[0]	For edmp (irq1) interface, indicates Wake On Motion event ORing of X, Y, and Z axis masking bit for irq1 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[3:2]	-	-	Reserved
[1]	R/W	INT_GYRO_DRDY_PIN_1_DIS[0]	For edmp (irq1) interface, indicates gyro data ready masking bit for irq1 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[0]	R/W	INT_ACCEL_DRDY_PIN_1_DIS[0]	For edmp (irq1) interface, Indicates accel data ready masking bit for irq1 line. For UI/AP interface, indicates if FIFO full interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

22.16 STATUS_MASK_PIN_16_23

Name: STATUS_MASK_PIN_16_23
Address: 108 (6Ch)
Reset value: 0x3F
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	INT_ON_DEMAND_PIN_2_DIS[0]	For edmp (irq2) interface, indicates on demand masking bit for irq2 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[4]	R/W	INT_WOM_DRDY_PIN_2_DIS[0]	For edmp (irq2) interface, indicates Wake On Motion event ORing of X, Y, and Z axis masking bit for irq2 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[3:2]	-	-	Reserved
[1]	R/W	INT_GYRO_DRDY_PIN_2_DIS[0]	For edmp (irq2) interface, indicates gyro data ready masking bit for irq2 line 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[0]	R/W	INT_ACCEL_DRDY_PIN_2_DIS[0]	For edmp (irq2) interface, Indicates accel data ready masking bit for irq2 line. For UI/AP interface, indicates if FIFO full interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

22.17 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR
Address: 119 (77h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	WOM_X_TH[7:0]	WoM thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg).

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22.18 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR
Address: 120 (78h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	WOM_Y_TH[7:0]	WoM thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg).

22.19 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR
Address: 121 (79h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	WOM_Z_TH[7:0]	WoM thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg).

22.20 IOC_PADS_CONFIG0

Name: IOC_PADS_CONFIG0
Address: 125 (7Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	FSYNC_POLARITY[0]	FSYNC pin polarity 0: Active low 1: Active high
[4:0]	-	-	Reserved

22.21 IREG_OTP_CFG

Name: IREG_OTP_CFG
Address: 130 (82h)
Reset value: 0x03
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1:0]	R/W	OTP_COPY_MODE[1:0]	OTP Copy mode 0: No OTP Copy 1: OTP Copy bank0 and bank1/2 2: Reserved 3: Copy self-test

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22.22 SELFTEST

Name: SELFTEST
Address: 137 (89h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	EN_GZ_ST[0]	[Supports Dynamic Change] GZ self-test enable 0: GZ self-test is disabled 1: GZ self-test is enabled
[4]	R/W	EN_GY_ST[0]	[Supports Dynamic Change] GY self-test enable 0: GY self-test is disabled 1: GY self-test is enabled
[3]	R/W	EN_GX_ST[0]	[Supports Dynamic Change] GX self-test enable 0: GX self-test is disabled 1: GX self-test is enabled
[2]	R/W	EN_AZ_ST[0]	[Supports Dynamic Change] AZ self-test enable 0: AZ self-test is disabled 1: AZ self-test is enabled
[1]	R/W	EN_AY_ST[0]	[Supports Dynamic Change] AY self-test enable 0: AY self-test is disabled 1: AY self-test is enabled
[0]	R/W	EN_AX_ST[0]	[Supports Dynamic Change] AX self-test enable 0: AX self-test is disabled 1: AX self-test is enabled

22.23 IPREG_MISC

Name: IPREG_MISC
Address: 144 (90h)
Reset value: 0x02
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R	EDMP_IDLE[0]	0: Indicates eDMP is busy 1: Indicates eDMP is idle
[0]	-	-	Reserved

22.24 SW_RCOSC1_TRIM

Name: SW_RCOSC1_TRIM
Address: 161 (A1h)
Reset value: Varies by device
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	SW_RCOSC1_TRIM[7:0]	Stores variation of RCOSC frequency test measurement vs. target value, used for SW applications. Value to trim = (RCOSC_measurement – 6400Hz) / 6400Hz * 2540. 6400Hz is the target divided-down RCOSC freq. 2540 is the resolution coefficient: max register range / max oscillator frequency error = (2^7 - 1) / 5%, with a sign bit.

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22.25 SW_PLL1_TRIM

Name: SW_PLL1_TRIM
Address: 162 (A2h)
Reset value: Varies by device
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	SW_PLL1_TRIM[7:0]	Stores variation of PLL frequency test measurement vs. target value, used for SW applications. Value to trim = (PLL_measurement – 6144000Hz) / 6144000Hz * 2540. 6144000Hz is the target PLL freq. 2540 is the resolution coefficient: max register range / max oscillator frequency error = (2^7 - 1) / 5%, with a sign bit.

22.26 FIFO_SRAM_SLEEP

Name: FIFO_SRAM_SLEEP
Address: 167 (A7h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:1]	-	-	Reserved
[0]	R/W	FIFO_GSLEEP_SHARED_SRAM[1:0]	Set selected SRAM bank global sleep mode (pwr_gsleep) 0: Selected SRAM bank sleep mode is controlled by PSEQ, ps_fifo_gsleep_fifo_sram, if this bank contains FIFO data. Otherwise SRAM is in sleep mode (SRAM bank pwr_gsleep = 1). 1: Selected SRAM bank remains in active mode (pwr_gsleep = 0). Can be changed when FIFO is disabled (Bypass mode), AHB interface idle.

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23.1 ACCEL_DATA_X_0

Name: ACCEL_DATA_X_0
Address: 00 (00h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_X_AP[15:8]	Accel X axis data for UI/AP path.

23.2 ACCEL_DATA_X_1

Name: ACCEL_DATA_X_1
Address: 01 (01h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_X_AP[7:0]	Accel X axis data for UI/AP path.

23.3 ACCEL_DATA_Y_0

Name: ACCEL_DATA_Y_0
Address: 02 (02h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Y_AP[15:8]	Accel Y axis data for UI/AP path.

23.4 ACCEL_DATA_Y_1

Name: ACCEL_DATA_Y_1
Address: 03 (03h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Y_AP[7:0]	Accel Y axis data for UI/AP path.

23.5 ACCEL_DATA_Z_0

Name: ACCEL_DATA_Z_0
Address: 04 (04h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Z_AP[15:8]	Accel Z axis data for UI/AP path.

23.6 ACCEL_DATA_Z_1

Name: ACCEL_DATA_Z_1
Address: 05 (05h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Z_AP[7:0]	Accel Z axis data for UI/AP path.

23.7 GYRO_DATA_X_0

Name: GYRO_DATA_X_0
Address: 06 (06h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_X_AP[15:8]	Gyro X axis data for UI/AP path.

23.8 GYRO_DATA_X_1

Name: GYRO_DATA_X_1
Address: 07 (07h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_X_AP[7:0]	Gyro X axis data for UI/AP path.

23.9 GYRO_DATA_Y_0

Name: GYRO_DATA_Y_0
Address: 08 (08h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Y_AP[15:8]	Gyro Y axis data for UI/AP path.

23.10 GYRO_DATA_Y_1

Name: GYRO_DATA_Y_1
Address: 09 (09h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Y_AP[7:0]	Gyro Y axis data for UI/AP path.

23.11 GYRO_DATA_Z_0

Name: GYRO_DATA_Z_0
Address: 10 (0Ah)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Z_AP[15:8]	Gyro Z axis data for UI/AP path.

23.12 GYRO_DATA_Z_1

Name: GYRO_DATA_Z_1
Address: 11 (0Bh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Z_AP[7:0]	Gyro Z axis data for UI/AP path.

23.13 TEMP_DATA_0

Name: TEMP_DATA_0
Address: 12 (0Ch)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TEMP_DATA_AP[15:8]	Temperature data for UI/AP path.

23.14 TEMP_DATA_1

Name: TEMP_DATA_1
Address: 13 (0Dh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TEMP_DATA_AP[7:0]	Temperature data for UI/AP path.

23.15 TMST_FSYNC_DATA_0

Name: TMST_FSYNC_DATA_0
Address: 14 (0Eh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TMST_FSYNC_DATA_AP[15:8]	Timestamp/FSYNC data for UI/AP path.

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23.16 TMST_FSYNC_DATA_1

Name: TMST_FSYNC_DATA_1
Address: 15 (0Fh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TMST_FSYNC_DATA_AP[7:0]	Timestamp/FSYNC data for UI/AP path.

23.17 EXT_DATA_X

Name: EXT_DATA_X
Address: 16 (10h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R	EXT_ACCEL_DATA_X_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Accel X axis for UI/AP path
[3:0]	R	EXT_GYRO_DATA_X_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Gyro X axis for UI/AP path

23.18 EXT_DATA_Y

Name: EXT_DATA_Y
Address: 17 (11h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R	EXT_ACCEL_DATA_Y_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Accel Y axis for UI/AP path
[3:0]	R	EXT_GYRO_DATA_Y_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Gyro Y axis for UI/AP path

23.19 EXT_DATA_Z

Name: EXT_DATA_Z
Address: 18 (12h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R	EXT_ACCEL_DATA_Z_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Accel Z axis for UI/AP path
[3:0]	R	EXT_GYRO_DATA_Z_AP[3:0]	When sensor data resolution is configured to 20 bits, this register provides the 4 least significant bits for Gyro Z axis for UI/AP path

23.20 PWR_MGMT0

Name: PWR_MGMT0
Address: 20 (14h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	ACCEL_LP_CLK_SEL[0]	[Supports Dynamic Change] This bit is applicable to the AP side's operation. This bit is effective when AP is in accel-only operation with AP/accel mode = LP. (a) accel_lp_clk_sel = 1, the AP sensor operation is in ALP mode. (b) accel_lp_clk_sel = 0, the AP sensor operation is in AULP mode. When the I3C Synchronous timing control function is enabled on the AP side, the accel_lp_clk_sel must be at a value of 1. When the I3C Synchronous timing control function is enabled, the chip supports AULP mode operation, but the power consumption is at the ALP level.
[4]	-	-	Reserved
[3:2]	R/W	GYRO_MODE[1:0]	[Supports Dynamic Change] Gyroscope Power-Mode: 00: OFF 01: Standby 10: LP 11: LN
[1:0]	R/W	ACCEL_MODE[1:0]	[Supports Dynamic Change] Accelerometer Power-Mode: 00: OFF 01: OFF 10: LP 11: LN

23.21 FIFO_COUNT_0

Name: FIFO_COUNT_0
Address: 22 (16h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	FIFO_DATA_CNT[15:8]	[Supports Dynamic Change] FIFO data counter. It returns the number of unread frames inside the FIFO. Can be read anytime. For the case of a 16 bit FIFO data count, this register must be read in one 2-byte burst, or one hybrid count+data burst. Internally, FIFO locks the count when the data count register is read, so that MSB and LSB bytes are from the same snapshot. The lock is to prevent the count from changing if a new frame was written to FIFO during count read. For SPI serial interface mode: if SPI clock frequency is more than 10 MHz, a minimum tBUF (CS_n=1) of 500ns is needed, in order to correctly read FIFO frame count immediately after reading complete data frames.

23.22 FIFO_COUNT_1

Name: FIFO_COUNT_1
Address: 23 (17h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	FIFO_DATA_CNT[7:0]	[Supports Dynamic Change] FIFO data counter. It returns the number of unread frames inside the FIFO. Can be read anytime. For the case of a 16 bit FIFO data count, this register must be read in one 2-byte burst, or one hybrid count+data burst. Internally, FIFO locks the count when the data count register is read, so that MSB and LSB bytes are from the same snapshot. The lock is to prevent the count from changing if a new frame was written to FIFO during count read. For SPI serial interface mode: if SPI clock frequency is more than 10 MHz, a minimum tBUF (CS_n=1) of 500ns is needed, in order to correctly read FIFO frame count immediately after reading complete data frames.

23.23 FIFO_DATA

Name: FIFO_DATA
Address: 24 (18h)
Reset value: 0x7F
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	FIFO_RDATA[7:0]	FIFO data read by serial interface

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23.24 INT1_CONFIG0

Name: INT1_CONFIG0
Address: 26 (1Ah)
Reset value: 0x80
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	INT1_STATUS_EN_RESET_DONE[0]	For UI/AP interface, source enable register for Reset process is finished (after OTP copy is complete, i.e. after OTP_DONE signal) interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[6]	R/W	INT1_STATUS_EN_AUX1_AGC_RDY[0]	For UI/AP interface, source enable register for Optical Image Stabilization Interface #1 AGC Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[5]	R/W	INT1_STATUS_EN_AP_AGC_RDY[0]	For UI/AP interface, source enable register for User Interface AGC Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[4]	R/W	INT1_STATUS_EN_AP_FSYNC[0]	For UI/AP interface, source enable register for User Interface FSYNC interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no any interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[3]	R/W	INT1_STATUS_EN_AUX1_DRDY[0]	For UI/AP interface, source enable register for Optical Image Stabilization Interface 1 Sensor Register Data Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

Name: INT1_CONFIG0
Address: 26 (1Ah)
Reset value: 0x80
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[2]	R/W	INT1_STATUS_EN_DRDY[0]	For UI/AP interface, source enable register for User Interface Sensor Register Data Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[1]	R/W	INT1_STATUS_EN_FIFO_THS[0]	For UI/AP interface, source enable register for FIFO count ≥ FIFO threshold interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[0]	R/W	INT1_STATUS_EN_FIFO_FULL[0]	For UI/AP interface, source enable register for FIFO full interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

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23.25 INT1_CONFIG1

Name: INT1_CONFIG1
Address: 27 (1Bh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	INT1_STATUS_EN_APEX_EVENT[0]	For UI/AP interface, source enable register for edmp event interrupt. 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[5]	-	-	Reserved
[4]	R/W	INT1_STATUS_EN_I3C_PROTOCOL_ERR[0]	For UI/AP interface, source enable register for I3C protocol error detected by I3C Slave interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[3]	R/W	INT1_STATUS_EN_WOM_Z[0]	For UI/AP interface, source enable register for Wake On Motion event on Z axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[2]	R/W	INT1_STATUS_EN_WOM_Y[0]	For UI/AP interface, source enable register for Wake On Motion event on Y axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[1]	R/W	INT1_STATUS_EN_WOM_X[0]	For UI/AP interface, source enable register for Wake On Motion event on X axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

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Name: INT1_CONFIG1
Address: 27 (1Bh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[0]	R/W	INT1_STATUS_EN_PLL_RDY[0]	For UI/AP interface, source enable register for PLL is locked interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

23.26 INT1_CONFIG2

Name: INT1_CONFIG2
Address: 28 (1Ch)
Reset value: 0x04
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2]	R/W	INT1_DRIVE[0]	Sets INT1 PAD in to Open-drain or Push-pull 0: Push-pull 1: Open-drain
[1]	R/W	INT1_MODE[0]	UI/AP interface: Interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled
[0]	R/W	INT1_POLARITY[0]	UI/AP interface: Interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled

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23.27 INT1_STATUS0

Name: INT1_STATUS0
Address: 29 (1Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/C	INT1_STATUS_RESET_DONE[0]	For UI/AP interface, indicates if status register (ISR) for Reset process is finished (after OTP copy is complete, i.e. after OTP_DONE signal) interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[6]	R/C	INT1_STATUS_AUX1_AGC_RDY[0]	For UI/AP interface, indicates if status register (ISR) for Optical Image Stabilization Interface #1 AGC Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[5]	R/C	INT1_STATUS_AP_AGC_RDY[0]	For UI/AP interface, indicates if status register (ISR) for User Interface AGC Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[4]	R/C	INT1_STATUS_AP_FSYNC[0]	For UI/AP interface, indicates if status register (ISR) for User Interface FSYNC interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[3]	R/C	INT1_STATUS_AUX1_DRDY[0]	For UI/AP interface, indicates if status register (ISR) for Optical Image Stabilization Interface 1 Sensor Register Data Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

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Name: INT1_STATUS0
Address: 29 (1Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[2]	R/C	INT1_STATUS_DRDY[0]	For UI/AP interface, indicates if status register (ISR) for User Interface Sensor Register Data Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[1]	R/C	INT1_STATUS_FIFO_THS[0]	For UI/AP interface, indicates if status register (ISR) for FIFO count ≥ FIFO threshold interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[0]	R/C	INT1_STATUS_FIFO_FULL[0]	For UI/AP interface, indicates if status register (ISR) for FIFO full interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

23.28 INT1_STATUS1

Name: INT1_STATUS1
Address: 30 (1Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/C	INT1_STATUS_APEX_EVENT[0]	For UI/AP interface, indicates if status register (ISR) for edmp event interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[5]	-	-	Reserved
[4]	R/C	INT1_STATUS_I3C_PROTOCOL_ERR[0]	For UI/AP interface, indicates if status register (ISR) for I3C protocol error detected by I3C Slave interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[3]	R/C	INT1_STATUS_WOM_Z[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on Z axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[2]	R/C	INT1_STATUS_WOM_Y[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on Y axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[1]	R/C	INT1_STATUS_WOM_X[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on X axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

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Name: INT1_STATUS1
Address: 30 (1Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[0]	R/C	INT1_STATUS_PLL_RDY[0]	For UI/AP interface, indicates if status register (ISR) for PLL is locked interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

23.29 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 31 (1Fh)
Reset value: 0x06
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6:4]	R/W	AP_ACCEL_FS_SEL[2:0]	[Supports Dynamic Change] Set the UI/AP signal path accel full scale 0: 32g 1: 16g 2: 8g 3: 4g 4: 2g
[3:0]	R/W	ACCEL_ODR[3:0]	[Supports Dynamic Change] Accelerometer Output Data Rate 0: 6.4kHz (LN only) 1: 6.4kHz (LN only) 2: 6.4kHz (LN only) 3: 6.4kHz (LN only) 4: 3.2kHz (LN only) 5: 1.6kHz (LN only) 6: 800Hz (default, LN only) 7: 400Hz 8: 200Hz 9: 100Hz 10: 50Hz 11: 25Hz 12: 12.5Hz 13: 6.25Hz (LP only) 14: 3.125Hz (LP only) 15: 1.5625Hz (LP only) This field can be changed on-the-fly even if accel sensor is already on

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23.30 GYRO_CONFIG0

Name: GYRO_CONFIG0
Address: 32 (20h)
Reset value: 0x06
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	AP_GYRO_FS_SEL[3:0]	[Supports Dynamic Change] Set the UI/AP signal path gyro full scale 0: 4000 dps 1: 2000 dps 2: 1000 dps 3: 500 dps 4: 250 dps 5: 125 dps 6: 62.5 dps 7: 31.25 dps 8: 15.625 dps
[3:0]	R/W	GYRO_ODR[3:0]	[Supports Dynamic Change] Gyroscope Output Data Rate 0: 6.4kHz (LN only) 1: 6.4kHz (LN only) 2: 6.4kHz (LN only) 3: 6.4kHz (LN only) 4: 3.2kHz (LN only) 5: 1.6kHz (LN only) 6: 800Hz (default, LN only) 7: 400Hz 8: 200Hz 9: 100Hz 10: 50Hz 11: 25Hz 12: 12.5Hz 13: 6.25Hz (LP only) 14: 3.125Hz (LP only) 15: 1.5625Hz (LP only) This field can be changed on-the-fly even if gyro sensor is already on

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23.31 FIFO_CONFIG0

Name: FIFO_CONFIG0
Address: 33 (21h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	R/W	FIFO_MODE[1:0]	[Supports Dynamic Change] Set the FIFO operation mode. 2'b00: Bypass (disabled) 2'b01: Stream mode - Frames are overwritten when the FIFO full condition is reached. Supported only for 8, 16, 20 bytes frame size. 2'b10: Stop-on-full mode - Frames are not stored in FIFO once the FIFO full condition is reached 2'b11: Reserved
[5:0]	R/W	FIFO_DEPTH[5:0]	Set the FIFO depth in bytes. 000111: Sets FIFO depth to 2K bytes (recommended setting) 001111: Sets FIFO depth to 4K bytes (valid when all APEX features are disabled) Others: Reserved Can be changed when FIFO is disabled (Bypass mode).

23.32 FIFO_CONFIG1_0

Name: FIFO_CONFIG1_0
Address: 34 (22h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FIFO_WM_TH[7:0]	[Supports Dynamic Change] FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. MSByte write pulse is used to check watermark level and generate WM interrupt event. Can be changed on-the-fly.

23.33 FIFO_CONFIG1_1

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Name: FIFO_CONFIG1_1
Address: 35 (23h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	FIFO_WM_TH[15:8]	[Supports Dynamic Change] FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. MSByte write pulse is used to check watermark level and generate WM interrupt event. Can be changed on-the-fly.

23.34 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 36 (24h)
Reset value: 0x20
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	W/C	FIFO_FLUSH[0]	[Supports Dynamic Change] FIFO flush command. When set high the FIFO is flushed, meaning the pointers and control logic is reset. Configuration registers are not reset. The register is auto-cleared by hardware. Can be changed on-the-fly.
[6:5]	-	-	Reserved
[4]	R/W	FIFO_INT_OVFL[0]	Select whether the FIFO full and FIFO watermark interrupts are generated continuously when FIFO is in overflow 0: Interrupts stop when FIFO is overflowed 1: Interrupts are continuously generated when FIFO is overflowed Can be changed when FIFO is disabled (Bypass mode).
[3]	R/W	FIFO_WR_WM_GT_TH[0]	Set write watermark interrupt generating condition. 0: Write watermark interrupt generated when counter is equal to threshold 1: Write watermark interrupt generated when counter is greater than or equal to threshold Can be changed when FIFO is disabled (Bypass mode).
[2:0]	-	-	Reserved

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23.35 FIFO_CONFIG3

Name: FIFO_CONFIG3
Address: 37 (25h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	FIFO_HIRES_EN[0]	Enable high resolution accel and gyro data insertion into FIFO frame
[2]	R/W	FIFO_GYRO_EN[0]	Enable gyro data insertion into FIFO frame
[1]	R/W	FIFO_ACCEL_EN[0]	Enable accel data insertion into FIFO frame
[0]	R/W	FIFO_IF_EN[0]	[Supports Dynamic Change] Enable the SREG-FIFO interface. The SREG-FIFO interface should be enabled when the FIFO is also enabled (i.e., not in bypass mode), so a standard enable sequence is: 1) Enable FIFO. 2) Enable SREG-FIFO interface. The opposite for the disable sequence. To prevent power drain, sreg_fifo_if_en should be set to 0 if FIFO is in bypass mode.

23.36 FIFO_CONFIG4

Name: FIFO_CONFIG4
Address: 38 (26h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:5]	-	-	Reserved
[4:2]	R/W	FIFO_COMP_NC_FLOW_CFG[2:0]	Configures the compression algorithm to write non-compressed frames at a certain rate 0: Non-compressed frame flow is disabled 1: Non-compressed frame every 8 frames 2: Non-compressed frame every 16 frames 3: Non-compressed frame every 32 frames 4: Non-compressed frame every 64 frames 5: Non-compressed frame every 128 frames
[1]	R/W	FIFO_COMP_EN[0]	Enable the FIFO compression algorithm
[0]	R/W	FIFO_TMST_FSYNC_EN[0]	Enable the insertion of the Timestamp or FSYNC data into FIFO frame 0: No Timestamp/FSYNC data inserted into FIFO frame (timestamp fields are 0x0000). fsync_tag_en bit in FIFO header is 0 1: Timestamp/FSYNC data inserted into FIFO frame. fsync_tag_en bit in FIFO header is set on a FSYNC trigger event

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23.37 TMST_WOM_CONFIG

Name: TMST_WOM_CONFIG
Address: 39 (27h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	TMST_DELTA_EN[0]	Time Stamp delta Enable: When set to 1, the Time stamp field contains the measurement of time since the last occurrence of trigger event
[5]	R/W	TMST_RESOL[0]	Time Stamp resolution When set to 0 (default), time stamp resolution is 1µs. When set to 1, resolution is 16µs
[4]	R/W	WOM_EN[0]	0: Wake-On-Motion feature is disabled 1: Wake-On-Motion feature is enabled When wom_mode=0, the sample which comes after this bit has been set to 1 becomes the initial sample for the compare operation
[3]	R/W	WOM_MODE[0]	0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample
[2]	R/W	WOM_INT_MODE[0]	0: The three interrupt sources WOM_X, WOM_Y, WOM_Z are triggered by the respective WOM axes (i.e., WOM_X is triggered by the X axis motion logic, WOM_Y is triggered by the Y axis motion logic, WOM_Z is triggered by the Z axis motion logic). 1: The three interrupt sources WOM_X, WOM_Y, WOM_Z are triggered by the AND of the three motion axes, collapsing the three interrupts in a single interrupt. Any of WOM_X, WOM_Y, WOM_Z can be used for the purpose. In this mode, one gets a motion interrupt only when a motion is detected simultaneously on all three axes.
[1:0]	R/W	WOM_INT_DUR[1:0]	Configure the interrupt deglitch logic to trigger the WoM interrupt only after a certain number of events. 0: WoM interrupt is asserted at first detected event 1: WoM interrupt is asserted at second detected event 2: WoM interrupt is asserted at third detected event 3: WoM interrupt is asserted at fourth detected event

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23.38 FSYNC_CONFIG0

Name: FSYNC_CONFIG0
Address: 40 (28h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	AP_FSYNC_FLAG_CLEAR_SEL[0]	Select the FSYNC flag clear policy 0: FSYNC flag is cleared when UI/AP sensor reg is updated 1 : FSYNC flag is cleared when UI/AP serial interface reads the sensor register LSB of FSYNC tagged axis
[2:0]	R/W	AP_FSYNC_SEL[2:0]	Select the sensor that will carry the FSYNC tagging 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA LSB 2: Tag FSYNC flag to GYRO_DATA_X LSB 3: Tag FSYNC flag to GYRO_DATA_Y LSB 4: Tag FSYNC flag to GYRO_DATA_Z LSB 5: Tag FSYNC flag to ACCEL_DATA_X LSB 6: Tag FSYNC flag to ACCEL_DATA_Y LSB 7: Tag FSYNC flag to ACCEL_DATA_Z LSB

23.39 FSYNC_CONFIG1

Name: FSYNC_CONFIG1
Address: 41 (29h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	AUX1_FSYNC_FLAG_CLEAR_SEL[0]	Select the FSYNC flag clear policy 0: FSYNC flag is cleared when OIS1 sensor reg is updated 1: FSYNC flag is cleared when AUX1 serial interface reads the sensor register LSB of FSYNC tagged axis
[2:0]	R/W	AUX1_FSYNC_SEL[2:0]	Select the sensor that will carry the FSYNC tagging 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA_AUX1 LSB 2: Tag FSYNC flag to GYRO_DATA_X_AUX1 LSB 3: Tag FSYNC flag to GYRO_DATA_Y_AUX1 LSB 4: Tag FSYNC flag to GYRO_DATA_Z_AUX1 LSB 5: Tag FSYNC flag to ACCEL_DATA_X_AUX1 LSB 6: Tag FSYNC flag to ACCEL_DATA_Y_AUX1 LSB 7: Tag FSYNC flag to ACCEL_DATA_Z_AUX1 LSB

23.40 RTC_CONFIG

Name: RTC_CONFIG
Address: 42 (2Ah)
Reset value: 0x03
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	RTC_ALIGN[0]	RTC align bit – re-align command is generated by writing this bit.
[5]	R/W	RTC_MODE[0]	If set to 1 enables the RTC functionality: the external clock source CLK_IN is used to keep the time-base and generate precise ODR values. If also the I3C Synchronous Mode functionality is enabled, then setting this bit to 1 will have no effect. RTC functionality can be enabled only if accel_lp_clk_sel is set to 1; otherwise device may not behave as expected.
[4:0]	-	-	Reserved

23.41 DMP_EXT_SEN_ODR_CFG

Name: DMP_EXT_SEN_ODR_CFG
Address: 43 (2Bh)
Reset value: 0x01
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2:0]	R/W	APEX_ODR[2:0]	[Supports Dynamic Change] DMP Output Data Rate. The dmp_odr needs to be smaller than or equal to both the accel_odr and gyro_odr. Also, all rates but 800Hz can be set if Accel UI/AP is in LP; in order to set the DMP ODR to 800Hz, the Accel UI/AP PM must be set in LN, otherwise the new rate will not be applied). 3'b000: 25Hz 3'b001: 50Hz (default) 3'b010: 100Hz 3'b011: 200Hz 3'b100: 400Hz 3'b101: 800Hz (LN-only) 3'b110: Reserved 3'b111: Reserved

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23.42 ODR_DECIMATE_CONFIG

Name: ODR_DECIMATE_CONFIG
Address: 44 (2Ch)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	R/W	GYRO_FIFO_ODR_DEC[3:0]	Decimation factor for the sreg_update rate at the Gyroscope FIFO. Decimation value is 2^(gyro_fifo_down) 4'b0000: 1 (as input ODR rate) 4'b0001: 2 4'b0010: 4 4'b0011: 8 4'b0100: 16 4'b0101: 32 4'b0110: 64 4'b0111: 128 4'b1000: 256 4'b1001: 512 4'b1010: 1024 4'b1011: 2048 4'b1100: 4096 4'b1101: Reserved 4'b1110: Reserved 4'b1111: Reserved The final sreg_update value will be gyro_odr/2^(gyro_fifo_odr_dec), with a minimum decimated rate equal to the minimum ODR value.
[3:0]	R/W	ACCEL_FIFO_ODR_DEC[3:0]	Decimation factor for the sreg_update rate at the Accel FIFO. Decimation value is 2^(accel_fifo_down): 4'b0000: 1 (as input ODR rate) 4'b0001: 2 4'b0010: 4 4'b0011: 8 4'b0100: 16 4'b0101: 32 4'b0110: 64 4'b0111: 128 4'b1000: 256 4'b1001: 512 4'b1010: 1024 4'b1011: 2048 4'b1100: 4096 4'b1101: Reserved 4'b1110: Reserved 4'b1111: Reserved The final sreg_update value will be accel_odr/2^(accel_fifo_odr_dec), with a minimum decimated rate equal to the minimum ODR value.

23.43 EDMP_APEX_EN0

Name: EDMP_APEX_EN0
Address: 45 (2Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	SMD_EN[0]	Set 1 to enable SMD algorithm
[6]	R/W	R2W_EN[0]	Set 1 to enable Raise to Wake algorithm
[5]	R/W	FF_EN[0]	Set 1 to enable Freefall algorithm
[4]	R/W	PEDO_EN[0]	Set 1 to enable Pedometer algorithm
[3]	R/W	TILT_EN[0]	Set 1 to enable Tilt algorithm
[2]	R/W	SHAKE_EN[0]	Set 1 to enable Shake algorithm
[1]	R/W	NOMOTION_EN[0]	Set 1 to enable No-Motion algorithm
[0]	R/W	TAP_EN[0]	Set 1 to enable Tap algorithm

23.44 EDMP_APEX_EN1

Name: EDMP_APEX_EN1
Address: 46 (2Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	EDMP_ENABLE[0]	0: Mask out all eDMP input interrupts and freeze eDMP processing after eDMP is finished with current processing sample of all ISRs. 1: Enable eDMP operation mode
[5]	R/W	B2S_EN[0]	Set 1 to enable Bring-to-See (B2S) algorithm
[4:3]	-	-	Reserved
[2]	R/W	POWER_SAVE_EN[0]	Set 1 to enable power save mode
[1]	RWS	INIT_EN[0]	This bit is set by the host to indicate: eDMP executes only the segment of code that initialize constants used by algorithms. The register is R/W by the external host through the direct register accessing path. The register is R/C by any AHB master when it is accessed via internal AHB/APB bus.
[0]	R/W	FLAT_EN[0]	Set 1 to enable Flat algorithm

23.45 APEX_BUFFER_MGMT

Name: APEX_BUFFER_MGMT
Address: 47 (2Fh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	R/W	FF_DURATION_HOST_RPTR[1:0]	LSB indicates SRAM address for host to read MSB indicates size 2 buffer wrap around 00: Host reads buffer 0 01: Host reads buffer 1 10: Host reads buffer 0 11: Host reads buffer 1
[5:4]	R	FF_DURATION_EDMP_WPTR[1:0]	LSB indicates SRAM address for eDMP to write MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1
[3:2]	R/W	STEP_COUNT_HOST_RPTR[1:0]	LSB indicates SRAM address for host to read MSB indicates size 2 buffer wrap around 00: Host reads buffer 0 01: Host reads buffer 1 10: Host reads buffer 0 11: Host reads buffer 1
[1:0]	R	STEP_COUNT_EDMP_WPTR[1:0]	LSB indicates SRAM address for eDMP to write MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1

23.46 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 48 (30h)
Reset value: 0x0A
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	R/W	VIRTUAL_ACCESS_AUX1_EN	Enable AUX1 virtual access by host interface 0: AUX1 virtual access by host interface not enabled 1: AUX1 virtual access by host enabled; AUX1 registers are accessible by host interface but not accessible by AUX1 interface
[4:2]	-	-	Reserved
[1]	R	AP_SPI_34_MODE[0]	Read only register field, shows OTP trim for UI interface SPI in 3-wire or 4-wire mode 0: 3-wire mode 1: 4-wire mode
[0]	R	AP_SPI_MODE[0]	Read only register field, shows OTP trim for UI interface SPI mode selection 0: SPI mode 0 or 3 1: SPI mode 1 or 2s

23.47 INTF_CONFIG1_OVRD

Name: INTF_CONFIG1_OVRD
Address: 49 (31h)
Reset value: 0x0C
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	AP_SPI_34_MODE_OVRD[0]	0: Override disable for AP interface SPI 4-wire/3-wire modes 1: Override enable for AP interface SPI 4-wire/3-wire modes
[2]	R/W	AP_SPI_34_MODE_OVRD_VAL[0]	Override value for AP interface SPI 4-wire/3-wire modes 0: SPI 3-wire mode 1: SPI 4-wire mode
[1]	R/W	AP_SPI_MODE_OVRD[0]	0: Override disable for AP interface SPI_MODE value 1: Override enable for AP interface SPI_MODE value
[0]	R/W	AP_SPI_MODE_OVRD_VAL[0]	Override value for AP interface SPI Mode 0: SPI mode 0 or 3 1: SPI mode 1 or 2

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23.48 INTF_AUX_CONFIG

Name: INTF_AUX_CONFIG
Address: 50 (32h)
Reset value: 0x02
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R/W	AUX1_SPI_34_MODE[0]	0: SPI 3 mode, use SDA pad to send data out for OIS1 1: SPI 4 mode, use SDO pad to send data out for OIS1
[0]	R/W	AUX1_SPI_MODE[0]	SPI Mode based on CPOL and CPHA for AUX1 0: spi_mode0 or spi_mode3 1: spi_mode1 or spi_mode2

23.49 IOC_PAD_SCENARIO_OVRD

Name: IOC_PAD_SCENARIO_OVRD
Address: 53 (35h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2]	R/W	PADS_INT2_CFG_OVRD[0]	Override enable for ioc_pads_int2_cfg
[1:0]	R/W	PADS_INT2_CFG_OVRD_VAL[1:0]	Selects how INT2 pads are used 0: INT2 is selected 1: FSYNC is selected 2: CLKIN is selected 3: RESERVED

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23.50 DRIVE_CONFIG0

Name: DRIVE_CONFIG0
Address: 54 (36h)
Reset value: 0x36
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5:3]	R/W	PADS_I2C_SLEW[2:0]	Slew rate control for any pin in the I2C mode of operation, including pins on the AP serial interface when device is a client device of an I2C bus,. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 3 ns; TYP: 20 ns; MAX: 136 ns 010: MIN: 2 ns; TYP: 7 ns; MAX: 84 ns Others: Reserved
[2:0]	R/W	PADS_SPI_SLEW[2:0]	Slew rate control for any pin in the SPI mode of operation. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns

23.51 DRIVE_CONFIG2

Name: DRIVE_CONFIG2
Address: 56 (38h)
Reset value: 0x02
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2:0]	R/W	PADS_SLEW[2:0]	Slew rate control for INT1 pin at all times. Slew rate control for all pins before OTP copy operation is completed. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns

23.52 INT_APEX_CONFIG0

Name: INT_APEX_CONFIG0
Address: 61 (3Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	INT_STATUS_MASK_PIN_R2W_WAKE_DET[0]	For edmp_out interface, indicates if raise to wake detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[6]	R/W	INT_STATUS_MASK_PIN_FF_DET[0]	For edmp_out interface, Indicates if freefall interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[5]	R/W	INT_STATUS_MASK_PIN_STEP_DET[0]	For edmp_out interface, indicates if step detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[4]	R/W	INT_STATUS_MASK_PIN_STEP_CNT_OVFL[0]	For edmp_out interface, indicates if step count overflow interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[3]	R/W	INT_STATUS_MASK_PIN_TILT_DET[0]	For edmp_out interface, indicates if tilt detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[2]	R/W	INT_STATUS_MASK_PIN_LOW_G_DET[0]	For edmp_out interface, indicates if lowG detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[1]	R/W	INT_STATUS_MASK_PIN_HIGH_G_DET[0]	For edmp_out interface, indicates if highG detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

Name: INT_APEX_CONFIG0
Address: 61 (3Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[0]	R/W	INT_STATUS_MASK_PIN_TAP_DETECT[0]	For edmp_out interface, indicates if Tap detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

23.53 INT_APEX_CONFIG1

Name: INT_APEX_CONFIG1
Address: 62 (3Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	INT_STATUS_MASK_PIN_REVB2S_DET[0]	For edmp_out interface, indicates if reverse-bring-to-see (REVB2S) detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[6]	R/W	INT_STATUS_MASK_PIN_B2S_DET[0]	For edmp_out interface, indicates if bring-to-see (B2S) detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[5]	R/W	INT_STATUS_MASK_PIN_SHAKE_DET[0]	For edmp_out interface, indicates if shake detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[4]	R/W	INT_STATUS_MASK_PIN_SA_DONE[0]	For edmp_out interface, secure authentication done interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[3]	-	-	Reserved

Name: INT_APEX_CONFIG1
Address: 62 (3Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[2]	R/W	INT_STATUS_MASK_PIN_SELFTEST_DONE[0]	For edmp_out interface, indicates if self-test done interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[1]	R/W	INT_STATUS_MASK_PIN_SMD_DET[0]	For edmp_out interface, indicates if significant motion detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[0]	R/W	INT_STATUS_MASK_PIN_R2W_SLEEP_DET[0]	For edmp_out interface, indicates if raise to wake sleep detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

23.54 INT_APEX_CONFIG2

Name: INT_APEX_CONFIG2
Address: 63 (3Fh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	INT_STATUS_MASK_PIN_FLAT_DET[0]	For edmp_out interface, indicates if motion detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[2]	R/W	INT_STATUS_MASK_PIN_NOFLAT_DET[0]	For edmp_out interface, indicates if motion detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[1]	R/W	INT_STATUS_MASK_PIN_MOTION_DET[0]	For edmp_out interface, indicates if motion detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.
[0]	R/W	INT_STATUS_MASK_PIN_NOMOTION_DET[0]	For edmp_out interface, indicates if no-motion detection interrupt is masked 0: The occurrence of interrupt source event will assert the assigned interrupt pin. 1: The occurrence of interrupt source event will not assert the assigned interrupt pin.

23.55 INT_APEX_STATUS0

Name: INT_APEX_STATUS0
Address: 64 (40h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/C	INT_STATUS_R2W_WAKE_DET[0]	For edmp_out interface. Indicates if status register (ISR) for raise to wake wake detection interrupt is set 0: Status not set. 1: Status set.
[6]	R/C	INT_STATUS_FF_DET[0]	For edmp_out Interface. Indicates if status register (ISR) for freefall interrupt is set 0: Status not set. 1: Status set.
[5]	R/C	INT_STATUS_STEP_DET[0]	For edmp_out interface. Indicates if status register (ISR) for step detection interrupt is set 0: Status not set. 1: Status set.
[4]	R/C	INT_STATUS_STEP_CNT_OVFL[0]	For edmp_out interface. Indicates if status register (ISR) for step count overflow interrupt is set 0: Status not set. 1: Status set.
[3]	R/C	INT_STATUS_TILT_DET[0]	For edmp_out interface. Indicates if status register (ISR) for tilt detection interrupt is set 0: Status not set. 1: Status set.
[2]	R/C	INT_STATUS_LOW_G_DET[0]	For edmp_out interface. Indicates if status register (ISR) for lowG detection interrupt is set 0: Status not set. 1: Status set.
[1]	R/C	INT_STATUS_HIGH_G_DET[0]	For edmp_out interface. Indicates if status register (ISR) for highG detection interrupt is set 0: Status not set. 1: Status set.
[0]	R/C	INT_STATUS_TAP_DETECT[0]	For edmp_out interface. Indicates if status register (ISR) for Tap detection interrupt is set 0: Status not set. 1: Status set.

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23.56 INT_APEX_STATUS1

Name: INT_APEX_STATUS1
Address: 65 (41h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/C	INT_STATUS_REVB2S_DET[0]	For edmp_out interface. Indicates if status register (ISR) for reverse-bring-to-see (REVB2S) detection interrupt is set 0: Status not set. 1: Status set.
[6]	R/C	INT_STATUS_B2S_DET[0]	For edmp_out interface. Indicates if status register (ISR) for bring-to-see (B2S) detection interrupt is set 0: Status not set. 1: Status set.
[5]	R/C	INT_STATUS_SHAKE_DET[0]	For edmp_out interface. Indicates if status register (ISR) for shake detection interrupt is set 0: Status not set. 1: Status set.
[4]	R/C	INT_STATUS_SA_DONE[0]	For edmp_out interface. Indicates if status register (ISR) for secure authentication done interrupt is set 0: Status not set. 1: Status set.
[3]	-	-	Reserved
[2]	R/C	INT_STATUS_SELFTEST_DONE[0]	For edmp_out interface. Indicates if status register (ISR) for self-test done interrupt is set 0: Status not set. 1: Status set.
[1]	R/C	INT_STATUS_SMD_DET[0]	For edmp_out interface. Indicates if status register (ISR) for significant motion detection interrupt is set 0: Status not set. 1: Status set.
[0]	R/C	INT_STATUS_R2W_SLEEP_DET[0]	For edmp_out interface. Indicates if status register (ISR) for raise to wake sleep detection interrupt is set 0: Status not set. 1: Status set.

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23.57 INT_APEX_STATUS2

Name: INT_APEX_STATUS2
Address: 66 (42h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/C	INT_STATUS_FLAT_DET[0]	For edmp_out interface. Indicates if status register (ISR) for motion detection interrupt is set 0: Status not set. 1: Status set.
[2]	R/C	INT_STATUS_NOFLAT_DET[0]	For edmp_out interface. Indicates if status register (ISR) for motion detection interrupt is set 0: Status not set. 1: Status set.
[1]	R/C	INT_STATUS_MOTION_DET[0]	For edmp_out interface. Indicates if status register (ISR) for motion detection interrupt is set 0: Status not set. 1: Status set.
[0]	R/C	INT_STATUS_NOMOTION_DET[0]	For edmp_out interface. Indicates if status register (ISR) for no-motion detection interrupt is set 0: Status not set. 1: Status set.

23.58 INTF_CONFIG_OVRD_AUX1

Name: INTF_CONFIG_OVRD_AUX1
Address: 70 (46h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:4]	-	-	Reserved
[3]	R/W	AUX1_SPI_34_MODE_OVRD[0]	Override enable for SPI4/SPI3 modes for OIS1
[2]	R/W	AUX1_SPI_34_MODE_OVRD_VAL[0]	Override value for SPI4/SPI3 modes for OIS1 0: SPI 3 mode, use SDA pad to send data out. 1: SPI 4 mode, use SDO pad to send data out.
[1]	R/W	AUX1_SPI_MODE_OVRD[0]	Override enable for spi_mode register value for aux1
[0]	R/W	AUX1_SPI_MODE_OVRD_VAL[0]	Override value for SPI Mode based on CPOL and CPHA for aux1 0: spi_mode0 or spi_mode3 1: spi_mode1 or spi_mode2 No change is expected from default mode when IxC slave is selected for host serial transfer.

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23.59 ACCEL_DATA_X_AUX1_0

Name: ACCEL_DATA_X_AUX1_0
Address: 72 (48h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_X_AUX1[15:8]	Accel X axis data for AUX1 path.

23.60 ACCEL_DATA_X_AUX1_1

Name: ACCEL_DATA_X_AUX1_1
Address: 73 (49h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_X_AUX1[7:0]	Accel X axis data for AUX1 path.

23.61 ACCEL_DATA_Y_AUX1_0

Name: ACCEL_DATA_Y_AUX1_0
Address: 74 (4Ah)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Y_AUX1[15:8]	Accel Y axis data for AUX1 path.

23.62 ACCEL_DATA_Y_AUX1_1

Name: ACCEL_DATA_Y_AUX1_1
Address: 75 (4Bh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Y_AUX1[7:0]	Accel Y axis data for AUX1 path.

23.63 ACCEL_DATA_Z_AUX1_0

Name: ACCEL_DATA_Z_AUX1_0
Address: 76 (4Ch)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Z_AUX1[15:8]	Accel Z axis data for AUX1 path.

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23.64 ACCEL_DATA_Z_AUX1_1

Name: ACCEL_DATA_Z_AUX1_1
Address: 77 (4Dh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	ACCEL_DATA_Z_AUX1[7:0]	Accel Z axis data for AUX1 path.

23.65 GYRO_DATA_X_AUX1_0

Name: GYRO_DATA_X_AUX1_0
Address: 78 (4Eh)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_X_AUX1[15:8]	Gyro X axis data for AUX1 path.

23.66 GYRO_DATA_X_AUX1_1

Name: GYRO_DATA_X_AUX1_1
Address: 79 (4Fh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_X_AUX1[7:0]	Gyro X axis data for AUX1 path.

23.67 GYRO_DATA_Y_AUX1_0

Name: GYRO_DATA_Y_AUX1_0
Address: 80 (50h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Y_AUX1[15:8]	Gyro Y axis data for AUX1 path.

23.68 GYRO_DATA_Y_AUX1_1

Name: GYRO_DATA_Y_AUX1_1
Address: 81 (51h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Y_AUX1[7:0]	Gyro Y axis data for AUX1 path.

23.69 GYRO_DATA_Z_AUX1_0

Name: GYRO_DATA_Z_AUX1_0
Address: 82 (52h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Z_AUX1[15:8]	Gyro Z axis data for AUX1 path.

23.70 GYRO_DATA_Z_AUX1_1

Name: GYRO_DATA_Z_AUX1_1
Address: 83 (53h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	GYRO_DATA_Z_AUX1[7:0]	Gyro Z axis data for AUX1 path.

23.71 TEMP_DATA_AUX1_0

Name: TEMP_DATA_AUX1_0
Address: 84 (54h)
Reset value: 0x80
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TEMP_DATA_AUX1[15:8]	Temperature data for AUX1 path.

23.72 TEMP_DATA_AUX1_1

Name: TEMP_DATA_AUX1_1
Address: 85 (55h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TEMP_DATA_AUX1[7:0]	Temperature data for AUX1 path.

23.73 TMST_FSYNC_DATA_AUX1_0

Name: TMST_FSYNC_DATA_AUX1_0
Address: 86 (56h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TMST_FSYNC_DATA_AUX1[15:8]	Timestamp/FSYNC data for AUX1 path.

23.74 TMST_FSYNC_DATA_AUX1_1

Name: TMST_FSYNC_DATA_AUX1_1
Address: 87 (57h)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	TMST_FSYNC_DATA_AUX1[7:0]	Timestamp/FSYNC data for AUX1 path.

23.75 PWR_MGMT_AUX1

Name: PWR_MGMT_AUX1
Address: 88 (58h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R/W	GYRO_AUX1_EN[0]	[Supports Dynamic Change] Enable the AUX1 interface for the Gyroscope sensor. 0: OFF 1: ON
[0]	R/W	ACCEL_AUX1_EN[0]	[Supports Dynamic Change] Enable the AUX1 interface for the Accelerometer sensor. 0: OFF 1: ON

23.76 FS_SEL_AUX1

Name: FS_SEL_AUX1
Address: 89 (59h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6:3]	R/W	AUX1_GYRO_FS_SEL[3:0]	[Supports Dynamic Change] Set the AUX1 signal path gyro full scale 0: 4000dps 1: 2000dps 2: 1000dps 3: 500dps 4: 250dps 5: 125dps 6: 62.5dps 7: 31.25dps 8: 15.625dps Others: Reserved
[2:0]	R/W	AUX1_ACCEL_FS_SEL[2:0]	[Supports Dynamic Change] Set the AUX1 signal path accel full scale 0: 32g 1: 16g 2: 8g 3: 4g 4: 2g Others: Reserved

23.77 INT2_CONFIG0

Name: INT2_CONFIG0
Address: 90 (5Ah)
Reset value: 0x80
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/W	INT2_STATUS_EN_RESET_DONE[0]	For UI/AP interface, source enable register for Reset process is finished (after OTP copy is complete, i.e. after OTP_DONE signal) interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[6]	R/W	INT2_STATUS_EN_AUX1_AGC_RDY[0]	For UI/AP interface, source enable register for Optical Image Stabilization Interface #1 AGC Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[5]	R/W	INT2_STATUS_EN_AP_AGC_RDY[0]	For UI/AP interface, source enable register for User Interface AGC Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[4]	R/W	INT2_STATUS_EN_AP_FSYNC[0]	For UI/AP interface, source enable register for User Interface FSYNC interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no any interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[3]	R/W	INT2_STATUS_EN_AUX1_DRDY[0]	For UI/AP interface, source enable register for Optical Image Stabilization Interface 1 Sensor Register Data Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

Name: INT2_CONFIG0
Address: 90 (5Ah)
Reset value: 0x80
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[2]	R/W	INT2_STATUS_EN_DRDY[0]	For UI/AP interface, source enable register for User Interface Sensor Register Data Ready interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[1]	R/W	INT2_STATUS_EN_FIFO_THS[0]	For UI/AP interface, source enable register for FIFO count ≥ FIFO threshold interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[0]	R/W	INT2_STATUS_EN_FIFO_FULL[0]	For UI/AP interface, source enable register for FIFO full interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

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23.78 INT2_CONFIG1

Name: INT2_CONFIG1
Address: 91 (5Bh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/W	INT2_STATUS_EN_APEX_EVENT[0]	For UI/AP interface, source enable register for edmp event interrupt. 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[5]	-	-	Reserved
[4]	R/W	INT2_STATUS_EN_I3C_PROTOCOL_ERR[0]	For UI/AP interface, source enable register for I3C protocol error detected by I3C Slave interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[3]	R/W	INT2_STATUS_EN_WOM_Z[0]	For UI/AP interface, source enable register for Wake On Motion event on Z axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[2]	R/W	INT2_STATUS_EN_WOM_Y[0]	For UI/AP interface, source enable register for Wake On Motion event on Y axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.
[1]	R/W	INT2_STATUS_EN_WOM_X[0]	For UI/AP interface, source enable register for Wake On Motion event on X axis interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

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Name: INT2_CONFIG1
Address: 91 (5Bh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[0]	R/W	INT2_STATUS_EN_PLL_RDY[0]	For UI/AP interface, source enable register for PLL is locked interrupt 0: Disable interrupt source. The corresponding interrupt status bit will not be set and no interrupt pin will be asserted when the specified interrupt source event occurs. 1: Enable interrupt source. The corresponding interrupt status bit will be set and the designated interrupt pin(s) will be asserted when the specified interrupt source event occurs.

23.79 INT2_CONFIG2

Name: INT2_CONFIG2
Address: 92 (5Ch)
Reset value: 0x04
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:3]	-	-	Reserved
[2]	R/W	INT2_DRIVE[0]	Sets INT2 PAD in to Open-drain or Push-pull 0: Push-pull 1: Open-drain
[1]	R/W	INT2_MODE[0]	UI/AP interface: Interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled
[0]	R/W	INT2_POLARITY[0]	UI/AP interface: Interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled

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23.80 INT2_STATUS0

Name: INT2_STATUS0
Address: 93 (5Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	R/C	INT2_STATUS_RESET_DONE[0]	For UI/AP interface, indicates if status register (ISR) for Reset process is finished (after OTP copy is complete, i.e. after OTP_DONE signal) interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[6]	R/C	INT2_STATUS_AUX1_AGC_RDY[0]	For UI/AP interface, indicates if status register (ISR) for Optical Image Stabilization Interface #1 AGC Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[5]	R/C	INT2_STATUS_AP_AGC_RDY[0]	For UI/AP interface, indicates if status register (ISR) for User Interface AGC Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[4]	R/C	INT2_STATUS_AP_FSYNC[0]	For UI/AP interface, indicates if status register (ISR) for User Interface FSYNC interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[3]	R/C	INT2_STATUS_AUX1_DRDY[0]	For UI/AP interface, indicates if status register (ISR) for Optical Image Stabilization Interface 1 Sensor Register Data Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

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Name: INT2_STATUS0
Address: 93 (5Dh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[2]	R/C	INT2_STATUS_DRDY[0]	For UI/AP interface, indicates if status register (ISR) for User Interface Sensor Register Data Ready interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[1]	R/C	INT2_STATUS_FIFO_THS[0]	For UI/AP interface, indicates if status register (ISR) for FIFO count ≥ FIFO threshold interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[0]	R/C	INT2_STATUS_FIFO_FULL[0]	For UI/AP interface, indicates if status register (ISR) for FIFO full interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: the interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

23.81 INT2_STATUS1

Name: INT2_STATUS1
Address: 94 (5Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7]	-	-	Reserved
[6]	R/C	INT2_STATUS_APEX_EVENT[0]	For UI/AP interface, indicates if status register (ISR) for edmp event interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[5]	-	-	Reserved
[4]	R/C	INT2_STATUS_I3C_PROTOCOL_ERR[0]	For UI/AP interface, indicates if status register (ISR) for I3C protocol error detected by I3C Slave interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[3]	R/C	INT2_STATUS_WOM_Z[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on Z axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[2]	R/C	INT2_STATUS_WOM_Y[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on Y axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.
[1]	R/C	INT2_STATUS_WOM_X[0]	For UI/AP interface, indicates if status register (ISR) for Wake On Motion event on X axis interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

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Name: INT2_STATUS1
Address: 94 (5Eh)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[0]	R/C	INT2_STATUS_PLL_RDY[0]	For UI/AP interface, indicates if status register (ISR) for PLL is locked interrupt is set. 0: Indicates status not set 1: Indicates status set NOTE: The interrupt pin de-assertion operation assumes the interrupt status registers assigned to consecutive addresses are read in one single burst transaction.

23.82 WHO_AM_I

Name: WHO_AM_I
Address: 114 (72h)
Reset value: 0x08
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R	WHO_AM_I[7:0]	Device ID

23.83 REG_HOST_MSG

Name: REG_HOST_MSG
Address: 115 (73h)
Reset value: 0x00
Clock Domain(s): mclk

BIT	ACCESS	NAME	DESCRIPTION
[7:6]	-	-	Reserved
[5]	RWS	EDMP_ON_DEMAND_EN[0]	Set 1 to create pulse to set int_status_edmp_on_demand_pin_0, int_status_edmp_on_demand_pin_1, int_status_edmp_on_demand_pin_2 to 1
[4:1]	-	-	Reserved
[0]	R/W	TESTOPENABLE[0]	[Supports Dynamic Change] 1: Enable test op, Read SRAM to know if the test op is for self-test(A/G)

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23.84 IREG_ADDR_15_8

Name: IREG_ADDR_15_8
Address: 124 (7Ch)
Reset value: 0xA3
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	IREG_ADDR_15_8[15:8]	[Supports Dynamic Change] DREG register for holding indirect access of IREG. Bits [15:8] If (1) CS_N=1 when in SPI, or (2) STOP when in IxC, is followed after a write operation to this register, then a read-prefetching operation to IREG is kicked off with new address. Poll register ireg_ireg_done to confirm that it is '1' before writing to this register.

23.85 IREG_ADDR_7_0

Name: IREG_ADDR_7_0
Address: 125 (7Dh)
Reset value: 0x0A
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	R/W	IREG_ADDR_15_8[7:0]	[Supports Dynamic Change] DREG register for holding indirect access of IREG. Bits [15:8] If (1) CS_N=1 when in SPI, or (2) STOP when in IxC, is followed after a write operation to this register, then a read-prefetching operation to IREG is kicked off with new address. Poll register ireg_ireg_done to confirm that it is '1' before writing to this register.

23.86 IREG_DATA

Name: IREG_DATA
Address: 126 (7Eh)
Reset value: 0x00
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:0]	RWS	IREG_DATA[7:0]	[Supports Dynamic Change] DREG register for holding indirect access IREG data. Address bit LSB = 0 A write operation to this register kicks off a write operation to IREG with the 32-bit indirect address, waiting for CS_N=1 (SPI) or STOP (IxC). A read operation to this register kicks off a read-prefetching operation to IREG with the 32-bit indirect address, waiting for CS_N=1 (SPI) or STOP (I2C). In both write and read operations to IREG, whether auto-incremented 32-bit indirect address is used or not depends on the setting of reg_ireg_auto_addr_inc_dis register. A read to reg_ireg_data gets result from previous read-prefetching operation to IREG, not the value from previous write operation to reg_ireg_data. The DREG address auto increment stops when pointing to this register. Poll register ireg_ireg_done to confirm that it is '1' before writing/reading to/from this register.

23.87 REG_MISC2

Name: REG_MISC2
Address: 127 (7Fh)
Reset value: 0x01
Clock Domain(s): sclk

BIT	ACCESS	NAME	DESCRIPTION
[7:2]	-	-	Reserved
[1]	R/W	SOFT_RST[0]	[Supports Dynamic Change] Soft reset from Host.
[0]	R	IREG_DONE[0]	[Supports Dynamic Change] 0: Indicates that an Internal IREG operation is in progress. No new IREG access should be triggered. 1: IREG access completed. New IREG access can be triggered

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24 REFERENCE

Please refer to the following application notes for additional information.

- ICM-56686 Errata (AN-000471)
- IMU PCB Design and MEMS Assembly Guidelines (AN-000393)

25 DOCUMENT INFORMATION

25.1 REVISION HISTORY

Revision Date	Revision	Description
03/25/2024	0.1	Initial Release
05/13/2024	0.2	Updated procedures for writing to and reading from an IREG (Sections 13.4, 13.5); Updated IPREG_SYS1_REG_154 (Section 20.14); Updated DREG_BANK1 register map descriptions (Section 23); Updated Reference (Section 24); Added IPREG_SYS1_REG_0, IPREG_SYS1_REG_1, IPREG_SYS1_REG_146, IPREG_SYS1_REG_148, IPREG_SYS1_REG_150 (Sections 14, 19); Added IPREG_SYS2_REG_105, IPREG_SYS2_REG_106, IPREG_SYS2_REG_107 (Sections 14, 20); Updated IPREG_SYS2_REG_117 (Sections 14, 20); Removed IMEM_SRAM_STC (Sections 13, 14, 15)
09/24/2024	1.0	Updated FIFO information (Sections 1.2, 2.4); Updated SPI speed (Cover Page; Sections 1.2, 2.4, 9.1); Updated Applications (Cover Page; Section 1.3); Added RTC (CLKIN) Timing Characterization (Section 3.7); Updated Digital-Output Temperature Sensor (Section 4.19); Updated Standard Power Modes (Section 4.22); Updated FIFO information (Section 5); Updated FIFO Header (Section 5.2); Register Map Updates (Sections 14 to 22); Updated ACCEL_CONFIG0 (Section 23.29); Updated GYRO_CONFIG0 (Section 23.30); Updated FIFO_CONFIG0 (Section 23.31); Updated RTC_CONFIG (Sections 14.9, 23.40); Updated INTF_CONFIG0 (Sections 14.9, 23.46); Updated REG_HOST_MSG (Sections 14.9, 23.83); Updated IPREG_SYS1_REG_154 (Section 20.18); Updated IPREG_SYS1_REG_157 (Section 20.20); INTF_CONFIG1_OVRD (Section 23.47); IOC_PAD_SCENARIO_OVRD (Section 23.49)

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